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High-$T_c$ SQUIDs on Silicon Substrates

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Abstract. We have developed high-$T_c$ SQUIDs based on Josephson step-edge junctions on silicon substrates. The SQUIDs show a transfer function up to $150 \mu V/\Phi_0$ and a white noise of $10^{-3} \Phi_0/\text{Hz}^{1/2}$ at 50 K. During the last three years extensive investigations of the growth of YBCO, buffer and passivation layers as well as step-preparation and patterning processes were necessary to find a standard preparation process comparable to the preparation of Josephson step-edge junctions on classical substrates. In this paper we give an overview on the technical solutions based on the laser deposition of YBCO / buffer multilayer systems and we discuss Josephson junction and SQUID properties depending on different device preparation processes.

1. INTRODUCTION

Electronic HTSC thin film devices like Josephson junctions, SQUIDs and bolometers are highly developed on substrate materials like SrTiO$_3$ or NdGaO$_3$. These “classical” substrates show a good adaption to the crystal lattice and the chemical properties of the superconductors. The use of technical substrates like silicon offers semiconductor-superconductor hybrid circuits [1] and cheaper devices. But the epitaxial growth of HTSC films on silicon is much more complicated as on SrTiO$_3$ as the result of lattice mismatch, interdiffusion effects of YBCO and silicon and the large difference in their thermal expansion coefficients. Thus, thin YBCO films on silicon with applicable electrical properties require epitaxial buffer layers and a YBCO film thickness smaller than 50 nm to avoid cracks [2]. This limitation requires high epitaxial YBCO films, well defined step-edges as well as a YBCO surface passivation to avoid degradation processes during measurements in cryogenic media. Significant progress was obtained by use of three technologies: a) application of the double buffer system YSZ (yttrium stabilized ZrO$_2$) / CeO$_2$ [3,4], b) shift of the step-preparation process from the silicon substrate to the first buffer layer [4], c) development of a crack free YBCO passivation layer [5].

2. EXPERIMENTAL RESULTS

2.1 Film deposition and patterning

The laser deposition technique was used to prepare all layers: the buffer layers YSZ and CeO$_2$, the YBCO films and the silver layer for contact pads. The standard preparation process of the Josephson step-edge junctions includes two parts of film deposition and two parts of film patterning [6]. After deposition of the first buffer layer the vacuum process is interrupted for photolithography and ion beam etching of 35-45 nm deep steps in the YSZ film. The second part of deposition starts with the CeO$_2$ buffer. Then we deposit 25-40 nm thick epitaxial c-axis oriented YBCO passivated by a second non-superconducting YBCO layer with a modified crystal structure and a thickness of about 70 nm. After deposition of the silver layer for contact pads the patterning is necessary to prepare the YBCO bridge structure. Figure 1
shows a SEM picture of a realized layout including 5 dc-SQUIDs and 2 single Josephson junctions. The bridge width varies between 4 and 10 μm, the SQUID-loops have a size of 5-25 μm².

To simplify the preparation process we have further investigated an unification of the two patterning parts to one process using an inhibit technology. The idea is to etch directly after the YSZ step preparation through the YSZ buffer into the silicon substrate with the same mask used for the YBCO patterning. Thus, in the second vacuum process the CeO₂ and YBCO films grow epitaxially only in the area of the prospective device (Figure 2). The device is now complete after film deposition and ready for electrical measurements. First realizations of such SQUID devices will be shown elsewhere [7].

Our non-superconducting YBCO layer on top of the superconducting YBCO realizes the passivation of the whole device as well as low resistance contact pads in connection with the silver top layer. An important property of this material is that its film thickness of more than 100 nm can be observed without cracks. The reason of this behaviour is the difference in the crystal structure compared to the superconducting c-axis YBCO deposited at a substrate temperature of 700°C. The non-superconducting YBCO deposited at 500°C has a lattice constant perpendicular to the substrate surface of 3.8 Å (see Fig. 3). But further XRD and TEM investigations did not show an in-plane alignment of the c-axis like for common a-axis oriented films. Detailed results about the crystal structure of this kind of YBCO films including HR-TEM studies are in preparation [8].

**Figure 1**: SEM image of realized layout with seven devices on a buffered silicon chip

**Figure 2**: Scheme of complete film system utilizing inhibit process

**Figure 3**: XRD 2θ-scans of multilayer systems YBCO / CeO₂ / YSZ on silicon substrate for different deposition temperatures of YBCO. Parenthesis indicate the reflexes for c-axis and a-axis oriented YBCO

**Figure 4**: R(T) curve of a Josephson step-edge junction with etched step in the YSZ buffer layer
The superconducting properties depend very strongly on the preparation conditions. The etching of steps directly in the silicon substrates led to critical temperatures of step-edge junctions below 20 K. Only for a junction width of about 10 μm or more we find Josephson behaviour in these junctions. The current distribution in the junction area was very inhomogeneous and was temporal unstable [9]. The etching of steps in the buffer layer overcomes these problems [4]. The operation temperature rises up to boiling point of liquid nitrogen. The temperature dependence of the Josephson junction resistance shows a footstructure below the critical temperature of a patterned YBCO film, typically for a lot of grain boundary junctions (Fig.4). To produce step-edge junctions on silicon substrates we used nearly the same ratio of the step height h to the film thickness d as determined from investigations on SrTiO₃ substrates [10]. For these step-edge junctions with laser ablated YBCO films we find Josephson behaviour for a ratio h/d between 1.2 and 1.4. For our steps on silicon substrates we varied the step height between 35 and 45 nm using the same ratio h/d successfully. Due to the improved etching technology for preparation of steps we were able to reduce the junction width down to 4 μm. With a YBCO film thickness of 30 nm the realized junction area of 4.5·10⁻⁹ cm² is in the same order like the area of our step-edge junctions on SrTiO₃ substrates [10].

For the microbridges without Josephson junctions we found critical temperatures up to 86 K as well as critical current densities at 77 K in the range of 1·10⁶ A/cm².
Our Josephson junctions show RSJ-like I-V characteristics up to $T_c$ (Fig. 5). We found a clear modulation of the Shapiro steps in the current-voltage characteristics depending on the microwave power up to $T_c$ (see Fig. 6). The critical current can be suppressed in external magnetic fields but not to zero. Figure 7 shows the magnetic field dependence of the current-voltage characteristics of a Josephson junction with a width of 6 µm. These results were comparable to our best step-edge junctions on SrTiO$_3$. The $I_cR_N$ products ranged from 0.3 to 0.8 mV at 70 K depending on the preparation conditions. The lower $I_cR_N$ products observed for step-edge junctions without passivation layer were also comparable to our best step-edge junctions on SrTiO$_3$ substrates with a standard film thickness of 120nm. With the non-superconducting YBCO passivation layer we realized Josephson junctions with time stable superconducting properties and low contact resistance. We also observe a drastical change in the normal resistance of these step-edge junctions. For the same critical current the normal resistance increases about a factor 5 to 10. But we measured also for the step-edge junctions with the passivation layer the same temperature dependence of the critical current density as for other grain boundary junctions (Fig.8). Based on these junctions we started to prepare dc-SQUIDS with a SQUID inductance between 20 and 40 pH depending on the loop area, the junction width and the film thickness. The realized loop area is for the same SQUID inductance smaller as for our step-edge or bicrystal junctions on SrTiO$_3$, caused by the thinner YBCO films.

We found a maximum SQUID transfer function of about 150 µV/$\Phi_0$ at 50 K (see Fig. 9). The noise properties with a white noise level below $10^{-4}$ $\Phi_0$/Hz$^{1/2}$ up to 50K (Fig.10) are comparable to our step-edge junction SQUIDs on SrTiO$_3$ substrates with significant thicker YBCO films [11]. Further we are now able to investigate SQUIDs on silicon substrates for a much longer time with the same noise properties using the non-superconducting YBCO film as a passivation layer.

3. SUMMARY

High-$T_c$ Josephson junctions and SQUIDs with working temperatures up to 77 K were prepared on silicon substrates using an improved multilayer technology. The properties of these devices are comparable to those on SrTiO$_3$ substrates. Even the $I_cR_N$ products can be one order higher if a passivation layer of non-superconducting YBCO is used. The nature of this layer will be studied in further investigations.

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