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Abstract. The SAIL (self-aligned in-line) technique has been applied to the preparation of ultrasmall metallic tunnel junctions. By using e-beam lithography and sputter methods the area of both $Al/AlO_x/Al$ and $Nb/AlO_x/Nb$ contacts has so far been reduced to less than $0.005\mu m^2$. At low temperatures high-ohmic double junctions with a small metallic island in between show the Coulomb blockade effect. The current through such a device can be modulated by a voltage applied to a gate electrode capacitively coupled to the island (single-electron transistor). Both these single-charge phenomena have been observed at temperatures of a few hundred mK.

1. INTRODUCTION

One of the simplest devices of single-electron tunneling (SET) electronics [1] is a double junction with a small conducting island between the tunnel contacts. Two conditions must be fulfilled to observe SET effects. The capacitance of the junctions must be low enough to satisfy the relation $e^2/2C_\Sigma \gg k_BT$ (C_Σ is the total capacitance of the island) for suppressing thermal fluctuations of charge on the island. Furthermore, the resistance of the tunnel junctions must be much higher than the quantum resistance $R_Q = h/e^2 \approx 25.8k\Omega$ to avoid quantum fluctuations. Tunnel junctions with lateral dimensions in the submicron range for single-charge devices have been fabricated usually by the shadow evaporation technique [2,3]. In this work we describe how the so-called self-aligned in-line (SAIL) technique [4,5] may be applied to the fabrication of ultralow capacitance SET transistors based on $Al/AlO_x/Al$ and $Nb/AlO_x/Nb$ edge tunnel junctions. We report measurements of the Coulomb blockade and of the current modulation by a gate voltage in these devices [6] in the temperature range $300 - 350mK$.

2. FABRICATION TECHNIQUE

The principle of the SAIL process can be outlined as follows: The tunnel junction is prepared at the edge of a thin base electrode thus restricting one of the dimensions of the junction to the film thickness. By using a very narrow stripline the lateral dimension can be kept small as well. The mask required for etching a transverse edge into the stripe serves as a lift-off stencil after etching, barrier generation and deposition of a second metallic film. This way a small-area junction may be fabricated perpendicular to the substrate plane.

The SAIL conception consists of the following steps:

1. preparation of a thin narrow metallic stripline on the substrate [see Fig. 1(a)],
2. generation of a resist mask, which leaves uncovered the area of the future counter electrode [Fig. 1(b)],
3. anisotropic etching of the stripline [Fig. 1(c)],
4. formation of a dielectric barrier at the surface of the metal edge [Fig. 1(d)],
5. deposition of the second metallic film [Fig. 1(e)],
6. lift-off process [Fig. 1(f)].

The mask generated in the second step fixes the position of the barrier as well as the shape and position of the counter electrode. Lengthwise positioning is automatically accurate due to self-alignment. Shifts in the transverse direction can be easily compensated by patterning a slightly wider second electrode.

Since it is to be used as a lift-off stencil the mask must have an undercut, i.e. a negative slope of the resist edges. In the case of e-beam lithography one can simply take advantage of the natural electron distribution (scattering volume) to obtain a suitable undercut.

The barrier generation is carried out after the last e-beam exposure and the ion beam etching. By this method a damage of the barrier by high-energy electrons or ions can be prevented. Finally, the counter electrode is created by sputtering and subsequent lift-off process.

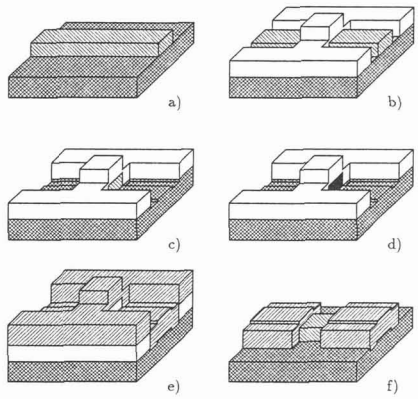

Figure 1: Scheme of the SAIL preparation of two in-line junctions. The substrate is depicted by crosshatching and the electrodes are marked by diagonal lines (see text).

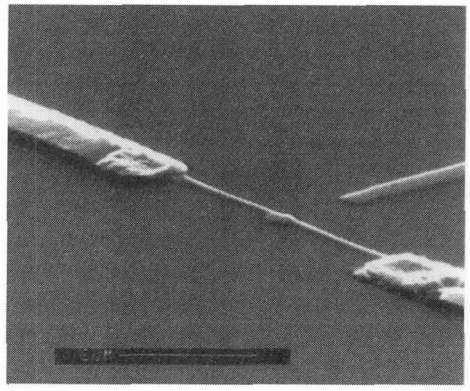

Figure 2: SEM micrograph of an $Al/AlO_x/Al$ SET transistor fabricated by SAIL technique.

3. SAMPLE PREPARATION

We have prepared both Al based (see Fig. 2) and (in contrast to Harada et al. [7]) all-Nb based SET transistors consisting of two junctions in series and a capacitively coupled gate electrode.

The base electrode stripline was typically $50nm$ thick and $80 - 150nm$ wide. It was patterned in a lift-off process. The stencil was made of an AR-P 610 [8] resist of about 150 nm thickness. The exposure was carried out in the LION LV1 [9] e-beam lithographical system. In order to obtain a suitable undercut of the stencil the accelerating voltage of the electron beam ($10 - 15\ kV$) was matched to the thickness of the resist. The metals were deposited by sputtering.

The second mask was based on a doublelayer resist consisting of a higher sensitive lower layer of $400nm$ AR-P 641 and $250nm$ AR-P 671 [8] on top. It was exposed in the LION LV1 facility, too, the pattern linewidth was kept $150nm$ approximately. The gate electrodes of the SET transistors are patterned also with this mask. By this method the positioning accuracy of the lithographical system does not affect the distance and the coupling capacitance between gate and island electrode.

For anisotropic etching we used an Ar ion beam of $120mm$ diameter, an energy of about $500eV$ and a current density of $380 - 400\mu A/cm^2$. Since the aluminum etch rate is approximately $25nm/min$ for these parameters, the etch step took about $2.5min$. We found that the thickness of the resist mask was typically reduced by $100 - 130nm$ in this time. Immediately after etching the dielectric barrier was generated by oxidation in dry air at a pressure of $200Pa$ in the lock chamber of the high vacuum facility. Subsequently, but in the same vacuum cycle as the previous two steps, the second aluminum film was deposited by sputtering.

Our Nb transistors are fabricated on principle in the same way as described in Fig. 1. However, for the formation of the barrier the edge was first covered by sputtering a layer of a few nanometers Al, then the Al was oxidized.

4. EXPERIMENTAL RESULTS

We have fabricated several wafers with SET devices. The high-voltage tunnel resistances of working devices were in the range of several $10M\Omega$. Transistors close together on one wafer had quite similar resistances.

The measurements were carried out in a ^3He-cryostat at temperatures of about $300 - 350mK$.

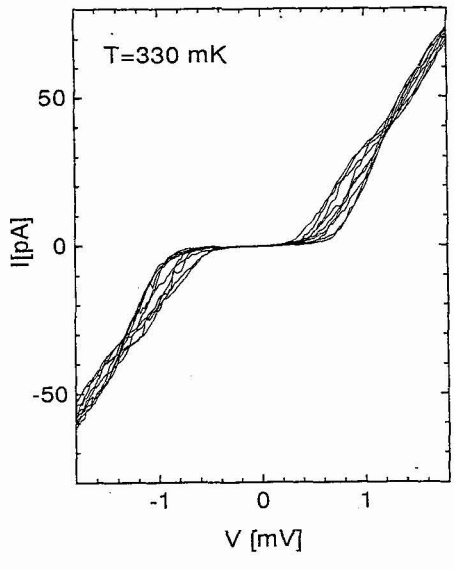

Figure 3: A family of $I - V$ quasiparticle characteristics of an $Al/AlO_x/Al$-type SET transistor for different values of the gate voltage V_g. Here the variation δV_g corresponds to an island charge spread $\delta Q = e$.

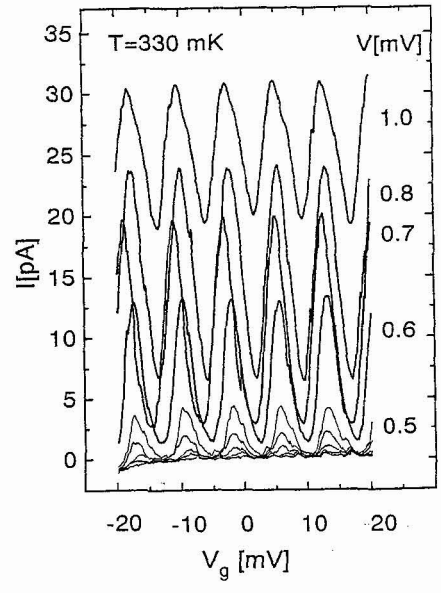

Figure 4: Current modulation characteristics of the same Al based SET transistor for several values of the bias voltage V.

In Fig. 3 we show a family of $I - V$ characteristics of an $Al/AlO_x/Al$ SET transistor at varying gate voltage V corresponding to the regime between complete Coulomb blockade and total de-blockade. The superconductivity was not reduced (or even suppressed) by a magnetic field. Therefore, one recognizes the

expected superconducting quasiparticle tunneling. The absence of a striking Coulomb staircase indicates that the individual junctions may be considered as very similar [10]. From the asymptotic behaviour of the $I-V$ curves and the bias voltage for the maximum current modulation we have estimated the capacitance of a junction and the superconducting energy gap $2\Delta_{(Al)}$ [11] to be less than $0.2fF$ and approximately $0.2meV$, respectively. The measured capacitance agrees well with values calculated from the geometrical dimensions of a tunnel junction with an area of $50 \times 100nm$ and a barrier thickness in the nanometer range.

The corresponding current modulation characteristics, I vs. V_g, are shown in Fig. 4. The capacitance between gate and island can be taken from the period of the modulation; it is about ten times smaller than the junction capacitance.

In Fig. 5 we show an $I-V$ characteristic of a $Nb/AlO_x/Nb$ transistor with complete Coulomb blockade and geometrical dimensions like the $Al/AlO_x/Al$ transistor described above. Finally, Fig. 6 shows several I vs. V_g characteristics of the same device. Here we have determineded a sum gap $2\Delta_{(Nb)}$ of about $2.5meV$. The junction capacitance was estimated to be less than $0.2fF$; from the current modulation period we have determined the gate capacitance of $0.04fF$.

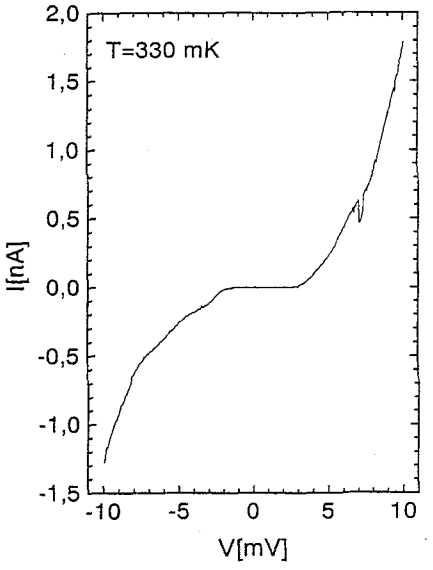

Figure 5: $I-V$ characteristic of a Nb based SET transistor fabricated by SAIL technique.

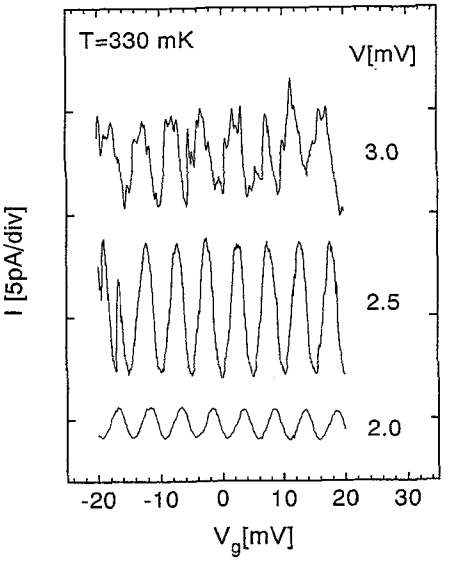

Figure 6: Current modulation ($I - V_g$) curves of the same $Nb/AlO_x/Nb$ SET transistor.

It should be mentioned that the Al devices have shown a remarkable stability of a few months without any protection against atmospheric influences. Because of rare experiences we are not able to give corresponding dates for the Nb samples up to now.

5. CONCLUSIONS

We have shown that the SAIL process can be used for the fabrication of both Al and Nb based SET devices. Due to its simplicity and the possibility to use sputter deposition methods, the SAIL technique should be applicable to other, especially, high-melting metals, too.

Up to now, the dimensions of our structures are still much larger than the resolution limit of the LION LV1 lithographical system, and we expect to be able to reduce the dimensions further.

ACKNOWLEDGMENTS

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REFERENCES

[1] Averin D.V., Likharev K.K., Single Charge Tunneling – Coulomb Blockade Phenomena in Nanostructures, NATO ASI Series B: Physics, Vol. 294, H. Grabert and M.H. Devoret Eds. (Plenum Press, New York and London, 1992) pp. 311-332.
[2] Niemeyer J., PTB-Mitt. **84** (1974) 251-253.
[3] Dolan G.J., Appl. Phys. Lett. **31** (1977) 337-339.
[4] Koch H., "Self-Aligned In-Line Junction – Fabrication and Application to DC-SQUIDs", Int. Supercond. Electr. Conf., Tokyo August 1987 (Extended Abstracts) pp. 281-284.
[5] Houwman E.P., Cantor R., Peters M., Scheer H.-J., Koch H., IEEE Trans. Magn. **MAG–25** (1989) 1147-1150.
[6] Fulton T.A., Dolan G.J., Phys. Rev. Lett. **59** (1987) 109-112.
[7] Harada Y., Haviland D.B., Delsing P., Chen D.C., Claeson T., Appl. Phys. Lett. **65** (1994) 636-638.
[8] reg. TM of All Resist GmbH, Berlin, Germany.
[9] reg. TM of Jenoptik GmbH, Jena, Germany.
[10] Ingold G.-L., Nazarov Yu.V., Single Charge Tunneling – Coulomb Blockade Phenomena in Nanostructures, NATO ASI Series B: Physics, Vol. 294, H. Grabert and M.H. Devoret Eds. (Plenum Press, New York and London, 1992) pp. 21-107.
[11] H.-O. Müller, unpublished.