Enhancements and Degradations in Ultrashort Gate GaAs and InP HEMTs Properties at Cryogenic Temperatures: an Overview

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Abstract : Enhanced performances of III-V field effects transistors are generally expected at cryogenic temperatures thanks to the better confinement and the velocity of carriers. An overview of our recent work on ultrashort gate-length HEMTs on GaAs and InP substrates at low temperature is presented in this paper. The compared behavior of the devices and the relative enhancement or degradation of their low and high frequency properties are discussed. The study is based on a set of device experimental characterizations on chip and device simulations. At cryogenic temperatures, trapping effects, impact ionization and classical short channel effects are enhanced while device self-heating associated with large current densities appear to decrease.

1. INTRODUCTION

Low temperature analysis (LTA) of state of the art devices allows to investigate the second order phenomena which limit their HF performances. LTA is a powerful tool to extrapolate the device performances versus their critical parameters. In this paper, we present the interest of LTA when cooling ultrashort gate-length GaAs and InP HEMTs. At cryogenic temperatures, both the good and the detrimental effects are much better underlined in the device. The analysis uses an important data base of simulations and experimental results both on GaAs and InP HEMTs. In the wide range of temperatures (50 K - 300 K), DC, pulsed and HF (0.5-50 GHz) characterizations on chip have been achieved [1-3]. Precise on chip calibrations at each temperature give an excellent accuracy to the results which allows to extract the device intrinsic parameters. Deep Level Transient Spectroscopy (DLTS) analysis and electroluminescence have also been carried out [4, 5]. Simulations are based on a temperature dependent quasi bidimensionnal hydrodynamic model (Q2D) [6], in which momentum and energy relaxation times have been calculated by Monte Carlo simulations [7]. Deep levels are not taken into account in this model; this gives informations on low temperature performance improvements if detrimental effects as trapping effects are not considered.

This paper is divided in four parts. We describe, first, the devices studied. Secondly, we present the evolution expected at low temperatures with simulations. Next, the improvements of DC and HF performances versus temperature are presented. The detrimental effects which limit the performance of the shortest gate-length HEMTs are discussed in the last paragraph.

2. DEVICES DESCRIPTION

The InP HEMTs studied consist of a 600 Å lattice-matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel growth on a 1500 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer on InP substrate. The channel is followed by a 35 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ spacer, a 110 Å Si doped layer ($6.0 \cdot 10^{18} \text{ cm}^{-3}$), a 220 Å undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer for the Schottky contact and a 50 Å undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer. The gate-lengths are from $L_g = 0.2 \mu\text{m}$ up to $5 \mu\text{m}$. A mixed and matched process has been applied in HEMT fabrication. Mesa area and electrode pads are fabricated using optical lithography. The gates are patterned by e-beam lithography (JEOLJBX5DII). The device is single recessed. The GaAs pseudomorphic HEMTs consists of a 120 Å strained $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel growth on a 2500 Å GaAs buffer. The channel is followed by a 50 Å $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ spacer, a 150 Å undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ layer with a $5.0 \cdot 10^{12} \text{ cm}^{-2}$ delta-doping above the spacer, a 800 Å $3.0 \cdot 10^{18} \text{ cm}^{-3}$ doped GaAs cap layer. The gate-lengths are from $L_g = 0.1 \mu\text{m}$ up to $0.4 \mu\text{m}$. The process is the same as for InP.

3. QUASI-2D-HYDRODYNAMIC (Q2D) SIMULATIONS

Simulations of Schrödinger equation in a AlGaAs/InGaAs/GaAs pseudomorphic HEMT (P-HEMT) at various temperatures are presented in Fig.1. This figure shows the ratio of carriers located on the first sublevel in the InGaAs quantum well versus gate voltage V_{gs} . We notice that the population rate of electrons on the first sublevel increases at low temperature. Moreover, the ratio of electrons inside the well for very positive values of V_{gs} remains significantly larger at cryogenic temperatures than at 500 K as seen in the inset of Fig.1. These results allow to conclude that electrons confinement improve at cryogenic temperature.

We follow now the incidence of the improvement of carriers velocity and confinement at low temperature from a quasi-2D hydrodynamic model Q2D [6]. Q2D simulations exhibit interesting results from the quantitative increase of intrinsic parameters of devices neglecting trapping effect or impact ionization. Q2D simulations show that average carriers velocity peak (located at the end of the gate) increases at low temperature as expected while low field mobility improvement is beneficial for access area.

Fig.1 : Simulation of carriers repartition in AlGaAs/InGaAs/GaAs HEMT

Fig. 2 : Simulations of IV characteristics for a 0.15 μm gate-length GaAs P-HEMT

The Fig.2 shows simulations of the IV characteristic of 0.15 μm gate length GaAs P-HEMT at 300 K and 100 K. The drain-source current I_{ds} and also transconductance G_m , are enhanced when cooling down the HEMT. As quasi static capacitances gate-source C_{gs} and gate-drain C_{gd} remain practically constant versus temperature, the current gain cut off frequency F_t increases at low temperature.

Fig.3 : Simulations of intrinsic current gain cut off frequency for a 0.15 μm gate-length GaAs PHEMT

Fig.4 : Simulation of the output conductance of a GaAs P-HEMT

The Fig 3 shows the evolution of F_t versus gate voltage at different temperatures (300 K, 200 K, 100 K). At 100 K, F_t is about 35 % larger than the 300 K one. An improvement in the same range is obtained by Q2D simulations for long gate device ($L_g=0.7 \mu\text{m}$) and for the shorter one $L_g=0.15 \mu\text{m}$. Nevertheless Q2D simulations show that some detrimental effect can be expected at low temperature : the output conductance G_d increases at low temperature (Fig.4) and the threshold voltage V_{th} shifts towards more negative values.

The main explanation is that, in both cases (low temperature and short gate), the carrier transport under the gate improves. When the gate becomes very short the non stationary transport increases, all the totality of the carriers can't relax under the gate. When the temperature is reduced, the carriers velocity increases due to reduction of electron-phonon interaction rates.

We have observed the incidence of carrier velocity improvement at low temperature on electrical parameters such as G_m , G_d , F_t , I_{ds} and V_{th} . On the other side, the improvement of electron confinement does not appear to have a noticeable influence on the low temperature behavior. We must underline here that simulations on carriers repartition rate in Fig.1 does not take into account the effect of carrier transport. Validity of a such simulation requires no drain voltage bias or a very small one. The lateral electric field heat carriers which repartition becomes very far from the one simulated in Fig.1. Moreover at low temperature carriers are able to gain more energy from the lateral electric field than at 300 K due to the improvement of electron velocity. If the "dynamic" confinement improved, measured capacitances would be smaller and both G_d and V_{th} should decrease when cooling down the device. The shift of threshold voltage towards more negative values, the degradation of output conductance G_d and the absence of evolution of capacitances versus temperature show that the improvement of cold carriers confinement on the lowest sublevel is screened by the improvement of carriers transport properties at low temperature.

In conclusion, we can stress on that cooling down a device increase noticeably I_{ds} , the current gain cut off frequency, and transconductance while output conductance and threshold voltage are affected. The trend on InP based HEMTs simulations gives similar results to GaAs ones. However, the discrepancy between the technological doping and the real one (due to large traps in InAlAs layers) means an over estimation of carrier confinement by Q2D in InAlAs/InGaAs/InAlAs heterojunctions. This gives difficult to obtain precise simulations of InP HEMTs.

4. DC AND HF PERFORMANCES ENHANCEMENT AT LOW TEMPERATURE

The main experimental evolutions observed with DC and HF measurements on GaAs and InP HEMT at low temperature are now discussed. The Fig.5-6 show I-V characteristics of a 0,2 μm and 0,6 μm gate-length lattice matched InP based HEMT at 300 K and 50 K. We, first, notice that I_{ds} increases at low temperature as expected but the improvement is not very significant. I_{ds} increases about 12% in saturation regime for $V_{gs}=0,2$ V between 300 K and 50 K for both 0,2 μm and 0,6 μm . Maximum I_{ds} value is weakly larger for the shorter gate. An explanation in this limited evolution is the lack of doping in cap layers for these devices.

Fig.5 : I-V characteristic of a 0,2 μm InP LM-HEMT
(Small kink effect at T=50K)

Fig.6: I-V characteristic of a 0,6 μm InP LM-HEMT
(Small kink effect at T=50K)

For gate voltage near the threshold voltage drain current is weaker at low temperature than at 300 K. But the evolution of threshold voltage at low temperature is difficult to analyse because various antagonist physical mechanisms occur at the same time. For standard AlGaAs/GaAs HEMTs threshold voltage observed under illumination is negative while it can be alternatively positive or negative in the dark according to the experimental conditions of measurements. For GaAs P-HEMT under illumination, the V_{th} shift is slightly negative but it is positive in the dark; for InP based HEMT, it is generally positive whatever illumination conditions. This last observation is discussed further.

Slope of drain current versus drain source voltage increases at low temperature because access resistances are reduced. The reduction of all the parasitic access resistances R_g , R_s and R_d when the transistors are cooled down is an important asset for low power and low noise applications. In all HEMT structures

investigated the gate resistance reduction is about 50-60% between 300 K and 50 K while the reduction of source and drain resistances is 20-30% in the same temperature range. This reduction of resistances allows an important increase of the maximum frequency of oscillation $F_{\max}$ at low temperature whatever the gate length. The Fig.7 shows the reduction of source and gate resistances versus temperature for a 0.15 μm GaAs HEMT. These resistances have been obtained with HF measurements. Determination of accurate access resistances requires very precise calibration and the embedding of the access coplanar waveguides. The reduction of parasitic access resistances allows to use these devices in low power applications.

Fig. 7 Access resistances for a 0.15 μm gate-length GaAs P-HEMT (HF measurements)

Fig.8: Intrinsic current gain cut off frequencies of LM-HEMT on InP

Thanks to the improvement of carriers velocity at cryogenic temperature, the intrinsic current gain cut off frequency F_{ij} increases. Experimental results show that the improvement of F_{ij} depends on, mainly, the gate-length (Fig.8). The longer the gate is, the larger the F_{ij} increase is. We underline about the F_{ij} variations a strong parallelism between the effect of reducing gate length and cooling down the device as discussed before. A similar parallelism occurs for the variation of the output conductance as well as for the threshold voltage shift. One can notice that similar results are obtained with Q2D simulations. We can thus conclude that the improvements or the degradations observed in the experimental results presented here are largely explained by the improvement of carriers transport properties at low temperature.

Due to the good confinement of carriers, the very high energy reached by a fraction of carriers and the poor thermal conductivity of III-V materials, self heating of HEMT devices can occur [1]. The best devices are heavily doped to reach large current densities which enhances detrimental mechanisms. The electroluminescence results have shown that in the drain access region, the substrate temperature increases at the hot spot can reach 150 K if the holder temperature is 300 K [4]. At low temperature no significant temperature increase is observed experimentally and the simulations confirm the experimental observations [6].

5. DETRIMENTAL EFFECTS

In Paragraph 4, we have stressed on some detrimental effects associated with cooling down an ultrashort gate HEMT. We have also pointed out twice strong parallelism between reducing gate-length and cooling down the device.

The first detrimental effect is the reinforcement of the so called "short channel effects"[3]. In all studied structures, short channel effects, due to the control of electrons located under the gate by the drain electrode increase when the transistor is cooled down. The output conductance G_d and the threshold voltage shift increase at low temperature. These phenomena are sometimes screened by trapping effects as discussed before. For GaAs devices an increase of the intrinsic output conductance is always observed. On the other side this is not observed in InP devices due to a very good confinement of carriers even in L satellite valley. However the intrinsic output conductance is generally higher at each temperature for InP devices than for GaAs ones devices due to the very good transport properties of the channel. An other traditional degradation associated with short channel effect is the saturation of the improvement of transconductance for gate length around 50-150 nm. We generally observe that improvement of intrinsic transconductance is relatively weak at low temperature. This evolution can be strongly affected by trapping effect, particularly in the dark.

The second detrimental effect revealed by LTA is carrier trapping effects. The Si doped AlGaAs layers contain DX centers at the same concentration as doping. If they have been discussed already in many papers, our study point out that in GaAs HEMTs the shorter the gate-length, the stronger are the effects of DX centers [1]. Aspects of carrier trapping on DX centers in high electric fields can be considered as a short channel effect. In comparison there is no DX-like trapping center in InP based devices and we show in a systematic analysis that the kink effect (Fig.9) in the IV characteristic is mainly due to carrier detrapping while the collapse is due to carrier trapping of carriers both located in InAlAs layers [2].

The third detrimental effect which is not the least revealed by our study is impact ionization. Electroluminescence experiments in both GaAs (Fig.10) [4] and InP [5] HEMTs have shown that impact ionization takes place in the channel. The strong luminescence intensity increase at cryogenic temperature is due to the increase of radiative relaxation processes versus non radiative ones and to the relative increase of the mean free path associated with high energy phonons (optical and acoustical) versus mean free path between two ionization collisions. The gate current peak intensity associated with impact ionization does not vary in the same way for GaAs and InP transistors. This may be due to the increase of radiative mechanism.

Fig.9: I-V characteristic of a 0.2 μm gate-length InP HEMT under light and in the dark

Fig.10 : Electroluminescence spectra of a 0.1 μm gate-length GaAs P-HEMT

6. CONCLUSION

The low temperature analysis allows to understand that at least four mechanisms occur which limit HF performances of ultrashort gate-length HEMTs. The first one is the classical so called short channel effect, due to the control of electrons located under the gate by the drain electrode, which is responsible for threshold voltage shift and output conductance increase. The three others are revealed by low temperature analysis and are deep level effects, impact ionization and self heating. The study shows that in-depth investigation of short gate HEMTs at low temperature is rich in new informations and allows a better understanding of the physical origin and the mechanisms involved in the enhancement or the degradation of HEMTs properties versus gate-length and temperature.

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