Threshold Voltage Characteristics of Superconductor Gate nMOSFET at 4.2 K

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Abstract. We propose a high mobility superconductor gate nMOSFET using undoped Si as the substrate. We have studied superconducting NbN gate nMOSFETs fabricated on p-type Si, undoped Si and n-type Si substrate, respectively. The nMOSFETs on undoped Si and n-type Si have operated properly at 4.2 K. The transconductance of nMOSFETs on undoped Si substrate is higher than that of nMOSFET on p-type Si. The difference in transconductance is attributed to the difference of impurity density in channels. The observed threshold voltages of NbN gate nMOSFETs on p-type Si, undoped Si and n-type Si have little difference at 4.2K.

1. INTRODUCTION

Much investigation has shown that many benefits are obtained from the operation of Si MOS devices at very low temperature [1,2]. Up to the present, however, performance improvement of room temperature Si MOS devices have been achieved steadily through the miniaturization of device feature sizes. On the other hand, superconductive electronics based on Josephson devices of low temperature superconductors (LTS) and high temperature superconductors (HTS) have been developed year by year. Recently, hybrid circuits consisting of semiconductor and superconductor devices have attracted much interests to utilize the advantages of each technology [3,4]. Superconducting Josephson integrated circuits (ICs) have demonstrated a promising potential for fast and low power devices for use in digital systems, e.g., Josephson computers [5]. However, one serious problem is how to obtain an easy access from ordinary semiconductor systems at room temperature to the systems based on Josephson ICs. The barrier between semiconductor- and superconductor-systems is formidably high. The difficulties arise not only from the difference of operational temperatures but also from the differences in the speed and levels of the signals processed by the two systems. Therefore, the interface between semiconductor and superconductor circuits is a very important issue to realize superconducting digital systems.

To demonstrate such interface circuits, we have fabricated a superconducting NbN gate nMOSFET on p-type Si with a self-aligned gate technique [6]. The superconductor gate FET will make it simple to fabricate superconducting Josephson devices and MOSFETs on the same substrate, which is a monolithic hybrid integrated circuit, since Josephson ICs are usually made of Nb or NbN films on Si substrates. Such monolithic hybrid ICs will operate at liquid He temperature (4.2K). It is well known that the mobility of Si with lower impurity concentration is higher at low temperature. Therefore, a high mobility FET operated at low temperature is expected to be realized with low impurity density in the channel. In this paper, we propose a high mobility superconductor gate nMOSFET using undoped Si as the substrate and report the characteristics of the fabricated nMOSFETs at 4.2K. Using the undoped Si substrate makes the fabrication process simple, especially for fabricating CMOS devices because the process of making wells can be omitted. We also fabricated the superconductor gate nMOSFETs on p-type Si and n-type Si substrates with the same fabrication process for reference. The nMOSFETs on undoped Si and n-type Si have operated properly at 4.2 K. The transconductance of nMOSFETs on undoped Si substrate is higher than that of nMOSFET on p-type Si, the difference is attributed to the difference of impurity density in the channels. The observed threshold voltages of NbN gate nMOSFETs on p-type Si, undoped Si and n-type Si show little difference from each other at 4.2K. However, one Nb gate nMOSFET had a threshold voltage of about 1.1V at 4.2K, which is 0.5V lower than the threshold voltage of NbN gate nMOSFET. The threshold voltage can be controlled at 4.2K by selecting the gate material which has an appropriate value of work function.

2. FABRICATION PROCESS OF SUPERCONDUCTOR GATE MOSFET

We have studied the possibility of using superconducting Nb and NbN as gate electrodes of self-aligned MOSFETs. Nb and NbN, which are classified as high melting point materials, have been used as basic materials for fabricating Josephson devices. If they can keep their superconductivity after thermal annealing in the self-aligned MOSFET fabrication process, power dissipation and delay in circuits will be dramatically improved. However, Nb group superconductors are known to be very active materials and it was reported that thermal annealing degrades superconductivity [7]. We have found that NbN films are stable against thermal annealing and NbN gate electrodes of nMOSFETs fabricated with the following process retain their superconducting properties [6]. Figure 1 shows our fabrication process for making a superconducting NbN gate nMOSFET. SiO_2 (about 55nm thick) is grown on Si wafer by thermal oxidation for 60 min at 1000°C as shown in Fig.1(a). To make the self-aligned superconducting gate, NbN film is deposited on SiO_2 by rf magnetron sputtering of a Nb target using a gas mixture of N_2, Ar and CH_4 (Fig.1(b)). Gate structures are made by reactive ion etching(RIE) of NbN and SiO_2. Etchant gas is CF_4 for etching NbN and mixed gas of CF_4 and H_2 for SiO_2, respectively. After making gate structures by the RIE process, P^+ ions are implanted with a dose of $5x10^{15}$ cm^{-2} at 50 keV and then samples are annealed for 30 min in dry N_2 at 800°C to form the source and drain regions (Fig.1(c)). This annealing condition makes no difference in superconducting transition temperature (T_C) of NbN film before and after annealing. NbN gates remain superconducting and have a T_C of about 15K after this process. SiO_2 for insulation is then sputtered and contact holes are opened by RIE with mixed etchant gas of CF_4 and H_2 (Fig.1(d)). After depositing a Nb film on the surface by dc sputtering for interconnection, contact electrodes are patterned by RIE with etchant gas of CF_4 (Fig.1(e)).

In this work we fabricated the NbN gate nMOSFETs on undoped (100) oriented Si wafer for obtaining a high mobility at very low temperature. Naturally it is very difficult to obtain intrinsic Si. We used an undoped FZ(float zone) Si wafer with over 1000 Ω·cm resistivity. Its impurity density was very low but non-zero. The carrier type was n. For reference we also fabricated the NbN gate nMOSFETs on B doped p-type and P doped n-type (100) oriented Si wafers, respectively. The resistivity of the p-type Si is 3 - 5 Ω·cm and that of the n-type Si is 3 - 10 Ω·cm. The fabricated nMOSFETs have the gate length of 2 - 10μm and the gate width of 50μm.

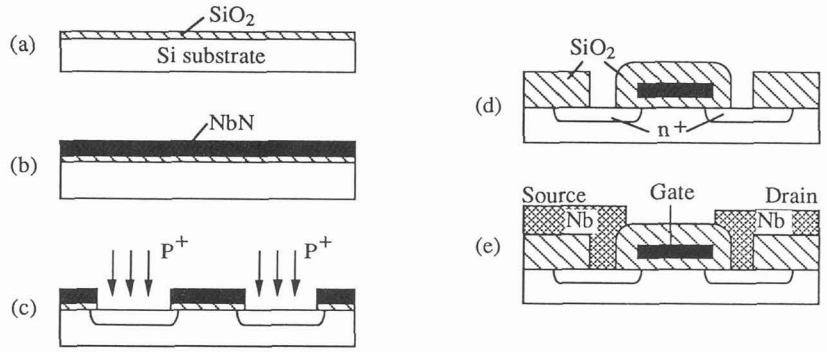


Figure 1: Fabrication process of NbN gate nMOSFET.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 Sheet Resistance of Source and Drain Regions

To obtain an nMOSFET operating at low temperature, the source and drain regions made by implantation of P^+ ions are needed to be sufficiently degenerated and have low resistance. The sheet resistance of implanted Si was measured. The test samples were p-type Si wafers on which 50 keV P^+ ions were implanted with doses of $5x10^{13}$ cm^{-2}, $5x10^{14}$ cm^{-2} and $5x10^{15}$ cm^{-2}, respectively. After implantation

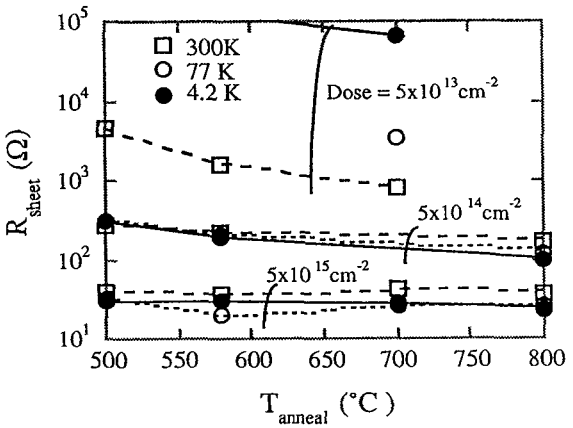


Figure 2: Sheet resistance of P^+ implanted Si. The condition of dose of $5x10^{15}cm^{-2}$ and annealing temperature 800°C is used in the fabrication process.

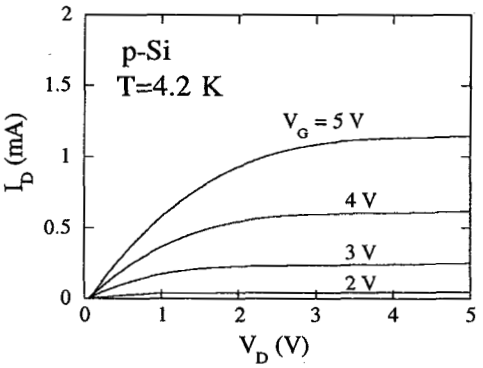
the samples were annealed at different temperatures ranging from 500 to 800°C in dry N_2 for 30 min. The sheet resistance of the samples was measured at room temperature, 77K and 4.2K, respectively, by van der Pauw method [8]. Results are shown in Fig.2. The sheet resistance of the sample under the condition of dose of $5x10^{15}$ cm^{-2} and 800°C annealing temperature, which was used in the process for fabricating the NbN gate nMOSFETs described above, is about 20 Ω even at 4.2K. Therefore, it is concluded the source and drain regions of fabricated nMOSFETs were degenerated.

3.2 Drain V-I Characteristics

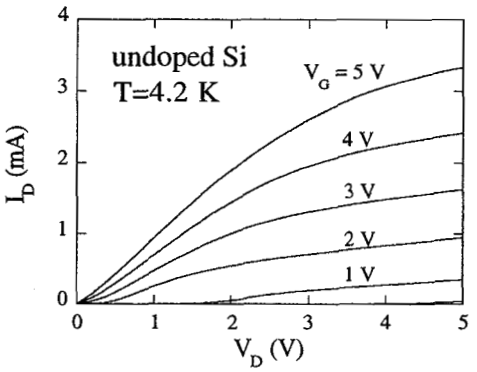
The drain V-I characteristics of fabricated NbN gate nMOSFETs were measured at room temperature, 77K and 4.2K, respectively. Both nMOSFETs fabricated on undoped Si and n-type Si did not work at room temperature and 77K because the FETs were always short through the bulk Si independent of the gate voltage V_G. Typical drain V-I characteristics of each nMOSFET with 10μm gate length at 4.2K are shown in Fig.3. Characteristics of a normal nMOSFET on p-type Si (p-type Si FET) is shown in Fig.3(a). Characteristics of nMOSFETs on undoped Si (undoped Si FET) and n-type Si (n-type Si FET) shown in Fig.3(b) and (c), respectively, demonstrate the proper FET operation at the relatively low drain voltage V_D. In the case of the n-type Si FET, drain current I_D increases even though V_G is under threshold voltage V_{th} as the drain voltage increases in relatively high V_D region. This leakage current is occurs at lower value of V_D when the gate length is shorter. A smaller leakage current is observed in undoped Si FETs at higher V_D than in n-type Si FETs. This leakage current is thought to be due to the impact ionization [9]. Transconductance of the undoped Si FET is higher than that of the p-type Si FET. The difference in transconductance is attributed to the difference in the field effect mobility of undoped Si and p-type Si at 4.2K because of the difference of impurity density in channels.

3.3 Subthreshold Characteristics and Threshold Voltage

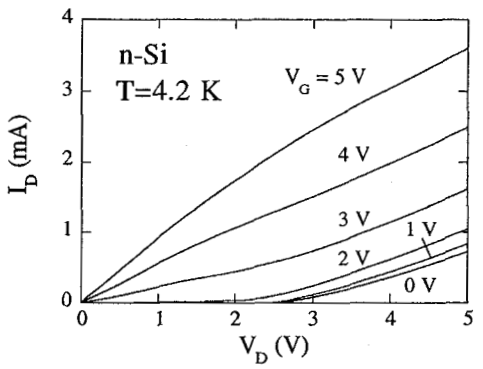
The subthreshold characteristics of fabricated NbN gate nMOSFETs were measured at room temperature, 77K and 4.2K, respectively. Typical subthreshold characteristics measured at the drain voltage 150mV are shown in Fig.4. As the temperature decreases from room temperature to 4.2K, the threshold voltage V_{th} of the p-typed Si FET increases as shown in Fig.4(a). As shown in Fig.4(b) and (c), the undoped Si FET and the n-type Si FET have no threshold voltage at room temperature and 77K because the leak I_D flows at any V_G. But at 4.2K they have the threshold voltage similar to the p-typed Si FET. TABLE I summarizes the threshold voltage at 4.2K of each nMOSFET fabricated in this work. The threshold voltages of NbN gate nMOSFETs on p-type Si, undoped Si and n-type Si are very similar values, from 1.6 to 1.9V in average at 4.2K. This result differs from the expectation derived from the equation of V_{th} for nMOSFET,



(a)

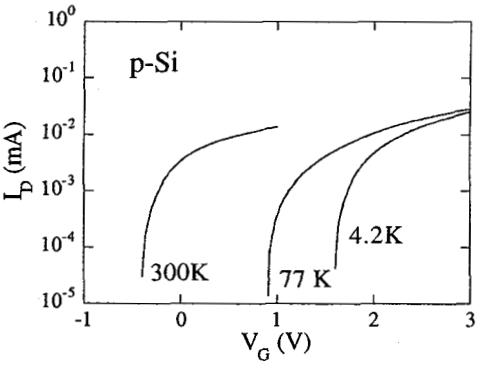


(b)

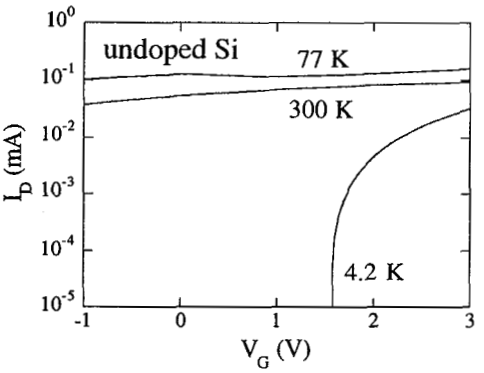


(c)

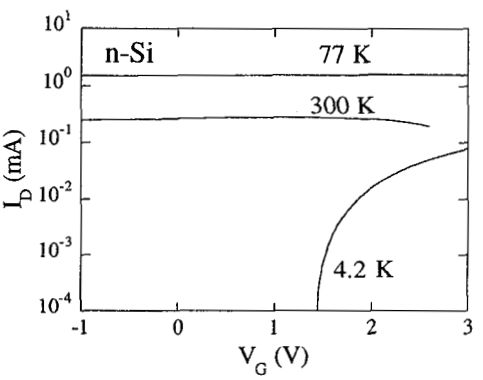
Figure 3: I_D-V_D characteristics of nMOSFETs at 4.2K on (a)p-type Si, (b)undoped Si and (c)n-type Si. L=10μm, W=50μm.



(a)



(b)



(c)

Figure 4: Subthreshold characteristics of nMOSFETs at 300K, 77K and 4.2K, respectively, on (a)p-type Si, (b)undoped Si and (c)n-type Si. L=10μm, W=50μm.

$$V_{th}=V_{FB}+2\phi_F+\frac{\sqrt{2\varepsilon_S\varepsilon_0 qN_A(2\phi_F)}}{C}$$

where V_{FB} is the flat-band voltage, ϕ_F is the Fermi potential, ε_S is the relative dielectric constant of Si, ε_0 is the permittivity of free space, q is the electronic charge, N_A is the concentration of acceptors, and C is the capacitance of MOS. At very low temperature ϕ_F of p-type Si and n-type Si are approximately $qE_G/2$ and $-qE_G/2$, respectively, where E_G is the band gap energy of Si. According to the equation, V_{th} of the p-type Si FET is about 1.8V larger than those of the n-type Si FET and undoped Si FET. We assumed that E_G is 1.1V and N_A is $5\times10^{15}cm^{-3}$ on account of the resistivity of the p-type Si. The values of V_{th} obtained from our experiment are scattering in a range of about 1V. V_{FB} changes its value depending on some trapped charges in the gate oxide and the interface. Therefore, improvements of the process for decreasing the charge trapping are needed to investigate and control the value of V_{th} of NbN gate nMOSFET at 4.2K.

Figure 5 shows subthreshold characteristics of a NbN gate and a Nb gate nMOSFET fabricated on p-type Si at 4.2K, respectively. The Nb gate nMOSFET was fabricated with a similar process to the process shown in Fig.1 except that the gate electrode consists of a Nb/NbN double layer and the annealing temperature is 580°C. V_{th} of the Nb gate FET is 0.5V lower than that of the NbN gate FET. We believe the difference in V_{th} between the two FETs is due to the difference in work function between Nb and NbN.

TABLE I: Threshold voltage of fabricated nMOSFETs at 4.2K.

Substrate	Average(V)	Max.(V)	Min.(V)
p-Si	1.6	2.0	1.3
undoped Si	1.9	2.4	1.6
n-Si	1.8	1.9	1.4

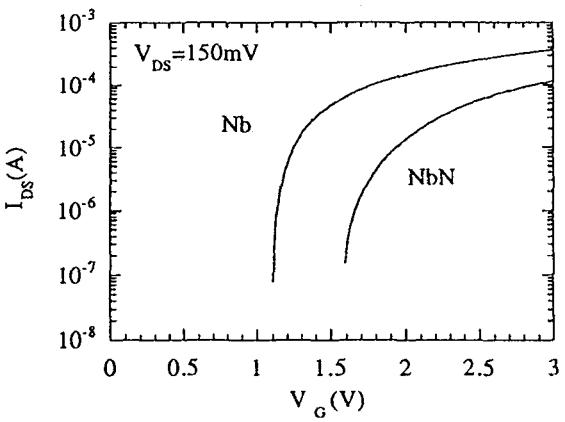


Figure 5: Subthreshold characteristics of Nb gate nMOSFET and NbN gate nMOSFET on p-type Si.

4. SUMMARY

We have proposed and fabricated a high mobility superconductor gate nMOSFET using undoped Si as a channel, which works only at very low temperature. For reference we have also fabricated superconducting NbN gate nMOSFETs on p-type Si and n-type Si substrate, respectively. The nMOSFETs on undoped Si and n-type Si have operated properly at 4.2 K. The transconductance of nMOSFETs on undoped Si substrate is higher than that of nMOSFET on p-type Si. The difference in transconductance is attributed to the difference of impurity density in channels. The observed threshold voltages of NbN gate nMOSFETs on p-type Si, undoped Si and n-type Si are little different from each other at 4.2K. However, this result disagrees with the calculated result from the equations of threshold voltage for nMOSFET. V_{th} of Nb gate nMOSFET is about 0.5 V lower than that of NbN gate nMOSFET at 4.2K.

Acknowledgment

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