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Theoretical and Experimental Study of the Substrate Effect on the Fully Depleted SOI MOSFET at Low Temperatures

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Abstract. In this work is presented a theoretical and experimental analysis of the substrate potential drop and your influence on the fully depleted SOI MOSFET threshold voltage. This study is done at room temperature and at liquid nitrogen temperature. Good agreement was found between the simple model and experimental results.

1. INTRODUCTION

The influence of the underlying substrate on SOI MOSFET operation, i. e. Substrate Effect, has been considered negligible in the classical models that describe the coupling in SOI structure as a function of the voltage applied in the front and back gate.
The first approach in order to develop a simple analytical model for substrate potential drop at room temperature was done by Martino et al.[1], where it was demonstrated that the influence of the substrate in the threshold voltage of the SOI MOSFET cannot be neglected under some circonstances depending on the processing parameters and bias conditions. This simple model was generalized later by Pavanello&Martino[2] for all enhancement mode SOI MOSFET at room temperature. An analytical back-gate bias effect model for ultrathin SOI devices was studied later by Sim&Kuo[3].

2. ANALYTICAL MODEL

For thin film fully depleted SOI MOSFETs the coupling between the front and back surface potential (ϕ_{SF} and ϕ_{SB}, respectively) as a function of the front gate voltage (V_{GF}) and back gate voltage (V_{GB}) is described classically by the Lim&Fossum[4] equations (1) and (2):

$$V_{GF} = \phi_{MS1} - \frac{Q_{ox1}}{C_{oxf}} + \frac{q\,N_{af}\,t_{si}}{2\,C_{oxf}} + \left(\frac{\varepsilon_{Si}}{t_{si}\,C_{oxf}} + 1\right)\phi_{SF} - \frac{\varepsilon_{Si}}{t_{si}\,C_{oxf}}\phi_{SB} \quad (1)$$

$$V_{GB} = \phi_{MS2} - \frac{Q_{ox2}}{C_{oxb}} + \frac{q\,N_{af}\,t_{si}}{2\,C_{oxb}} + \left(\frac{\varepsilon_{Si}}{t_{si}\,C_{oxb}} + 1\right)\phi_{SB} - \frac{\varepsilon_{Si}}{t_{si}\,C_{oxb}}\phi_{SF} \quad (2)$$

where C_{oxf} and C_{oxb} are the front and back oxide capacitance per unit of area respectively; C_{si} is the Silicon film capacitance per unit of area; N_{af} is the Silicon film dopant concentration; Q_{ox1} and Q_{ox2} are the fixed charge density in the 1st and 2nd interfaces; ϕ_{MS1} and ϕ_{MS2} are the front and back work function differences; V_{FB1} and V_{FB2} are the front and back flatband voltages respectively.
In this model the substrate potential drop (ϕ_{SUB}) is neglected.
The determination of the new equation for ϕ_{SUB} is done using the pseudo-MOS structure (Silicon film - Buried Oxide - Silicon Substrate), resulting the Band Diagram presented in figure 1.
As proposed by [2], solving the Band Diagram presented in figure 1 we obtain:

$$\phi_{SB} - V_{GB} = -\phi_{Si_B} + \phi_{Si_F} + V_{oxb} + \phi_{SUB} \quad (3)$$

Solving the equation (3) and assumming the depletion approximation the equation for ϕ_{SUB} is given by(4):

$$\phi_{SUB} = \left[\frac{-\sqrt{2q\, N_{ab}\, \varepsilon_{Si}}}{2C_{oxb}} + \sqrt{\left(\frac{2q\, N_{ab}\, \varepsilon_{Si}}{4C_{oxb}^2} - V_{FB3} \right) + (\phi_{SB} - V_{GB})} \right]^2 \quad (4) \; ; \quad V_{FB3} = \frac{kT}{q} \ln \frac{N_{af}}{N_{ab}} - \frac{Q_{ox3}}{C_{oxb}} \quad (5)$$

where N_{ab} is the Silicon Substrate concentration, Q_{ox3} is the fixed charge density at 3rd interface and V_{FB3} is the flatband voltage for pseudo-MOS structure.

The equation (4) is valid in the interval $0 \leq \phi_{SUB} \leq 2\phi_{Fb}$, where ϕ_{Fb} is the Fermi potential of the underlying substrate. With this interval it is possible to determine the extremes for V_{GB}.

Thus, if $V_{GB} \leq V_{GBmin}$ the 3rd interface will be in inversion ($\phi_{SUB} = 2\phi_{Fb}$) and the maximum influence of the substrate is observed. Otherwise, if $V_{GB} \geq V_{GBmax}$ the 3rd interface will be in accumulation ($\phi_{SUB} = 0$) and there are no influences of the substrate on SOI MOSFET.

To link the equation (4) with the equations (1) and (2) is necessary to add the term ($-\phi_{SUB}$) in equation (2), resulting:

$$V_{GB} = V_{FB2} + \frac{q\, N_{af}\, t_{si}}{2\, C_{oxb}} + \left(\frac{\varepsilon_{Si}}{t_{si}\, C_{oxb}} + 1 \right) \phi_{SB} - \frac{\varepsilon_{Si}}{t_{si}\, C_{oxb}} \phi_{SF} - \phi_{SUB} \quad (6)$$

In order to estimate ϕ_{SUB} at 77K, the change in the bandgap (Eg), the new values for Fermi potential and the reduction of the effective doping level due to the impurity freeze-out must be accounted in the equations (1), (4) and (6) using the Selberherr's[5] equations.

3. NUMERICAL SIMULATION

The validation of this new model at room temperature and at 77K was performed by numerical bidimensional simulation with MEDICI[6] for a SOI nMOSFET with p-type substrate.

The parameters used in the simulations are:

$N_{af}=8x10^{16}$ cm^{-3} ; $N_{ab}=1x10^{15}$ cm^{-3} ; t_{oxf} =20 nm ; t_{oxb}=400 nm ; t_{Si}=50 nm ; $Q_{ox1}/q=5x10^{10}$ cm^{-2} ; $Q_{ox2}/q=Q_{ox3}/q=1x10^{11}$ cm^{-2} .

The results of the comparison with the simulation and the solution of the equations system (1), (4) and (6) at room temperature and at 77K are shown in figure 2, where it is possible to observe a good agreement between the numerical simulation and the analytical model.

The analysis of the substrate effect on the threshold voltage[7] at room temperature and at 77K are presented in figures 3A and 3B respectively, where the results obtained solving the simple analytical model equations are compared with MEDICI numerical simulation using structures with and without substrate. The resultant ΔVth_F, i. e. the difference between the threshold voltage considering or not the substrate effect is shown.

As observed in figures 3A and 3B, the maximum threshold shift occurs when the 3rd interface is in inversion and increases when the temperature decreases because ϕ_{SUB} becomes higher due to the increase of the Fermi potential.

Using the simple model is possible to study the substrate effect as a function of process parameters variation. As demonstrated by [7] the most important parameter affecting the threshold voltage is the buried oxide thickness which is shown in figure 4. This parameter also influences the subthreshold slope[8].

In figure 4 can be seen that the maximum ΔVth_F increases drastically when the buried oxide thickness increases and temperature decreases. In the example, for t_{oxb}=80 nm the maximum ΔVth_F changes from 90mV to 230 mV when the temperature changes from 300K to 77K.

4. EXPERIMENTAL RESULTS

Devices were fabricated using 0.5μm SOI CMOS technology in SIMOX wafers with the characteristics below:

$N_{af}=1x10^{17}$ cm^{-3} ; $N_{ab}=1x10^{15}$ cm^{-3} ; t_{oxf} =15 nm ; t_{oxb}=390 nm ; t_{Si}=85 nm .

The experimental characterization of the substrate effect was done using a SOI nMOSFET with L=2μm and W=20μm. Only long channel devices were measured in order to avoid short channel effects which would cause problems in the observation of the shift in the threshold voltage. The threshold voltage was obtained experimentally and by simulation using the current level criteria $I_D=10^{-7}$ W/L in curve I_{DS} *vs* V_{GS}.
The experimental I_{DS} *vs* V_{GS} curves were obtained using the parameter analyzer HP4145B. The bias applied in the devices are V_{DS}=0.1V, V_{GF} from -0.5V to 1.5V step 5mV and V_{GB} from -1.5V to 3.5V step 100mV at room temperature and V_{GF} from -0.5V to 1.5V step 5mV and V_{GB} from -2.5V to 3.5V step 100mV at 77K.
The results of the electrical characterization are shown in the figure 5, where it is plotted the curve Vth_F as a function of V_{GB} obtained at room temperature and at 77K respectively. In these figures are also plotted the results obtained analytically solving the model equations considering or not the substrate.
As can be seen in figure 5, an excellent agreement was found between the results obtained experimentally and by the solution of analytical model equations at room temperatute and at 77 K. In both cases the substrate effect on threshold voltage can be identified and the maximum substrate influence occur when the 3rd interface is in inversion, confirming the theoretical and simulation study.
In the showed curves, when the temperature decreases from 300 K to 77 K the maximum ΔVth_F increases from 28 mV to 48 mV becomming significant.

5. CONCLUSION

In this work was presented a simple analytical model for account the potencial drop in the substrate and determine your influence on threshold voltage.
As experimentally demonstrated, the substrate effect on the threshold voltage occurs at room and at liquid nitrogen temperature and cannot be neglected at some process parameters conditions. Mainly at low temperatures the substrate effect becomes higher due to the increase of the Fermi potential. The comparison between the experimental results and modeled results was showed and an excellent agreement was found.
Indeed, the simple analytical model developed is sufficiently powerful for describe the substrate effect on the threshold voltage and should be included in the analytical device simulators, as SPICE for example, to improve the agreement between the experimental and simulated results .

Acknowledgment

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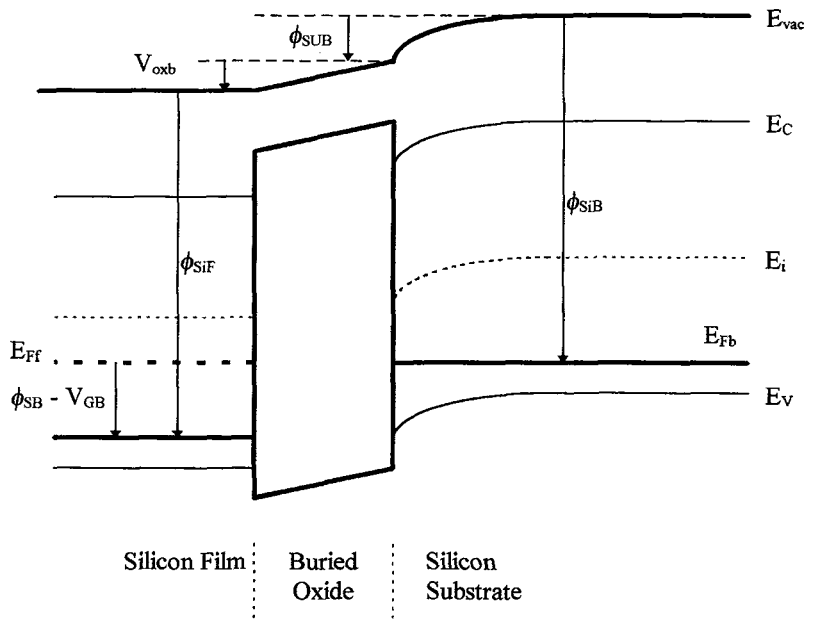

figure 1 - Band Diagram for pseudo-MOS structure

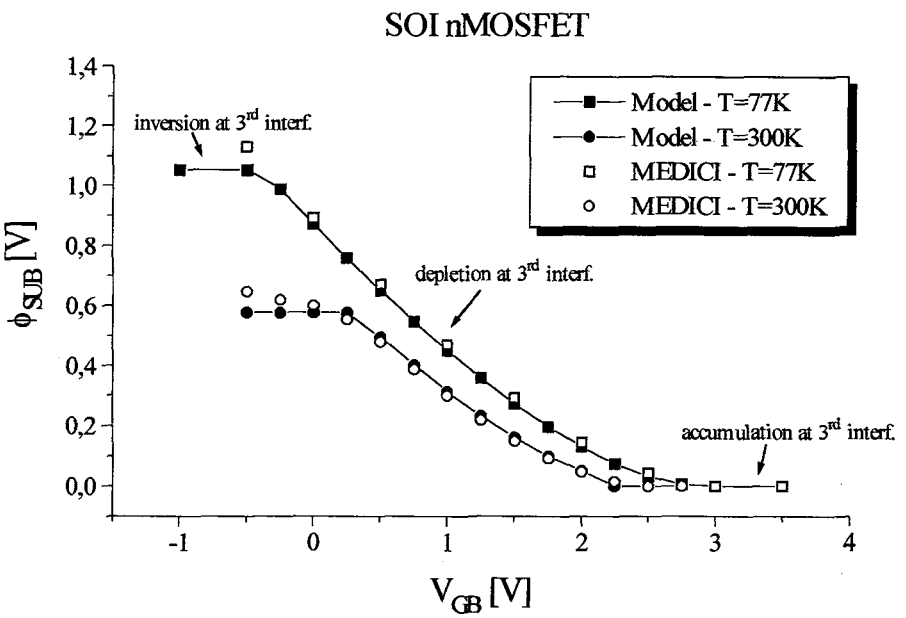

figure 2 - Comparison between analytical model and MEDICI simulation at room temperature and at 77 K.

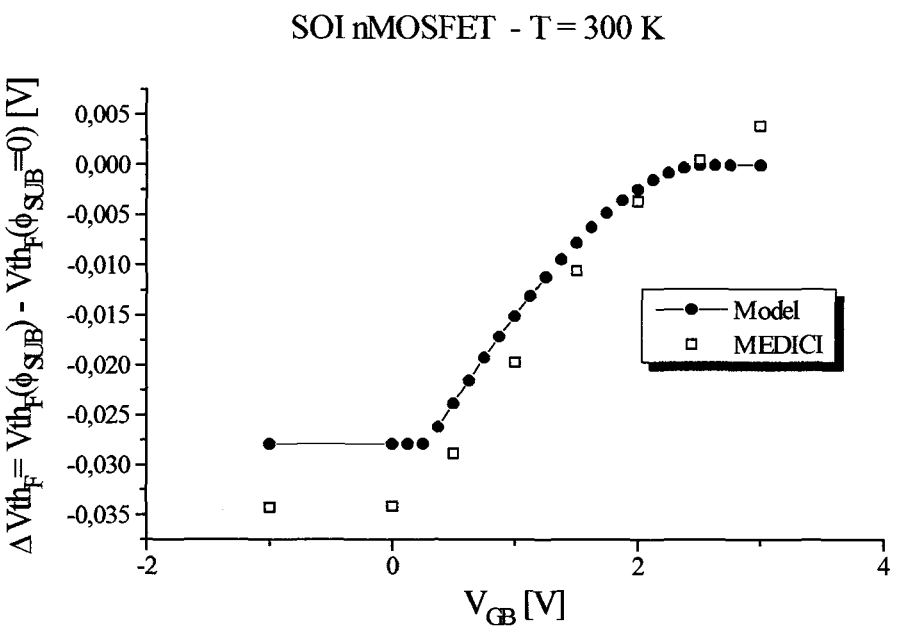

figure 3A - Influence of the substrate on the threshold voltage at room temperature

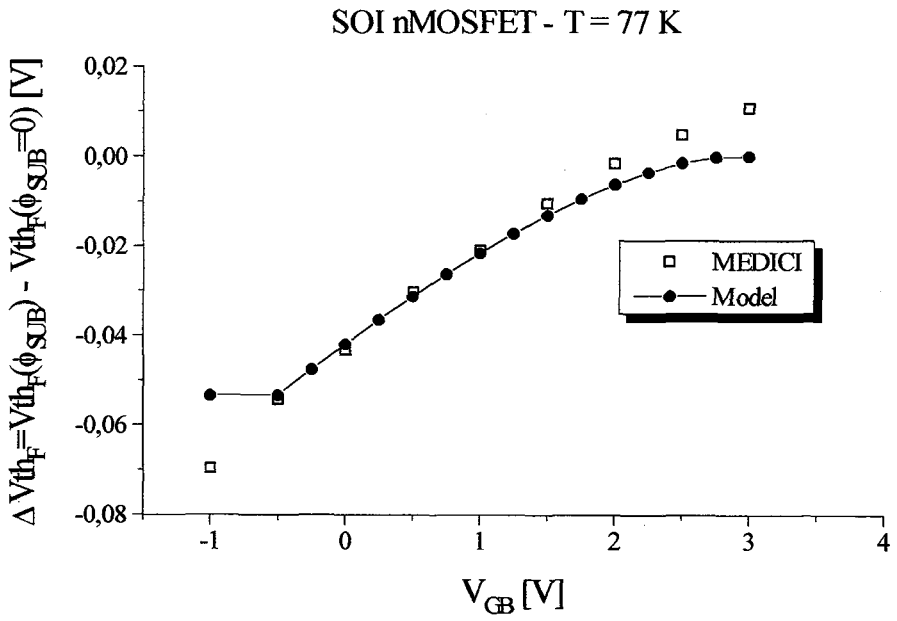

figure 3B - Influence of the substrate on the threshold voltage at 77K

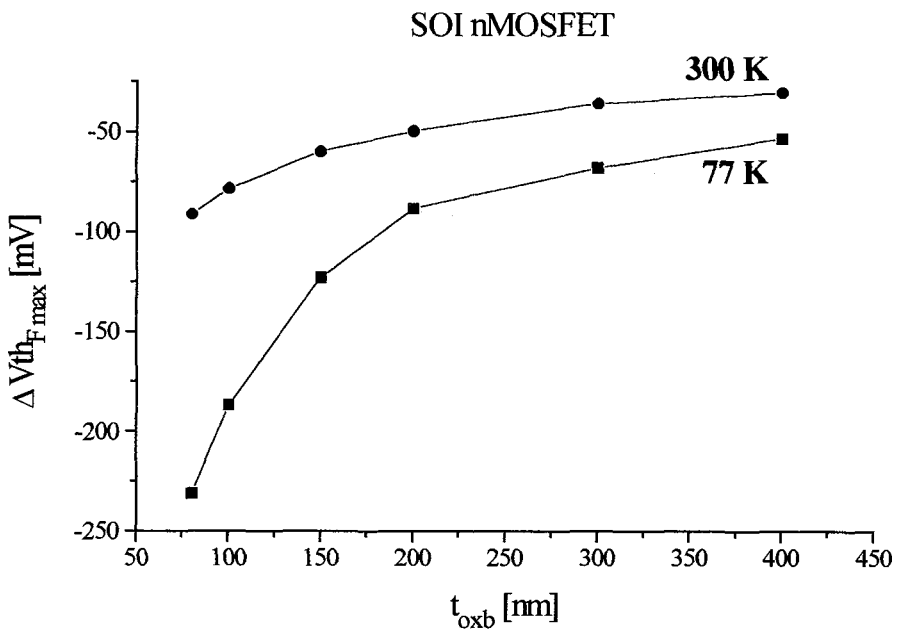

figure 4 - Maximum ΔVth_F as a function of buried oxide thickness decrement

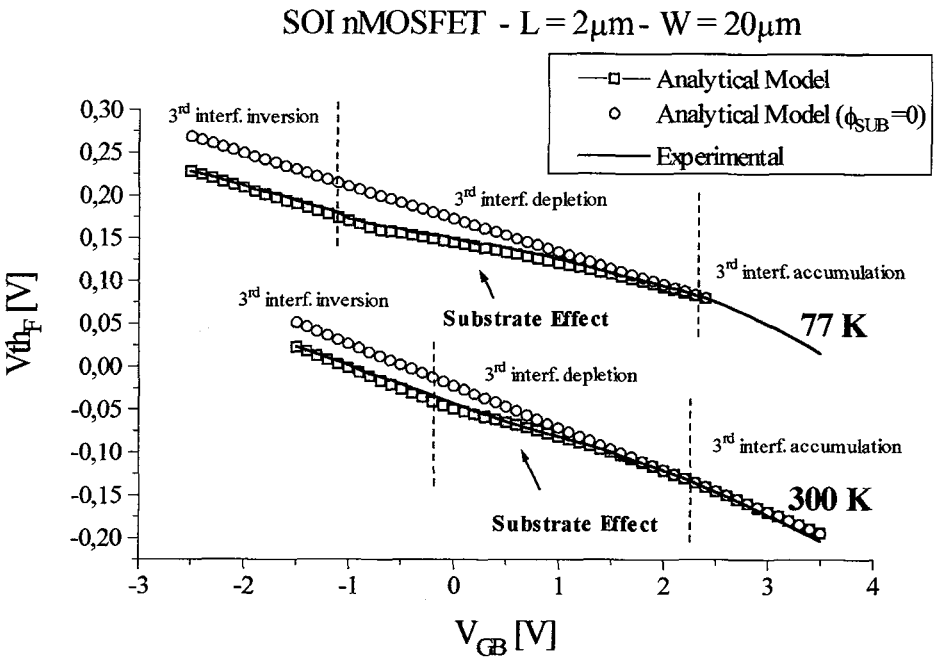

figure 5 - Comparison between modeled and experimental results for a SOI nMOSFET