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Abstract. In this paper, an overview is given of the methods for practical parameter extraction for MOSFETs operated at cryogenic temperatures. The methods considered are based on the input characteristics of the device, from which the charge threshold voltage, the subthreshold slope, the effective mobility, the series resistance and the effective gate length is derived. Whenever possible, the physical basis of the mostly semi-empirical methods will be outlined. Finally, pitfalls and problems, related to low temperature MOSFET characterisation, like transient and freeze-out effects, self-heating, etc, are briefly discussed.

1. INTRODUCTION

Today, MOSFET simulation and modelling has left its infancy and has reached a level whereby high agreement is reached with experimental characteristics. At the same time, by building in temperature dependent physical models, it is possible to predict the low temperature operation in an accurate way [1]-[4]. In principle, one could thus restrict the actual low-temperature device characterisation to the absolute minimum and rely on numerical parameter calculations. In practice, however, the situation is more complex. For instance, for MOSFETs operating in the freeze-out regime, which typically occurs below 50 K or so, some new physical phenomena start to play a role, which are generally less well understood and require a detailed study of the underlying mechanisms (for a recent overview see e.g. [5]). Furthermore, upon down-scaling the device dimensions to the submicron and the nanoscale, the device parasitics become prominent and start to affect the I-V characteristics. This is the more true for low temperature operation, which can increase the mobility degradation and the series resistance [5]. At the same time, high transverse and high lateral field effects become important [6] and carrier velocity saturation starts to limit the drive current [7]-[8]. At cryogenic temperatures and/or for sub 100 nm devices, even velocity overshoot has been demonstrated experimentally [9]-[11]. So from a practical and a more fundamental viewpoint there is still a need for detailed MOSFET studies at cryogenic temperatures and hence for parameter extraction methods, in order to unravel the temperature dependence of physically relevant properties like the charge threshold voltage V_T, the subthreshold swing S, the effective mobility (μ_{eff}), the source-drain series resistance R_{SD} and the effective device length L_{eff}.

In the next sections, the low-temperature extraction of the parameters listed above will be discussed separately. As will be seen, most methods rely on an input curve (I_D versus V_{GS}) registered in linear operation, i.e. for low drain voltage V_{DS}. It will become clear that traditional room temperature parameter extraction may no longer work at low T and therefore, dedicated and more sophisticated techniques have been developed, which require, however, a good insight into the underlying physics. In the final paragraph, some experimental difficulties which are typical for low temperature operation will be highlighted and their relevance discussed. Additionally, practical ways to circumvent these anomalies will be pointed out.

2. CHARGE THRESHOLD VOLTAGE EXTRACTION

A number of fairly simple, semi-empirical methods have been proposed to derive the threshold voltage V_T, some of which have become quite popular. The most widespread is probably the linear extrapolation method, which is illustrated in Fig. 1, whereby a straight line is fitted to the linear drain current I_D measured at low V_{DS} (typically 50 mV) to the point of maximum transconductance g_m. V_T is then defined as the gate voltage corresponding to the crossing point minus $V_{DS}/2$. This technique has been successfully applied to low temperature operation as well [12]-[15], although the corresponding value V_{Text} is larger than the true V_T at cryogenic T [14].

Another straightforward method is to determine the gate voltage which is necessary to establish a certain drain current level per unit of width (I_D/W) at V_{DS}=50 mV. Although very simple, this method has only limited applicability and is for instance useless for so-called accumulation-mode (AM) Silicon-on-Insulator (SOI) transistors [15], which can operate in different conduction modes, both at room [16] and at cryogenic T [17].

The Fowler and Hartstein (FH) method [18] determines the point of maximum slope in the transconductance (g_m) characteristic and linearly extrapolates this point to zero transconductance (Fig. 2). Another technique, introduced by Balestra and Ghibaudo [14] is well-suited for cryogenic MOSFETs and will be discussed in the next section, since it is related to the extraction of the effective mobility.

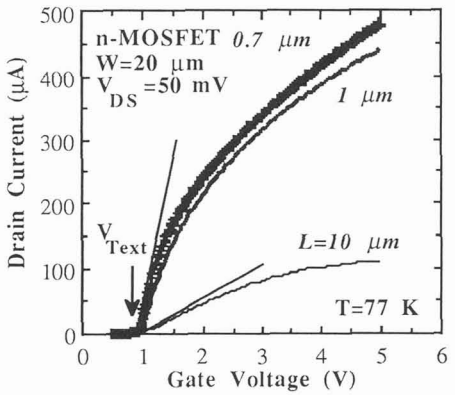

Fig. 1. Definition of the extrapolated threshold voltage, for three n-MOSFETs at 77 K.

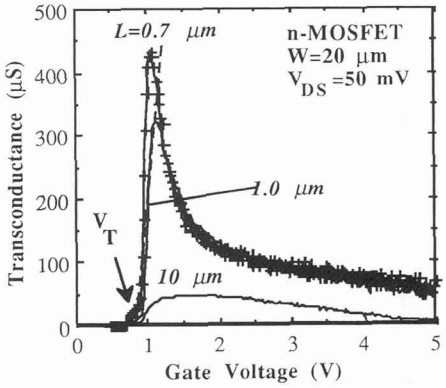

Fig. 2. Fowler-Hartstein method for the n-MOSFETs of Fig. 1.

Probably the most powerful (and fairly simple) method for V_T extraction is the so-called Transconductance peak [19],[20] (TC) or double-derivative method [21]. It is illustrated in Fig. 3 for three bulk n-MOSFETs at 77 K: V_T is defined here as the gate voltage corresponding to the peak maximum in the $\partial g_m/\partial V_{GS}$ curve. From a comparison of different techniques, it can be concluded that the TC method is closest to the 'correct' physical V_T, which can be determined by the so-called 'split' C-V method [19],[20]. Furthermore, it is rather insensitive to interface states, normal field mobility degradation [19],[20] and series resistance [19],[20],[22] which are highly desirable features for low-temperature extraction. Fig. 4 compares the extrapolated with the TC threshold voltage for three 0.7 μm bulk CMOS n-MOSFETs at 77 K, as a function of the device length. No systematic difference is found in this particular case.

Another benefit of the TC method is that it enables to determine the onset of other conduction modes. For instance, in the case of the AM SOI p-MOSFETs, it has been demonstrated that for each mode (back-channel; body; front-channel) a corresponding peak in the $\partial g_m/\partial V_{GS}$ is obtained, and this both at room temperature [21] and at low T [15]. The same applies for e.g. parasitic edge conductance, as illustrated in Fig. 3, where the first small peak for the L=0.7 μm n-MOSFET corresponds to premature conduction along the LOCOS field regions. Similar observations have been reported for irradiated SOI MOSFETs at low T [22], or for the edge-conduction in dual-gate SOI MOSFETs [23]. A final example of the power of the technique is given in Fig. 5, showing the V_T as a function of temperature for a 0.5 μmx20 μm SOI n-MOSFET, both fully depleted (FD) and partially depleted (PD). In general, a better agreement between the theoretically expected value and the measured data is obtained for the TC technique. Futhermore, for the

case that the back-interface of the FD device is in inversion, only this method yields an acceptable V_T [15].

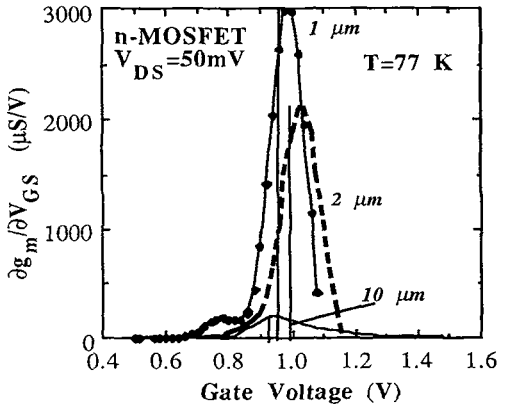

Fig. 3. TC threshold voltage for three n-MOSFETs at 77 K. The first maximum for the L=0.7 μm transistor corresponds to the onset of parasitic edge conduction, which is not seen at room temperature.

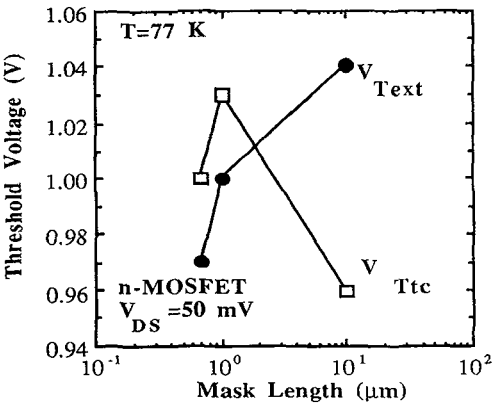

Fig. 4. Extracted threshold voltage as a function of device length, corresponding to T=77 K, for the n-MOSFETs of Fig. 1.

A phenomenon which has been frequently observed in the past for cooled room temperature CMOS technologies which were not optimised for cryogenic operation is the so-called drain-voltage threshold [24]. This occurs typically for deep cryogenic temperatures, where freeze-out becomes important and indicates an insufficient overlap of the gate with the source. As a result, there exists a potential barrier, which inhibits the injection of carriers in the channel. This type of behaviour aggravates for cooled submicron CMOS transistors with Lowly Doped Drain (LDD) regions [25]. Careful analysis of the phenomenon has pointed out that this drain threshold voltage phenomenon is connected to the negative ΔL often observed at low T and pointing to a loss of control of the gate electrode over the channel [26].

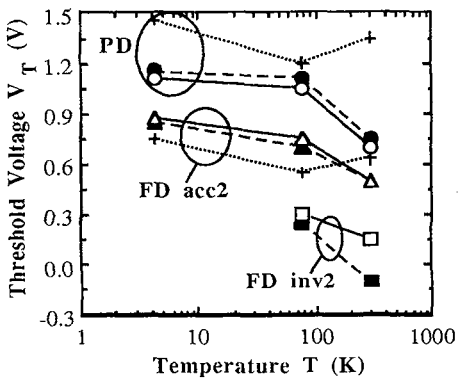

Fig. 5. Threshold voltage as a function of T for a PD and a FD 0.5 μmx20 μm SOI n-MOSFET. Full lines represent theoretical estimates; dashed lines TC extracted data and dotted lines extrapolated V_Ts. FD acc2 corresponds to the case with the back-gate in accumulation; FD inv2 to the case with the back-gate inverted [15].

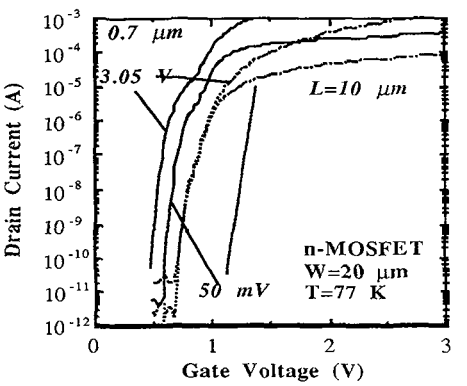

Fig. 6. DIBL effect at 77 K for a L=0.7 and 10 μm nMOSFET fabricated in a 0.7 μm CMOS technology: no effect is seen for the longer device at V_{DS}=3.05 V, while a shift of the input curve to the left is found for the 0.7 μm device.

For submicron MOSFETs several kinds of short-channel effects can reduce the threshold voltage. One such mechanism is Drain Induced Barrier Lowering (DIBL), which is illustrated in Fig. 6 for bulk 0.7 μm CMOS n-channel transistors. Only the shortest device suffers clearly from the DIBL effect. However, as demonstrated previously, low-temperature DIBL occurs already for long transistors (L=10 μm) in the case of a 3 μm CMOS technology on high-resistivity (HR) substrates [27]. In general, it is found that the

reduction of the threshold voltage, occurring for larger lateral fields (larger V_{DS}) diminishes upon cooling to 77 K, both for n-MOSFETs [28],[29] and p-MOSFETs [30],[31].

3. SUBTHRESHOLD SWING

The subthreshold swing, shown in Fig. 7 is defined as the inverse subthreshold slope and corresponds to:

$$S = \frac{\partial V_{GS}}{\partial \log I_D} \qquad \text{(mV/decade current)} \qquad (1)$$

for the device in linear operation. For standard MOSFETs this parameter is tightly connected to the interface and the fixed oxide charge through the equation:

$$S^{-1} \approx \frac{q}{kT} \frac{C_{ox}}{C_{ox} + C_d + C_{it}} \qquad (2)$$

where C_{ox} is the gate oxide capacitance per cm^2, C_d the depletion capacitance and $C_{it}=q^2N_{it}$ the interface state capacitance per unit of area, respectively, with N_{it} the surface density of interface traps ($/eVcm^2$) and kT/q the thermal voltage. Early studies indicated that the subthreshold swing at 4.2 K was higher than expected from eq. (2). In fact, no unique value for S could be extracted [32]. It has been recently demonstrated that eq. (2) is still valid in good approximation and that the observed variation of S with I_D at 4.2 K is due to the variation of N_{it} when approaching the band edge [33]. This is supported by the density of interface traps extracted from the dynamic conductance technique, which is in close agreement. The subthreshold swing has also been applied to analyse the density of interface traps in MOSFETs irradiated at 77 K [34].

In some cases, discrete steps or peaks are observed in the weak inversion drain-current of both bulk [35] and SOI MOSFETs [36] at 4.2 K. This is even more pronounced for devices which have been hot-carrier stressed either at room temperature or at cryogenic T [35],[37], or for small area devices. The physical explanation of this phenomenon is most likely interface-trap assisted resonant tunneling in the ≈0.1 μm degraded region near the drain of the device, although other models are currently being explored. In principle, such observations allow to study single interface traps, occurring close to the band-edges.

For thin-film fully-depleted, or AM SOI MOSFETs coupling between the front and the back interface will affect the subthreshold slope. For the back-gate in depletion, 1/S will reduce and depends on both the front- and the back-gate bias [38]. Consequently, eq. (2) is no longer a good approximation and can therefore not be used to extract N_{it}. Generally, S becomes a rather complex function for FD or AM SOI MOSFETs, but in some cases, a simplification is possible [39]. It has for instance been demonstrated that for AM MOSFETs the minimum S can be approximated by [39]:

$$S_{min} \approx \frac{kT}{q} \ln(10) \left[\left(1 + \frac{C_{itf}}{C_{oxf}} + \frac{C_{si}}{C_{oxf}}\right) - \frac{\frac{C_{si}}{C_{oxb}} \frac{C_{si}}{C_{oxf}}}{1 + \frac{C_{itb}}{C_{oxb}} \frac{C_{si}}{C_{oxb}}} \right] \qquad (3)$$

with C_{itf} and C_{itb} the front and back interface trap capacitance, respectively; C_{oxf} and C_{oxb} the corresponding front and back gate capacitance and C_{si} the Si film capacitance per cm^2, given by $\varepsilon_{si}\varepsilon_0/t_{si}$ (ε_{si} the dielectric constant of Si; ε_0 the permittivity of vacuum and t_{si} the thickness of the Si film). At the same time, it has been demonstrated that for negligible N_{itf} at 300 K, the front interface trap density at 77 K can be extracted from the increase in flatband voltage (or for an AM device, in V_T) upon cooling [40], yielding the expression:

$$N_{itf}(77\ K) \approx \frac{C_{oxf}}{q} \frac{\Delta V_T}{q\Phi_{f77K}} \qquad (4)$$

with ΔV_T the absolute value of the front threshold voltage increase, which is derived from the TC method as outlined above and Φ_{f77K} is the calculated Fermi level potential with respect of the intrinsic level [40]. Using eq. (4), typical N_{itf}s in the range $2x10^{11}$ $eV^{-1}cm^{-2}$ have been derived at 77 K for the AM p-MOSFETs shown in Fig. 8. Combining eqs. (3) and (4) and substituting the experimental S, the back interface trap density at 77 K can be extracted as well [41]. Typical values for N_{itb} are in the range 10^{12} $eV^{-1}cm^{-2}$. These should be considered as effective values for the respective interface trap densities. This analysis can be extended to any cryogenic temperature, provided that the threshold voltage difference with the room temperature value is sufficiently large to be accurately determined.

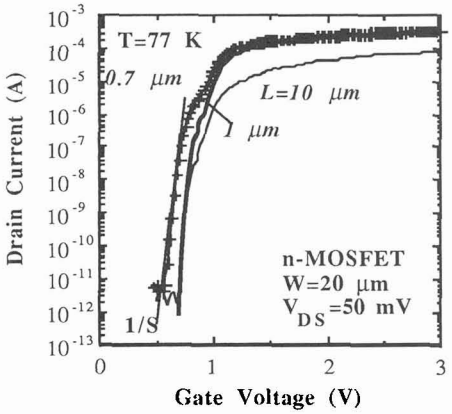

Fig. 7. Definition of the subthreshold swing for three n-MOSFETs at 77 K, with different mask length L.

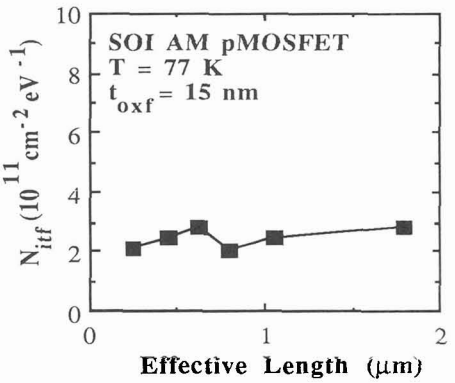

Fig. 8. Effective front interface trap density derived at 77 K for an array of 0.5 μm CMOS AM SOI p-MOSFETs. N_{itf}(300 K) is taken 0 in the calculation [40]. The device width is 20 μm.

4. MOBILITY

4.1 Effective mobility at moderate transverse electric field

The extraction and physical modelling of the inversion layer mobility has attracted a lot of attention in the past two decades, both at room temperature [42] and at cryogenic T [43]-[51]. At room temperature, the effective mobility μ_{eff}, which is defined as:

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}} \frac{g_d(V_{GS})}{qN_S(V_{GS})} \approx \frac{L_{eff}}{W_{eff}} \frac{I_D}{C_{ox}(V_{GS}-V_T)V_{DS}} \tag{5}$$

takes the form:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta^* (V_{GS}-V_T)} \tag{6}$$

in strong inversion. Hereby is g_d the channel conductance ($\partial I_D/\partial V_{DS}$), N_S the inversion layer carrier surface density and μ_0 is the zero-field mobility. The generalised mobility attenuation factor θ^* is given by [52]:

$$\theta^* = \theta + \frac{C_{ox} R_{SD} W_{eff} \mu_0}{L_{eff}} \tag{7}$$

and is a measure of the reduction of the effective mobility with increasing normal field. The latter is physically due to the increasing contribution of surface roughness scattering to the carrier mobility. In writing eqs. (6) and (7) it is assumed that the source-drain series resistance is constant with $V_{GS}-V_T$ (non-LDD type of MOSFETs) and that the gate overdrive voltage $V_{GS}-V_T >> I_D R_{SD}/2$.

As pointed out earlier [53]-[54], the extraction of μ_{eff} from a linear input curve at cryogenic temperatures requires in fact already an accurate modelling of the device characteristics, in case of the μ_{eff} dependence on the normal field, on T, etc. This implies that most of the extraction methods which have been proposed recently [55]-[57] are rather complex and require numerical treatment of the measurement data. In many cases, they are applicable only in a restricted temperature regime (generally from 77 K on), or to a particular class of devices. An attractive empirical method, applicable in the whole range between 4.2 K and 300 K has been proposed by Emrani et al. [53]-[54] and has been succesfully applied for the extraction of the electron mobility in inversion and accumulation layers [58], to SOI MOSFETs [59] and to n- and p-MOSFETs with nitrided oxide gates [60]. The principle of the extraction method is based on the empirical relationship between the function I_D^2/g_m and the gate overdrive voltage $V_{GS}-V_T$. For instance, as shown in Fig. 9 for bulk n-MOSFETs at 77 K and in Fig. 10 for PD SOI n-MOSFETs at 77 K, for sufficiently large $V_{GS}-V_T$, the following applies:

$$\frac{I_D^2}{g_m} = \beta (V_{GS}-V_T)^n \tag{8}$$

whereby the coefficient β depends on θ^*. Physically acceptable values for the empirical exponent n are in the range 2 (300 K) to 3 (4.2 K) [61]. The effective mobility is shown to be [53]:

$$\mu_{eff} = \mu_g \frac{X^{n-2}}{1 + X^{n-1}} \tag{9a}$$

with $X=\theta(V_{GS}-V_T)$ and μ_g proportional to the maximum effective mobility through the relationship:

$$\mu_{max} = \mu_g \frac{(n-2)^{(n-2)/(n-1)}}{(n-1)} \tag{9b}$$

At the same time, the charge threshold voltage V_T at any temperature in the range 4.2 to 300 K can be derived from:

$$V^*_{Text} = V_T + \frac{1}{\theta^*}\left[\frac{(n-2)}{n}\right]^{n/(n-1)} \tag{10}$$

whereby θ^* is obtained from:

$$\theta^* = \left(\frac{n-2}{n}\right)^{1/(n-1)} \frac{1}{V_{GSmax}-V_T} \tag{11}$$

V_{GSmax} is the gate voltage which corresponds to the maximum transconductance g_{mmax}. Since θ^* is a positive number and n becomes larger than 2 upon cooling, from eqs (10) and (11) follows that the linear extrapolated threshold voltage V_{Text} is slightly larger than the actual V_T at low T. In practice, it turns out that the exponent n starts to increase in the range between roughly 100 K and 200 K for n-channel devices, depending on the technology, while for p-MOSFETs, the change from 2 to 3 occurs between 20 K and 4.2 K. Physically speaking, the change of n from 2 to 3 points to a change in the dominant scattering mechanism upon cooling. Likewise, the bell-shaped μ_{eff} behaviour typically found at low T can be explained by assuming that μ_{eff} is an explicit function of the inversion charge Q_i, which in its most general form is represented by [54]:

$$\frac{1}{\mu_{eff}} = \frac{A}{Q_i^{n-2}} + BQ_i \tag{12}$$

whereby the coefficient A is a Coulomb scattering parameter and B a surface roughness scattering parameter.

Although this method is quite general and powerful, there exists a number of limitations which are for example illustrated in Fig. 9. The curves are obtained on bulk CMOS transistors with LDD. While for the L=10 μm device an n≈2.5 is obtained, n reduces to ≈2 (L=1 μm) and to physically unrealistic values for smaller lengths (1.7 for L=0.7 μm). This implies that the technique is not applicable to short-channel LDD devices at low T, probably because of the series resistance. Of course, it has been demonstrated that the function represented by eq. (8) is independent of R_{SD} and therefore also the determination of n and V_T [53],[61], which is, however, only valid if R_{SD} is indeed independent of $V_{GS}-V_T$. This fact has to be taken into account if the above extraction method is to be used for short-channel LDD MOSFETs.

As illustrated by Figs 11 and 12, the same analysis can in principle be applied to the case of p-MOSFETs fabricated on high-resistivity Si substrates (HR-CMOS) [27]. From the transconductance characteristics shown in Fig. 11, it is clear that at cryogenic temperatures this corresponds to a bell-shaped μ_{eff}. However, again only physical reasonable values of n are obtained in a limited range (n=2.08 for T=77 K), while n's lower than 2 are found for the other temperatures [27].

Another important point related to the mobility extraction at cryogenic T is the so-called universal electric field dependence of the effective mobility previously reported at room temperature for n- [62] and p-channel devices [63]. It turns out that if μ_{eff} is represented versus the effective normal electric field, given by:

$$E_{eff} = \frac{\eta Q_i + Q_d}{\varepsilon_{si}\varepsilon_0} \tag{13}$$

a universal curve is obtained, which is independent of substrate doping density, or substrate bias. Hereby is the empirical factor η=1/2 for electrons and 1/3 for holes. The resulting effective mobility then reads:

$$\mu_{eff} = \frac{\mu_{00}}{1 + E_{eff}/E_c} \qquad (14)$$

with μ_{00} the zero field maximum mobility and E_c is a critical electric field.

Early low-temperature studies revealed already that the parameter η is not a constant with T [46],[50],[51], but lies somewhere between 1/3 and 1, which points towards a change in dominant scattering mechanism upon cooling. More recently, detailed studies have been reported on the substrate and doping density dependence of the low temperature μ_{eff} [64]-[66], both for n- and for p-channel devices. Emrani et al. conclude from these studies that the universal field dependence approach represented by eqs. (13) and (14) has no physical meaning at cryogenic T and should therefore not be used [54],[64]. The same conclusion followed from the effect of Fowler-Nordheim carrier injection on the low temperature μ_{eff} [54],[65].

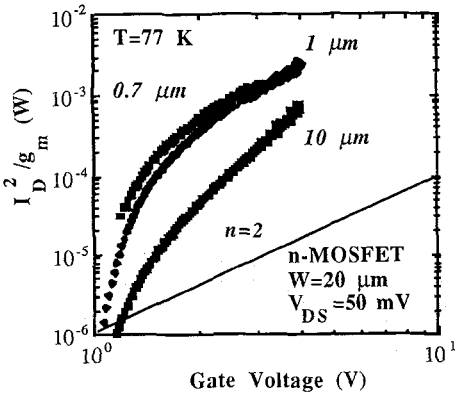

Fig. 9. Function defined by eq. (8) for an array of 0.7 μm CMOS n-MOSFETs at 77 K. A reference line proportional to V_{GS}^2 is drawn as a guide.

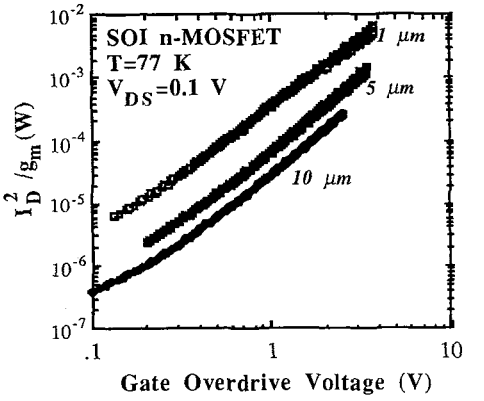

Fig. 10. Function defined by eq. (8) for an array of 1 μm CMOS PD SOI n-MOSFETs at 77 K. The corresponding exponents are : n=2.33±0.1 (L=10 μm); n=2.33±0.1 (L=5 μm) and n=2.1±0.1 (L=1 μm).

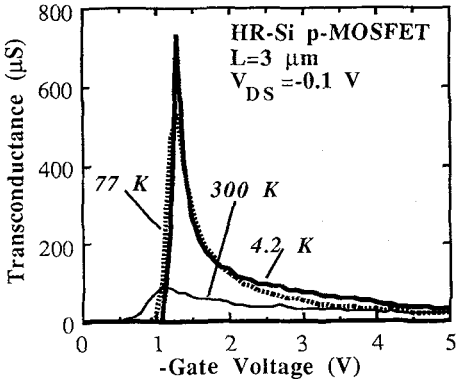

Fig. 11. Transconductance for an edgeless 58 μmx3 μm HR-Si p-MOSFET at 300 K (full line); 77 K (dotted line) and 4.2 K (bold line) [27].

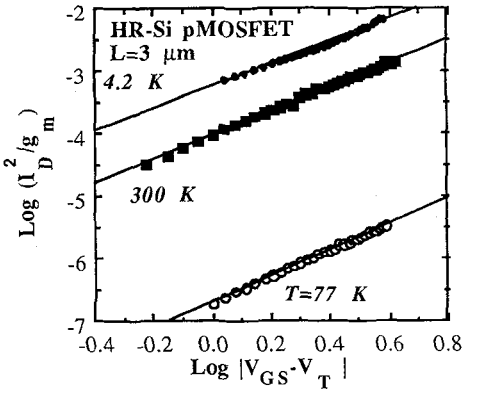

Fig. 12. Corresponding function (8) versus the gate overdrive voltage. n=1.92 (300 K); 1.78 (4.2 K) and 2.08 (77 K).

4.2 Effective mobility at high transverse electric field

Already in the mid sixties, it was found that the transconductance at large gate overdrive voltages (i.e. large normal fields) can become negative at 77 K [67]. This has more recently been confirmed for both n- and p-channel devices [68]-[70] and for MOSFETs with nitrided oxides [71]-[72]. It turns out that the critical field for zero g_m is in the range 2.2-2.6 MV/cm for n-MOSFETs at 77 K and increases up to 7 to 8 MV/cm

for p-MOSFETs, depending on e.g. the gate oxide thickness [68]. In physical terms, this means that at low T, a change in scattering mechanism occurs at high normal fields. Empirically, this is modelled by introducing a second attenuation factor θ_2, as follows [68]-[70]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta\,(V_{GS}-V_T) + \theta_2\,(V_{GS}-V_T)^2} \tag{15}$$

The extraction of this second attenuation factor at low temperatures is in detailed discussed in [69]. Globally speaking, the effective mobility behaviour with T can be represented schematically by Fig. 13 [49],[65]. At 300 K, the inversion layer mobility is dominated by phonon scattering for low effective fields and by surface roughness scattering at high fields. At 77 K and 4.2 K, Coulomb scattering dominates the phonon scattering at low fields, while a much stronger E_{eff} dependence is observed at higher fields than at 300 K. Detailed expressions can be found in the cited literature for the different scattering mechanisms, but are out of the scope of this paper. It should finally be noted that for high effective fields around 1 MV/cm nitrided oxides yield a higher μ_{eff} than conventional oxides, both at 300 K and at liquid nitrogen temperatures, which provides a benefit [71]-[72]. The opposite is, however, true at lower effective fields.

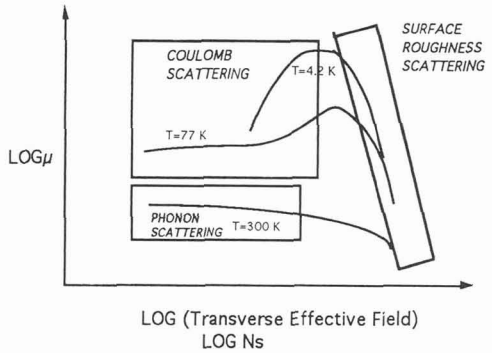

Fig. 13. Schematical representation of the temperature and gate voltage dependence of the inversion layer effective mobility of a MOSFET.

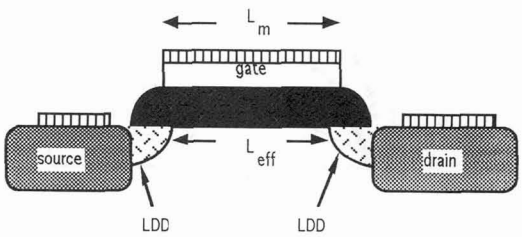

Fig. 14. Schematical representation of a LDD MOSFET.

4.3 Velocity saturation and overshoot

For deep submicron MOSFETs velocity saturation at sufficiently large lateral fields creates a serious limitation of the device performance [6],[7]. In that case, the saturation drain current becomes linearly dependent on the gate overdrive voltage, instead of quadratic and can be approximated by [6]:

$$I_{Dsat} = \frac{1}{2}\mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} \frac{(V_{GS}-V_T)^2}{[1 + \mu_0(V_{GS}-VT)/2v_{sat}L_{eff}]} \tag{16}$$

which for very small device lenghts L_{eff}-->0 reduces to the fully velocity saturated current:

$$I_{Dsat} = C_{ox}\, W_{eff}\, v_{sat}\,(V_{GS}-V_T) \tag{17}$$

The saturation velocity v_{sat} is thus an important parameter in view of the continuous downscaling of the device dimensions and ultimately can limit the performance. In many cases, v_{sat} is derived from the drift velocity v_{ds} of the carriers in the lateral electric field E_S [73], which is given by the empirical model [6],[7],[73]:

$$v_{ds} = \frac{\mu_0 E_S}{[1 + (E_S/E_C)^{\alpha}]^{1/\alpha}} \tag{18}$$

The saturation velocity is next obtained from the critical drift field E_C, since $v_{sat}=\mu_0 E_C$. The exponent α is a fitting parameter, generally ranging from 2 to 5. Recently, several alternative techniques have been

proposed to extract v_{sat}, both at 300 K [74] and at cryogenic T [7],[8],[75]. However, due to experimental difficulties (establishing an as homogeneous as possible drift field; source-drain resistance in short-channel devices,...) a large spread is generally found, giving rise to values between $4.2x10^6$ cm/s up to $9.2x10^6$ cm/s for electrons at room temperature [75] and $7x10^6$ cm/s for holes [7]. Upon cooling v_{sat} is found to increase to values approaching 10^7 cm/s (electrons) or higher [7],[8]. This implies that for short-channel devices, the benefit of cooling is only a mere 20 % increase in drive current or so, which is much smaller than the factor 2 to 4 increase observed for long-channel MOSFETs. It should finally be remarked that for ultra-short channel devices, however, velocity overshoot (and hence ballistic transport) has been reported at cryogenic temperatures [9]-[11] and even at room temperature for $L \approx 0.1$ μm MOSFETs [76],[77].

5. EFFECTIVE LENGTH AND SERIES RESISTANCE

Present-day CMOS technologies have an architecture schematically represented by Fig. 14, containing an LDD region close to the source and drain, covered by spacer oxides. The LDD serves to reduce the maximum lateral field next to the drain junction in order to reduce hot-carrier degradation effects. As a consequence, however, the series resistance of the devices increases and furthermore is no longer independent of the gate voltage. At the same time, the electrical effective device length $L_{eff}=L_m-\Delta L$ becomes also a function of $V_{GS}-V_T$. L_m is the drawn gate length and ΔL is the channel length reduction (generally positive) which is related to source-drain lateral underdiffusion. The electrical effective length is now determined by the positions where the inversion charge density equals the LDD concentration. As both R_{SD} and L_{eff} are critical parameters in the MOSFET device modelling, in the past decade, extensive effort has been spent in developping extraction techniques [78]-[83].

Classically, ΔL and R_{SD} are determined simultaneously by plotting the total measured resistance ($R_T=R_{SD}+R_{channel}$) at different $V_{GS}-V_T$ (or inverse conductance) in linear operation versus the mask length L_m [78]. The crossing point of the different lines corresponds with ΔL (horizontal axis) and with R_{SD} (vertical axis). Applying these methods to cryogenic temperatures, negative and thus unrealistic ΔL values are found generally [26],[52],[84]-[87]. An example is given in Figs 15 and 16 for bulk n-MOSFETs: while acceptable R_{SD} are obtained at 77 K, the negative ΔL in Fig. 16 indicates that the proposed method is not useful for low-temperature extraction.

In order to overcome these problems, some dedicated techniques have been proposed recently, which take into account the gate voltage dependence of R_{DS} and ΔL [84]-[86]. In that case, the total resistance as a function of the mask length is no longer considered a straight line for constant $V_{GS}-V_T$, but some function, where the best fit is to be determined. For instance, Ortiz-Conde et al. [84], assume that $G_T=1/R_T$ is given by:

$$G_T = \frac{1}{2R_{SD}} + C1\, L_{eff}^{1/3} + C2\, L_{eff}^{-2/3} \tag{19}$$

with C1 and C2 fitting parameters. In practice, it turns out that the gate voltage dependence both at 300 K and at 77 K can be described empirically by [86],[88]:

$$R_{SD} = R_{SD0} + \frac{1}{V_{GS} + a} \tag{20a}$$

$$\Delta L = \Delta L_0 + \frac{1}{V_{GS} + b} \tag{20b}$$

An alternative approach for determining the parasitic series resistance of for instance an LDD region is based on a measurement of the channel conductance $g_d=\partial I_D/\partial V_{DS}$ in the linear region [81]. If $1/g_d$ is plotted vs $1/g_m$ at constant V_{GS} (>VT), for different device lengths L, a straight line is obtained, which is given by:

$$\frac{1}{g_d} = \frac{1}{g_m}\left(\frac{1}{V_{GS}-V_T} + \theta\right) + R_{SD} \tag{21}$$

The Y-axis intercept should then correspond to R_{SD}. This technique has been used to study the series resistance of the LDD region as a function of the lateral electric field [25]. At cryogenic temperatures (< 100 K), R_{LDD} shows a pronounced reduction with the field, whereby it is believed that shallow level impact ionisation is the responsible mechanism for this reduction for an LDD lateral field E >3kV/cm.

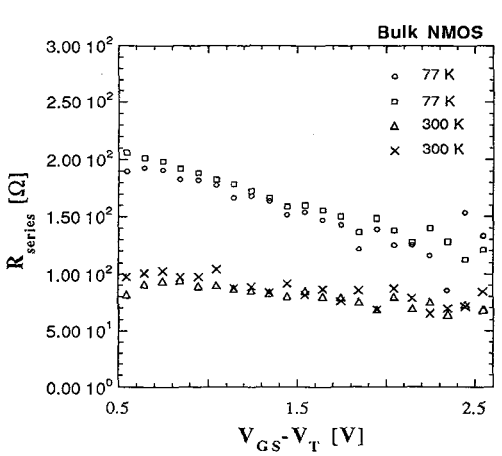

Fig. 15. Extracted R_{SD} as a function of the gate overdrive voltage for 0.7μm CMOS nMOSFETs at 300K and 77K.

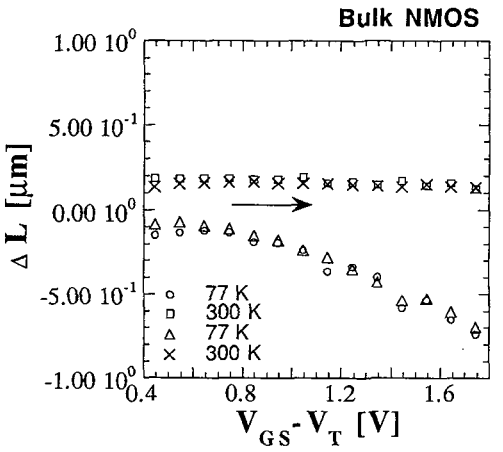

Fig. 16. Corresponding ΔL. The extractions were performed on two different L-arrays, with W=20 μm [87].

6. POTENTIAL PITFALLS AND MEASUREMENT PROBLEMS

Upon reducing the effective device length and/or the operation temperature in the linear region, one may be concerned with the fact that for some V_{DS}, the gradual channel approximation no longer holds and for instance a non-homogeneous charge density and hence a drain voltage dependent mobility results [66]. This is for instance the case in ohmic operation for MOSFETs in the liquid helium temperature region [61], for sufficiently large lateral fields (>1 V/cm). In the literature, different empirical expressions have been proposed to model the V_{DS} dependence of μ_{eff} [61],[89]. On the other hand, too small a V_{DS} is also impractical in general, so that a compromise has to be sought. At 77 K a V_{DS}=25 to 50 mV seems to be a reasonable value. For 4.2 K characterisation, even lower values can be considered, e.g. 10 mV.

Another issue related to the recording of a low temperature input curve is the step resolution in the gate voltage. As discussed recently [41], this is particularly important for an accurate determination of the subthreshold swing. Fig. 17 illustrates the value of S obtained for different V_{GS} steps at 77 K, for an AM SOI p-MOSFET. For too large a step, an erroneous value is obtained due to the slow response of the device on a relatively fast change in front gate voltage (so-called transient effect). For too small steps, on the other hand, the noise in the measurement becomes too large to allow a stable reading. The lower the temperature is, the lower optimal step height for a stable reading is necessary.

In deriving the effective mobility given by eq. (5), in many cases the inversion layer charge density qN_S is approximated by $qC_{ox}(V_{GS}-V_T)$. This first of all requires an accurate determination of the charge threshold voltage V_T and furthermore assumes the validity of the gradual channel approximation [66]. A more precise determination of qN_S is by the split C-V technique [50],[65]. At cryogenic T, some special features are observed in this type of measurements, which are related to the slow charging/discharging of interface traps, as described recently [90],[91]. Generally, rather large-area transistors are required for this type of analysis.

On several occasions, it has been noted that the MOSFET I-V characteristics suffer from transient and hysteresis effects. This is particularly true in the liquid helium temperature range for bulk MOSFETs [92]-[94], although for SOI devices, transients have been observed up to room temperature, whereby the typical time constants increase upon cooling [95]-[97]. For SOI MOSFETs time constants of minutes at 77 K up to hours and days at 4.2 K have been observed [98] when either the front or the back-gate bias was abruptly changed at low T. As a result, the threshold voltage can be switched to any desirable value within a certain operation margin and with a stability determined by the transient time constants. It has been suggested to utilise this so-called multistable charge-controlled memory effects at cryogenic T for one and two-transistor memory cells [98]. From a parameter-extraction viewpoint, this type of transient behaviour is highly undesirable. In many cases, it is related to the freeze-out of carriers on the dopant atoms in the substrate [94] and thus inherently related to low-temperature operation. Ways to circumvent, or at least minimise the effects is to measure the characteristics from high to low temperatures, with the bias applied

at higher temperatures [50]. Biasing at higher temperatures allows to build up the equilibrium depletion region in the substrate with much lower time constants. However, it should be remarked that upon changing the device bias at deep cryogenic T generally provokes new transient and memory effects, which are not easy to 'erase' [94]-[96].

A final concern for low temperature operation of devices is the so-called self-heating problem [99]-[103]. In brief, this phenomenon is related to the fact that the local device (lattice) temperature can be higher than the ambient temperature due to the dissipiation of the power $I_D V_{DS}$ in the channel. This can have serious consequences for the extracted carrier mobilities in n- and p-channel devices [100]-[101]. Typical for devices suffering from selfheating is the negative differential resistance in saturation, which can be particularly pronounced for short-channel SOI MOSFETs [103]. Self-heating effects are in first order caused by an insufficient thermal contact with the cooling ambient. In case of SOI devices, the floating substrate on top of a buried oxide does not allow an efficient heat removal. However, as illustrated in Fig. 20, these effects are only thought to become important at higher V_{DS}s in saturation.

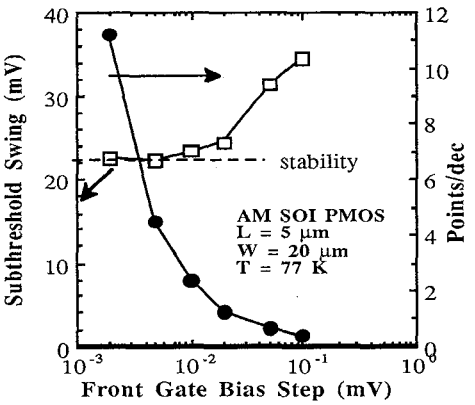

Fig. 17. Subthreshold swing as a function of the front gate voltage step at 77 K for a 20 μmx5 μm SOI AM p-MOSFET.

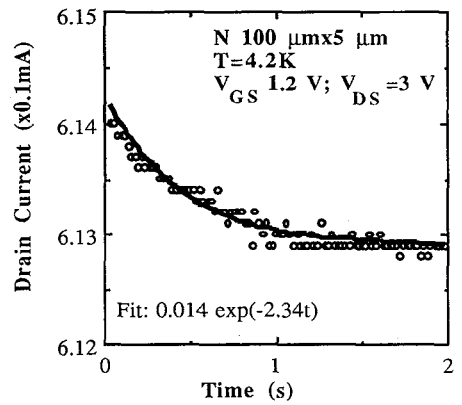

Fig. 18. Transient response of a 100 μmx5 μm bulk n-MOSFET at 4.2 K, upon pulsing both the gate and the drain voltage from 0 V to respectively 1.2 V and 3 V. Also shown is the exponential fit to the data points.

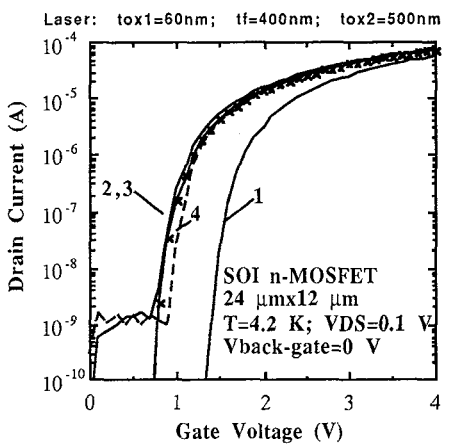

Fig. 19. V_T instability in a PD SOI n-MOSFET at 4.2 K. Curve 1 is the original measurement. Curves 2 and 3 are registered after that the drain has been swept to +3 V and +5 V respectively and curve 4 is after 24 h unbiased relaxation at 4.2 K.

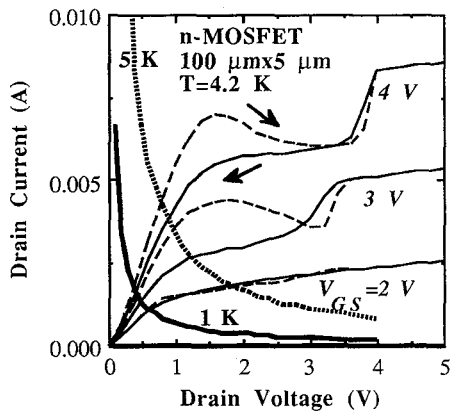

Fig. 20. Estimation of the self-heating effect in a 100 μmx5 μm bulk n-MOSFET at 4.2 K. The calculated hyperbolic lines correspond to a local temperature rise in the channel of respectively 1 K and 5 K.

7. CONCLUSIONS

From the above overview, it is clear that there exists still a necessity for adequate parameter extraction of Si MOSFETs operated at cryogenic temperatures. The state-of-the-art has been summarised and from this follows that there are still some problem areas, related to the device parasitics which gain importance upon down-scaling the device dimensions.

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