Low-Temperature Modelling of Electron-Velocity-Overshoot Effects on 70-250 nm Gate-Length MOSFETs

J. Roldán, F. Gámiz, J. López-Villanueva, J. Carceller

► To cite this version:

J. Roldán, F. Gámiz, J. López-Villanueva, J. Carceller. Low-Temperature Modelling of Electron-Velocity-Overshoot Effects on 70-250 nm Gate-Length MOSFETs. Journal de Physique IV Proceedings, 1996, 06 (C3), pp.C3-13-C3-18. 10.1051/jp4:1996302 . jpa-00254220

HAL Id: jpa-00254220

<https://hal.science/jpa-00254220>

Submitted on 1 Jan 1996

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Low-Temperature Modelling of Electron-Velocity-Overshoot Effects on 70-250 nm Gate-Length MOSFETs

J.B. Roldán, F. Gámiz, J.A. López-Villanueva and J.E. Carceller

Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Facultad de Ciencias, Avd. Fuentenueva s/n, 18071 Granada, Spain

Abstract. Modelling of the increase of MOSFET transconductance produced by electron-velocity overshoot as channel lengths are reduced has been performed at low temperature. The results obtained have been compared to room-temperature ones. To accomplish this, the charge-control model has been used to obtain a simple analytical expression to account for electron-velocity overshoot effects on the performance of very short channel MOSFETs. This model can be easily included in circuit simulators of systems with a huge number of components. Experimental verification of the accuracy of this model is provided. The improvement of MOSFET transconductance due to electron-velocity overshoot is found to be greater at low temperature than at room temperature.

1. INTRODUCTION

MOSFET transconductance, g_m , is known to be one of the most important figures of merit in dealing with the large-signal switching performance of logic devices, as the time constant for a small MOSFET to charge a load is proportional to C/g_m , where C is the node capacitance. That is why accurate modelling of this parameter is essential in circuit simulators of state-of-the-art MOSFETs [1]. The continuous reduction of the dimensions of these devices makes the carrier transit time comparable to the energy relaxation time [2], thus causing electron-velocity-overshoot effects. Therefore, this fact has a great influence on the performance of very short channel MOSFETs, mostly at low temperature.

2. CHARGE-CONTROL MODEL

We have taken into consideration the velocity-overshoot effects on the transconductance of short channel MOSFETs by using a local augmented drift-diffusion model for the electron velocity based on Thornber's equation [3]. This has been done by adding a term dependent on the longitudinal electric field gradient, which has been found to be the main cause of electron-velocity overshoot [4,5] (Expression 1):

$$v(E_{\parallel}, E_{\perp}) = \frac{\mu_0(E_{\perp})E_{\parallel}}{\left(1 + \left(\frac{\mu_0(E_{\perp}) \times E_{\parallel}}{v_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} + \lambda \frac{\partial E_{\parallel}}{\partial x} \quad (1)$$

We have corrected the stationary velocity vs. longitudinal electric field curves using Equation 1 to fit the velocity profiles obtained using a MOSFET Monte Carlo simulator [6]. A value of $\lambda = 6.4 \times 10^{-5} \text{ cm}^3/\text{Vs}$ ($T = 77\text{K}$) was found to work well for a wide sample of 100-1000 nm channel length MOSFETs at different operating conditions. This expression has also been found to work well in our drift-diffusion simulator, reproducing the experimental behaviour that transconductance shows as the length of the

MOSFET channel is reduced. Taking this as a starting point, we have used the charge control analysis to get a closed expression for the transconductance. We suppose that the source is located at $x=0$ and the potential at that point is zero; the drain is assumed to be at $x=L$, where L is the effective channel length, at a potential at V_{DS} . The drain current can be calculated as a product of the mobile channel charge (which is a function of the gate-source voltage and the local channel potential $V(x)$), the channel width, and the electron velocity along the X axis, from the source towards the drain (given by Expression 1):

$$I_D = W Q(V(x)) v_x(x) \quad (2)$$

At this stage some simplifying assumptions are made: we take an average value μ for the low-longitudinal-electric-field mobility corresponding to an average value of the transverse electric field along the channel. This is not a rough approximation for low- and medium-drain voltages; we also take $\beta=1$. Under these assumptions we get

$$I_D \int_0^L \left(1 + \frac{\mu}{v_{sat}} \frac{dV}{dx}\right) dx = W \int_0^L Q(V) \left[\mu \frac{dV}{dx} + \lambda \frac{d^2V}{dx^2} \left(1 + \frac{\mu}{v_{sat}} \frac{dV}{dx}\right) \right] \frac{1}{\frac{dV}{dx}} dV \quad (3)$$

We integrate the previous expression making use of the mean-value theorem for the second term in brackets and a simple variable change for the rest. The result is given by

$$I_D \left(1 + \frac{\mu}{v_{sat}} \frac{V_{DS}}{L}\right) L = W [\mu + \lambda \langle \frac{d^2V}{dx^2} (\frac{1}{\frac{dV}{dx}} + \frac{\mu}{v_{sat}}) \rangle] F(V_{GS}, V_{DS}) \quad (4)$$

where the mean value is shown in angles for the above expression, and the function $F(V_{GS}, V_{DS})$ is the integral of the inversion charge in the channel:

$$F(V_{GS}, V_{DS}) = \int_0^{V_{DS}} Q(V) dV \quad (5)$$

This expression contains the differences between the different field-effect transistors, and so changing the expression for $Q(V)dV$ would be enough to model these effects in other FET (MOSFETs, HEMTs, MESFETs, etc). The expression in angles is very high near the drain compared to the value of this expression in other zones of the channel and the value of the inversion charge that multiplies this value in the integral is higher near the source than in the rest of the zones closer to the drain, so there is no zone of the channel where the integrand is clearly dominant. Therefore, we will employ a semiempirically modified mean value along the channel for the expression in angles. To do so, we approximate the first and second derivative of the electrostatic potential as follows:

$$\frac{d^2V}{dx^2} \approx a \frac{V_{DS}}{L^2} \quad \frac{dV}{dx} \approx \frac{V_{DS}}{L} \quad (6)$$

where "a" is a constant. The transconductance obtained after these considerations is given by

$$g_m = \frac{W}{L} \frac{\partial F(V_{GS}, V_{DS})}{\partial V_{GS}} \left[\frac{\mu}{1 + \frac{\mu}{v_{sat}} \frac{V_{DS}}{L}} + \lambda \frac{a}{L} \right] \quad (7)$$

In accordance with the above calculation, it is obvious that the quotient of the transconductance, accounting and not accounting for the effects of velocity overshoot, can be calculated as

$$R = \frac{g_{m_{with\ overshoot}}}{g_{m_{without\ overshoot}}} = 1 + a\lambda \left(\frac{1}{\mu L} + \frac{V_{DS}}{v_{sat} L^2} \right) \quad (8)$$

3.RESULTS

In order to check this expression, we have calculated the ratio between experimental "intrinsic" transconductances measured for a sample of MOSFETs fabricated by G. A. Sai-Halasz et al. [7] and the same transconductances calculated by these authors using a classical drift-diffusion simulator with $V_{GS} - V_T = 0.6$ V, $V_{DS} = 0.8$ V, $\mu = 390$ cm²/Vs, $v_{sat} = 8 \times 10^6$ cm/s at $T = 300$ K and $\mu = 720$ cm²/Vs, $v_{sat} = 1 \times 10^7$ cm/s at $T = 77$ K. The same ratio, calculated using Equation 8 for the same parameters, is shown in solid line for $a = 6.25$ and $\lambda = 4 \times 10^{-5}$ cm³/Vs ($T = 300$ K) and $\lambda = 6.4 \times 10^{-5}$ cm³/Vs ($T = 77$ K) (Figure 1).

Figure 1: Room- and low-temperature ratio between experimental "intrinsic" and simulated transconductances versus channel length (solid line). The same ratio calculated analytically by Equation 8 is shown in solid squares.

As can be seen in Figure 1 the relative improvement of the transconductance is important for MOSFETs with a channel under $0.15 \mu\text{m}$. The low-temperature ratio is higher than the room-temperature one for all channel lengths; comparison of the two curves shows that the low-temperature ratio is higher than 15% for channel lengths under $0.1 \mu\text{m}$.

We have also tried to reproduce the experimental transconductances by applying Equation 7. To do so, we fit the measurements by G. A. Sai-Halasz et al. using Equation 7 and an estimated value for the partial derivative of $F(V_{GS}, V_{DS})$. To get this estimated value we took as a starting point a general expression for the absolute value of the inversion charge per unit area in MOSFETs [8]:

$$Q(V) = C_{ox}(V_{GB} - V_{FG} - \psi_s + \frac{Q_B}{C_{ox}}) \quad (9)$$

where C_{ox} is the oxide capacity per unit area, V_{FB} is the flat-band voltage, ψ_s is the surface potential and Q_B the depletion charge per unit area. The voltage between substrate and source was zero. Therefore we can substitute V_{GB} by V_{GS} . In strong inversion, the surface potential can be approximated by $\psi_s(x) \approx \phi_B + V(x)$ along the channel, where ϕ_B equals $2\phi_F + 6\phi_t$ ($e\phi_F$ is the difference between the Fermi level and the intrinsic Fermi level in the bulk in eV, and $\phi_t = KT/e$, K being Boltzmann's constant). If we substitute this value of the surface potential in strong inversion (which is the case here) in Equation 9, if Q_B is represented only by its value at the source, if its variation along the channel is neglected, and if the definition of threshold voltage is used [8], we obtain:

$$Q(V) = C_{ox}(V_{GS} - V_T - V) \quad (10)$$

Therefore with regard to the definition of function $F(V_{GS}, V_{DS})$, Equation 5, an estimated value of the partial derivative of $F(V_{GS}, V_{DS})$ can be easily obtained:

$$\frac{\partial F(V_{GS}, V_{DS})}{\partial V_{GS}} \approx C_{ox} V_{DS} \quad (11)$$

The value given by G.A. Sai-Halasz et al. for the oxide width was 4.5 nm, so for the bias reported before $V_{GS} - V_T = 0.6$ V and $V_{DS} = 0.8$ V, the estimated value of the partial derivative of $F(V_{GS}, V_{DS})$ is 6.1×10^{-7} C/cm². The values used to fit the experimental "intrinsic" transconductances for the partial derivative for $F(V_{GS}, V_{DS})$ were 5.2×10^{-7} C/cm² at $T = 300$ K and 5.5×10^{-7} C/cm² at 77K. A perfect fit can be observed in both cases (Figure 2).

Figure 2: Room- and low-temperature experimental "intrinsic" transconductances versus channel length and modelled transconductances calculated by means of Equation 7.

As can be observed the increase of experimental transconductances over theoretical ones (drift-diffusion simulated) is higher at low temperature. This is produced by a lower electron-phonon interaction which increases the energy relaxation time, making velocity overshoot more likely. A higher λ is obviously needed in this case, which means that in order to improve MOSFET-performance features connected to velocity overshoot-effects, low temperature operation is recommended.

To see what the contribution of the new term to the previous one is more clearly, as MOSFET channel length is reduced, we have plotted them versus channel length as they appear in Equation 7, adjusting for channel width and $\partial F(V_{GS}, V_{DS})/\partial V_{GS}$ normalization at $T=77K$.

Figure 3: Terms A and B described in Equation 12 are shown versus channel length at $T=77K$, calculated using the values $V_{DS}=0.8 V$, $\mu=720 \text{ cm}^2/Vs$, $v_{sat}=10 \times 10^6 \text{ cm/s}$, $a=6.25$, $\lambda=6.4 \times 10^{-5} \text{ cm}^3/Vs$. Term A (white squares), Term B (full squares).

Terms A and B are

$$\text{Term A} = \frac{\mu}{(1 + \frac{\mu}{v_{sat}} \frac{V_{DS}}{L})L} \quad \text{Term B} = \lambda \frac{a}{L^2} \quad (12)$$

As can be observed, Term B is not worth taking into account for channel lengths over $0.2 \mu m$. Velocity overshoot, as expected, does not affect the transconductance for these lengths. However, as channel length is reduced, Term B rises accounting for the increase observed experimentally, thus demonstrating that the effects of velocity overshoot on MOSFET transconductance are reproduced. We have also checked this fact by using our Monte Carlo MOSFET simulator.

The MOSFET transconductance increase due to electron-velocity-overshoot effects can be incorporated into conventional circuit simulators making use of Equation 7. Different materials and temperature conditions can be modelled by using the λ parameter. Parameter "a" can be used to characterise different technologies and MOSFET designs. The longitudinal electric field gradient at the MOSFET source depends on the specific design; velocity-overshoot effects are related to the value of this gradient and can be taken into account by means of parameter "a". However, as has been seen, both material and design

contribute to increase Term B in the same way (Equation 7), therefore a single parameter would be necessary to characterise a MOSFET.

4.-CONCLUSIONS

A simple analytical model to account for electron-velocity-overshoot effects on submicron MOSFET transconductance has been provided. It has been obtained by means of charge-control analysis. It has been shown that as channel dimensions shrink, a term inversely proportional to the square of the MOSFET channel length accurately describes the transconductance increase produced by electron-velocity overshoot. This model can be easily included in circuit simulators of systems with a huge number of components. Low-temperature conditions have been found to increase velocity-overshoot effects, improving performance of MOSFETs with channel lengths under $0.15\text{ }\mu\text{m}$.

Acknowledgements

This work has been carried out within the framework of research project TIC 95-0511, supported by the Spanish Government (CICYT).

References

- [1] Fischetti M.V., Laux S.E., Lee W., Solid-State Electron **32** (1989) p. 1723.
- [2] Ono M., Saito M., Takashi Y., Fiegna C., Ohguro T., Iwai H., IEEE Transaction on Electron Devices **ED-42** (1995) pp-1822-1830.
- [3] Thornber K.K., J. Appl. Phys. vol 51 (1980) p. 2127.
- [4] Baccarani G., Wordeman M.R., Solid-State Electron **28** (1985) p 407.
- [5] Ruch J.G., IEEE Transc. on Electron Devices ED-19 (1972) p.652.
- [6] Roldán J.B., Gámiz F., López-Villanueva J.A., Carceller J.E., "Monte Carlo simulation of a submicron MOSFET including inversion layer quantization", 4th IWCE Tempe (Arizona) October 1995, p. 37.
- [7] Sai-Halasz G.A., Wordeman M.R., Kern D.P., Rishton S., Ganin E., IEEE Elec. Dev. Let. **EDL-9** (1988) p.464.
- [8] Tsividis Y.T., Operation and modelling of the MOS transistor (McGraw-Hill, New York, 1987) p.110.