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Investigation of the Substrate/Epitaxial Interface of Si/Si_{1-x}Ge_x Layers Grown by LPCVD

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Abstract. The paper reports a study of the quality of the substrate/epilayer interface. Before growing the Si or Si/Si_{1-x}Ge_x structures by low pressure chemical vapour deposition, Si(100) substrates were cleaned by a modified RCA-cleaning and just before epitaxy different ex-situ and in-situ processes were applied to remove the oxide layer grown on the wafer substrates in the last step of the RCA-cleaning. The effect of interfacial contamination on electrical and optical properties were studied. By a wet-chemical removal of the oxide layer an interfacial oxygen level of 1.3×10^{13} atoms/cm² is found, while a thermal removal leads to an interfacial oxygen level below 6×10^{12} atoms/cm². In both cases carbon levels of $(1-2) \times 10^{14}$ atoms/cm² have been detected. By electrochemical capacitance-voltage profiling it was found that these contaminations are connected with electrically active donors. According to our investigations, electrochemical capacitance-voltage profiling is suitable to give a quick indication on the quality of the substrate/epitaxial interface. In addition, the removal of the oxide layer was investigated by high resolution electron energy loss spectroscopy on cleaned Si-surfaces.

1 INTRODUCTION

In recent years, a lot of work has been done on Si wafer cleaning to achieve a surface free of contamination [1] -[6]. This was motivated by the fact that structural and electrical properties of epitaxial films are improved when the amount of contaminations (especially oxygen and carbon) at the substrate/epilayer interface is reduced. The cleaning procedure commonly used consists of a wet chemical treatment ending with an oxidation of the clean Si-surface as a protection against atmospheric recontamination. Just before growing the epitaxial layer, the oxide is removed ex-situ in aqueous HF-solutions or in-situ by a thermal treatment.

The RCA-cleaning procedure [7] followed by an aqueous HF-dip was successful in achieving clean Si-surfaces with oxygen and carbon levels of less than 10^{13} cm⁻² [2, 8]. After a HF-dip the Si-surface is protected by hydrogen termination. In these procedures, samples were not water-rinsed, because it was shown that this lead to the contamination of the wafer surfaces [9, 10]. But, on oxide patterned wafers used for selective growth, where large areas of hydrophilic oxide are exposed during the etch, a water-rinse is preferred to wash away the HF. In this case the HF-dip can be replaced by a buffered HF (AF91), because this produces a surface that is potentially tolerant to a water-rinse without surface oxidation [11].

Borland et al. [12] found that after a HF-dip of 15 seconds followed by a DI-water-rinse and spin rinse dry, an in-situ rapid thermal cleaning (1 minute hydrogen bake at at least 850°C) was required

to eliminate the native oxide.

After removal of the oxide layer by high-temperature desorption, there is no hydrogen termination at the Si surface. Chemical equilibrium data for the stability of an oxide-free Si surface in the presence of water or oxygen vapour are given by studies of Smith and Gidini [13, 14].

In this paper we will compare different in-situ and ex-situ techniques to remove the oxide layer present on the wafer surface after the modified RCA-cleaning. Cleaned surfaces were studied by high-resolution electron energy loss spectroscopy (HREELS). Further, Si and Si/Si_{1-x}Ge_x -structures were grown by low pressure chemical vapour deposition (LPCVD) and characterized by Normarski microscopy, electrochemical capacitance-voltage (eCV), transmission electron microscopy (TEM), secondary-ion mass spectrometry (SIMS), and photoluminescence (PL) measurements.

After an aqueous AF91- or HF-dip (for 20 seconds) followed by a DI-water-rinsing for 1 minute, a blow dry with nitrogen, and an in-situ thermal cleaning at 900°C-950°C, oxygen and carbon contaminations at the substrate/epilayer interface with a level of $(8-10) \times 10^{12} \text{ cm}^{-2}$ and $(8-10) \times 10^{14} \text{ cm}^{-2}$, respectively, have been detected. By eCV measurements, it could be shown that these contaminations are correlated with electrically active donors.

Two different ways will be presented to reduce the contamination level at the substrate/epitaxial interface. The first one is to avoid the wet chemical HF-Dip and to use only a thermal removal of the oxide layer. In the second case, we did not use a thermal cleaning above the growth temperature, but, we tried to find an optimal way to perform the HF-dip and the heating-up procedure to the growth temperature. We will show, that eCV-measurements are suitable to get a first impression about the quality of the substrate/epitaxial interface. Compared to SIMS and TEM, eCV is a simple and quick measuring method.

2 EXPERIMENTAL DETAILS

The purpose of the work was to develop a recipe to prepare a clean Si substrate surface for LPCVD growth and to study the differences in contamination levels on the Si-substrate surfaces after different ex-situ and in-situ procedures to remove the oxide layer. This oxide grows during the last step of the modified RCA-cleaning as described in table I. We used (001)-orientated Si wafers (n-type doped with a resistivity of $\sim 1 \text{ } \Omega\text{cm}$) with oxide patterned for in-filling selective growth in order to determine the thickness of the epitaxial layer by step height measurements. Also $1000 \text{ } \Omega\text{cm}$ p-type and $1-10 \text{ } \Omega\text{cm}$ n-type (001) unpatterned Si substrates were used.

After removing of the oxide layer, Si- or Si/Si_{1-x}Ge_x -epitaxial layers were deposited in a cold wall, load locked LPCVD-system [15].

The reactor is a horizontal quartz tube with a SiC coated graphite holder. Heating is performed by external halogen lamps placed below and above the reactor tube with temperature control by three thermocouples placed inside the holder. The high vacuum system consisting of a turbomolecular pumping system for high vacuum is in parallel with a combination of root blower with a mechanical pump for pumping the reactive gases. The base pressure is $2 \times 10^{-7} \text{ Torr}$. The epitaxy reported here was carried out at a pressure of 0.12 Torr and temperature of 700°C - 800°C using SiCl₂H₂ and GeH₄ as source gases and H₂ as carrier gas.

SIMS depth profiling was performed in a quadrupole instrument with a Cs⁺ primary beam at 60° with respect to the sample normal and a primary ion energy of 10 keV. Both the detection of positive (CsSiO⁺) as negative (C⁻ and O⁻) secondary ions was used. The sheet densities for the impurities at the interface were obtained by integrating the impurity peaks of the SIMS measurements and subtracting out the background concentrations. For the eCV measurements, we used a polaron profile plotter (PN4300) with a NH₄HF based electrolyte and TEM was carried out with a JEOL 4000FX electron microscope. PL spectra were taken using a Fourier transform spectrometer (BIO

RAD FTS 40) and an Ar-ion laser emitting at 488nm.

The cleanness of the Si-substrate surfaces was studied by high-resolution electron loss spectroscopy (HREELS). For this we prepared substrates as for LPCVD. The only difference is that the base pressure of this characterisation system is 4×10^{-11} Torr and the samples are electrically heated instead of radiation heating as used in the LPCVD-system.

table I: Modified RCA-cleaning process.

Step	Solution	Temperature	Time	Comments
1a	H ₂ O ₂ : H ₂ SO ₄ 1 : 2	75 °C	5 minutes	ultra sonic
1b	rinse in deionized H ₂ O	20 °C	5 minutes	
2a	H ₂ O ₂ : NH ₄ OH : H ₂ O 1 : 1 : 5	75 °C	10 minutes	ultra sonic
2b	rinse in deionized H ₂ O	20 °C	10 minutes	
3a	HF : H ₂ O 1 : 50	20 °C	15 seconds	ultra sonic
3b	rinse in deionized H ₂ O	20 °C	30seconds	
4a	H ₂ O ₂ : HCl : H ₂ O 1 : 1 : 5	75 °C	10-15 minutes	ultra sonic
4b	rinse in deionized H ₂ O	20 °C	20 minutes	
5	dry blow with N ₂			

3 RESULTS AND DISCUSSION

First of all we cleaned wafers with a modified RCA-cleaning (Table I), to remove organic and metallic contaminations. At the end of this modified RCA-cleaning the Si-surface is chemically oxidized, with a thin (2.5 nm) oxide layer, as a protection against atmospheric recontamination. Just before growing, the wafers received a 20 second dip in an AF91-solution followed by a rinse in DI-water for 1 minute and then blown dry with nitrogen.

Before epitaxial growth of Si-layers or Si/Si_{1-x}Ge_x -structures the wafers were prebaked at 650°C for 10 minutes to remove hydrocarbons and at 900°C - 950°C for 1-40 minutes to remove rest of SiO₂ that could have grown during the DI-water-rinsing. In some cases a SiCl₂H₂ (0.1 sccm) or a H₂ (200 sccm) gas flow was used during the heating at the highest temperature. The results of SIMS and eCV measurements for various cleaning techniques are presented in table II.

Fig. 1a shows a CV measurement and Fig. 1b shows a TEM-image of sample 832AF which we will discuss in more detail. The sample consists of a Si(25nm)/Si_{0.91}Ge_{0.09}(235nm)/Si(30nm) epitaxial layer, which was not intentionally doped.

Figure 1: a) eCV-profile and b) TEM-image of a Si/Si_{0.91}Ge_{0.09}/Si epitaxial layer structure. The substrates have been dipped in AF91 for 20 seconds and were prebaked at 900°C for 40 minutes. The inset of Fig. 1a shows a CV-profile taken by varying the reverse bias.

The CV measurement (Fig. 1a) shows that the n-type background in the epitaxial layer is below 10^{16} cm^{-3} , as expected from earlier investigations [16]. However, the substrate/epitaxial interface is marked by a strong n-type charge accumulation. This indicates that the interfacial contaminations, are partially electrically active and n-type. A good spatial resolution is obtained by recording the CV depth profile by increasing the reverse bias (inset of Fig. 1a). However, in this case avalanche breakdown restricts the maximum depth that can be measured. A total depth profile has been obtained, by alternating CV measurements and etch steps (Fig. 1a). However, these etch steps have a detrimental influence on the depth resolution as seen in Fig. 1a. For this reason, when the peak profile is needed, as in this case, the CV measurement is preferred.

In the TEM cross section (Fig. 1b) the interface is clearly seen as a dark stripe, which shows the presence of contamination. In spite of the high level of contamination at the substrate/epitaxial interface, a monocrystalline layer could be grown. A possible explanation is the dissolution of individual oxygen and carbon atoms into the silicon lattice [17]. The interfacial contamination shown by TEM might be due to the formation of silicon carbide. This can appear, if significant loss of hydrogen from the surface occurs prior to the hydrocarbon desorption [18]. The presence of donors may possibly be a consequence of the nucleation of oxygen at a carbon site [19]. As will be shown below, the interfacial contaminations have a detrimental effect on the optical properties of single and multiple quantum wells (SQW and MQW).

The results presented here apply to all samples, which have been wet-chemical (ex-situ) and thermal (in-situ) treated to remove the oxide layer present on the wafer surface after the RCA-cleaning. The same results have been obtained when the AF91-dip was replaced by a diluted HF-dip. All these samples revealed a high carbon ($8\text{-}10 \times 10^{14} \text{ atoms/cm}^2$) and oxygen ($8\text{-}10 \times 10^{12} \text{ atoms/cm}^2$) concentration at the substrate/epitaxial interface.

The significant loss of hydrogen passivation at the Si-surface during the thermal prebake and the wet-chemical HF-dip (including the DI-water-rinsing) are two possible steps, during which the Si-surfaces could be contaminated. Therefore we have investigated two other ways to remove the oxide layer before epitaxy. The first one, is to remove the oxide layer by a thermal treatment as was shown by Tabe [20]. Sample 832 have been grown in the same run as sample 832AF, which we discussed above. The only difference between these samples is that sample 832 did not get a wet-chemical treatment, after the RCA-cleaning.

Fig. 2b

50 nm
└───┘

Figure 2: a) eCV-profile and b) TEM-image of a Si/Si_{0.91}Ge_{0.09}/Si epitaxial layer structure. The substrates have been prebaked at 900°C for 40 minutes.

The eCV profile (Fig. 2a) does not show an accumulation of charge at the interface layer for sample 832. The donor concentration is low enough to deplete the whole epitaxial layer ($\sim 300\text{nm}$) by the Schottky-contact and in the TEM image (Fig. 2b), the dark stripe is replaced by a few contrast points. Further, according to the SIMS measurements, the measured carbon ($1.4 \times 10^{14} \text{ cm}^{-2}$) and oxygen ($6 \times 10^{12} \text{ cm}^{-2}$) levels at the interface are noticeably reduced compared to the sample with both an AF91-dip and a thermal prebake. In this case, we had a oxygen signal from the order of the background concentration and only a maximum value of the oxygen contamination can be given.

These results are characteristic for all epitaxial samples subjected to a removal of the oxide layer by a wet-chemical treatment and a thermal prebake at the one side and only a thermal removal of the oxide at the other side. Changing or shutting off the gas flows did not lead to a further reduction of the contamination levels at the interface layers.

The reduction of the contaminations at the substrate/epitaxial layer by avoiding the AF91- or HF-dip is further illustrated by HREELS on cleaned Si-surfaces. Fig. 3a shows HREELS done on a sample after a modified RCA-cleaning and an AF91-dip followed by DI-water-rinsing, nitrogen dry blow and a thermal prebake at about 900°C under ultra high vacuum for 10 minutes. In Fig. 3b high resolution electron energy loss spectra on a sample with the same treatment except the AF91-dip are shown. It results that the wet-chemical removal of thin SiO_2 -layers has a detrimental effect on the cleanness of the Si-surface. Hydrocarbons and carbon are observed by HREELS (Fig. 3a). Between energy losses of 150meV and 300meV a high background is observed which is mainly due to the excitation of C-C and CH_x . This might be due to the fact, that after the DI-water-rinse, a significant loss of the hydrogen-termination occurs that should arise after the AF91-dip.

Figure 3: a) HREELS of a RCA-cleaned sample, dipped in AF91 for 20 seconds and prebaked at 900°C for 10 minutes and b) HREELS of a RCA-cleaned sample prebaked at 900°C for 10 minutes.

The sample without the AF91-dip had a much cleaner surface (Fig. 3b). The intensity of the quasi-elastic peak is much higher compared with the previous sample, and only low peak intensities due to the excitation of Si-C and C-C are observed in Fig. 3b. The carbon contamination could even be further decreased by a thermal annealing at 500°C for 10 hours.

The influence of the interfacial contaminations on the optical properties was investigated using PL measurements. These measurements were done on a Si/Si_{0.9}Ge_{0.1} multiple quantum well structure (MQW) and are shown in Fig. 4. One of the samples (810AF) was subjected to an AF91-dip followed by DI-water-rinsing and both samples have been prebaked at 950°C for 10 minutes. Both samples show excitonic peaks (no-phonon (NP) and transversal optical phonon (TO) replicas) arising from the Si_{0.9}Ge_{0.1} layers. There are no dislocation lines at 806 meV and 874 meV, indicating that in both samples (with and without AF91-dip) the Si_{0.9}Ge_{0.1} layers are fully strained. Remarkable is the increased PL-intensity of the sample without AF91 treatment which indicates a reduction of non-radiative recombinations in this sample. Because the samples were grown in the same run, we suppose that this is related to the reduction of interfacial contaminations.

Figure 4: PL spectra of a MQW structure, with and without AF91 treatment (sample 810).

A shortcoming of the thermal removal of the oxide layer is that one loses the advantage of low-thermal budget processing. Therefore, the second procedure used to reduce the contamination at the substrate/epitaxial interface is, to rely completely upon hydrogen passivation after a HF-dip, as demonstrated by Meyerson [21]. The adlayer of hydrogen which is formed during the HF-dip on the Si-substrate, leads to a reduction of the reactivity of the Si-surface with respect to oxidants such as oxygen and water. Therefore, RCA-cleaned substrates were dipped in diluted HF (5%, diluted in DI-water or in ethanol). After the HF-dip, only a part of the samples have been rinsed in DI-water. Then the substrates were prebaked for 1 hour at 200°C or at 400 °C (to remove the hydrocarbons) and a SQW-structure was grown. It was taken care that during the heating the temperature of the growth chamber did not exceed the growth temperature. The lowest donor concentration in eCV measurements ($2.2 \times 10^{17} \text{ cm}^{-3}$) was obtained for a 40 seconds dip of the substrate in 5% HF, diluted in ethanol followed by a DI-water-rinse for 15 seconds. Before epitaxy, the substrates were prebaked at 400°C for 1 hour using a hydrogen flow of 500 sccm and a pressure of 1 torr. According to SIMS measurements, the carbon and oxygen levels at the interface layer are $1.8 \times 10^{14} \text{ cm}^{-2}$ and $1.3 \times 10^{13} \text{ cm}^{-2}$, respectively. Especially, the reduction of the carbon level is an improvement compared to sample 832AF. Comparing different samples, the reduction of the n-type charge at the interface, found in eCV-measurements, is related with the enhancement of the PL intensity, in which NP transitions and their TO replicas from the QW are observed.

Table II: Interface sheet concentrations (atoms/cm²) of carbon and oxygen observed using SIMS and peak values of electrical active donors measured by eCV. Various cleaning procedures were used prior to growth.

wetchemical	Cleaning Procedure				SIMS		eCV
	first prebake		second prebake		carbon atoms/cm ²	oxygen atoms/cm ²	peak value cm ⁻³
	Temp (°C)	time (minutes)	Temp (°C)	time (minutes)			
20 sec. AF91 dip + 60 sec. DI-rinse	650	10	900 or 950	1 - 40	(8-10)×10 ¹⁴	(8-10)×10 ¹²	7×10 ¹⁸ -3×10 ¹⁹
20 sec. AF91 dip + 60 sec. DI-rinse	---	---	900 or 950	1 - 40	(8-10)×10 ¹⁴	(8-10)×10 ¹²	7×10 ¹⁸ -3×10 ¹⁹
20 sec. HF dip + 60 sec. DI-rinse	---	---	900	10	(8-9)×10 ¹⁴	7×10 ¹² -3×10 ¹³	(1-3)×10 ¹⁹
---	---	---	900	10	(1-2)×10 ¹⁴	< 5×10 ¹²	---
---	650	10	900 or 950	10, 40 or 80	(1-3)×10 ¹⁴	< 6×10 ¹²	---
40 sec. HF dip + 15 sec. DI-rinse	400	60	---	---	1.8×10 ¹⁴	1.3×10 ¹³	2.2×10 ¹⁷

4 CONCLUSIONS

In this work we compared the quality of the interfacial layer of epitaxial Si and Si/Si_{1-x}Ge_x layers, grown after either a wet-chemical and/or a thermal removal of the native oxide layer. All substrates were cleaned by a modified RCA-cleaning that produces a SiO₂ protecting layer on the clean Si-substrates. It was found, that compared to a wet chemical removal of the oxide layer followed by a thermal prebake at high temperatures, epitaxial layers with less carbon and oxygen contaminations at the interface could be grown by just a thermal removal of the oxide. Another procedure to reduce contaminations at the interface is to rely upon hydrogen passivation and to avoid temperatures above the growth temperature.

We have shown that these contaminations are (partially) electrically active, and the reduction of the interfacial contamination is noticeable in the optical properties of Si/Si_{1-x}Ge_x layers. We have shown that the eCV profiling technique is suitable to give a quick indication of the quality of the substrate/epitaxial interface. This is an advantage, because this technique is much less cumbersome than TEM and SIMS.

However, a shortcoming of the thermal removal of the oxide layer is that one loses the advantage of low-thermal budget processing.

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