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Preparation of small-area Al/AlO_x/Al tunnel junctions in a self-aligned in-line technology and observation of the Coulomb blockade

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Abstract: We have demonstrated the suitability of a self-aligned in-line (SAIL) technique for the preparation of ultra-small high-ohmic tunnel junctions as required for the investigation of single-charge tunneling phenomena. The Coulomb blockade has been observed at 14mK by means of a series array of five Al/AlO_x/Al tunnel junctions operated in the normal-conducting state. We have applied this conception to the fabrication of single junctions in a Nb/NbO_x/PbAuIn system as well. At 4.2K these samples show the typical I-V behaviour of Josephson tunnel junctions as expected. The compatibility of this process with several thin film deposition techniques, evaporation as well as sputtering, extremely small parasitic capacitances and excellent integrability promise interesting applications in both single-charge electronics and Josephson physics.

1. INTRODUCTION

For purposes of single-charge electronics high-ohmic tunnel junctions of an extremely small capacitance are required. These properties connected with cooling down the samples to very low temperatures guarantee a satisfactory suppression of fluctuations masking the tunneling of charge carriers one by one: i.e. of thermal fluctuations ($e^2/2C \gg k_B T$, i.e. $C \leq 10^{-15} \text{F}$ for circuits usually operated at $T \approx 20 \text{mK}$ in dilution refrigerators) as well as quantum fluctuations ($R_T \gg R_Q \approx 25.6 \text{k}\Omega$).^{1,2} To observe basic single-charge phenomena like the Coulomb blockade one has to connect one junction in series with at least one further junction or a high-ohmic resistor in order to exclude the influence of the low-impedance source. For SET applications arrays up to a large number of junctions are required paying attention to the minimization of island electrodes between neighbouring junctions for decreasing their intrinsic capacitances. The self-aligned in-line conception presented in this paper makes it possible to fabricate submicron tunnel junctions fulfilling the conditions mentioned above in a relatively simple and well reproducible way.

2. FABRICATION PROCESS

2.1 Description of the SAIL technology

The SAIL technology we applied to the sample preparation using the material systems Al/AlO_x/Al and Nb/NbO_x/PbAuIn comprises the following steps:

- 1) sputter deposition or evaporation of a thin metallic film (see Fig. 1a),
- 2) generation of a narrow resist strip (Fig. 1b),

- 3) etching of the metal layer and subsequent removal of the resist (Fig. 1c),
- 4) generation of an extended resist edge (in case of single junctions) or of a system of resist stripes (in case of series arrays), respectively (Fig. 1d),
- 5) anisotropic etching (Fig. 1e),
- 6) oxidation of the edges (Fig. 1f),
- 7) deposition of a second metallic film (thickness comparable to the one of the first metallic layer) (Fig. 1g),
- 8) lift-off process (Fig. 1h),
- 9) generation of a resist strip on top of the narrow stripline and the second metallic layer (its width should be slightly larger than the one of the first metallic stripline in order to cover that totally; Fig. 1i),
- 10) final patterning by dry etching (Fig. 1k).

The steps 5) to 7) can be carried out without interruption of the vacuum cycle.

2.2 Properties of SAIL junctions

Fig. 1: SAIL process

The basic idea of the conception described above is similar to that of a technology applied by Houwman et al.³ to the fabrication of Josephson junctions (Nb electrodes and barriers of NbO_x , $\alpha\text{-Si}$ or Si_xN_y), which has been firstly described by Koch⁴. Differing from this technique we substitute the lift-off process for lateral patterning by anisotropic etching, e.g. ion beam milling. In our opinion this change is advantageous in case of extremely narrow lateral structures ($<100\text{nm}$ as desirable for applications in single-charge electronics) because of the clearly increased aspect ratio.

By the help of self-alignment the technologically caused overlaps (cf. e.g. edge-type junctions presented by Broom et al.⁵ or Kleinsasser et al.⁶) acting as parasitic capacitances become avoidable. The in-line geometry ensures the minimization of the island electrode between two neighbouring junctions and makes it easy to integrate junctions in series arrays as frequently necessary in single-charge electronics.

The area of a junction is determined by the thicknesses of the metallic films (step 1) on the one hand and by the linewidth of the lateral constriction (steps 2 and 3) on the other hand. If e-beam lithography is used, values of 30nm times 50nm should be realizable resulting in areas of at least $<0.002\mu\text{m}^2$. Assuming a dielectric constant of approximately 10 (e.g. AlO_x) and a barrier thickness of 2nm , this corresponds to capacitances of the order 10^{-17}F . In this respect the SAIL technique can compete with technologies applied to the preparation of ultra-small tunnel junctions up to now such as the shadow evaporation technique introduced by Niemeyer⁷ and Dolan⁸ and commonly used in single-charge electronics. Our process has the

advantage of being fully compatible with several thin film deposition techniques, evaporation and sputtering as well.

The size of an island electrode, which has to be reduced as far as possible in order to minimize the intrinsic capacitance, is given by the tunnel area discussed above and by the distance between two barriers following one another in-line. Dimensions down to $(30 \times 50 \times 200) \text{ nm}^3$ should be achievable without difficulties.

We want to emphasize the early lateral constriction of the tunnel area at the beginning of the process (steps 2 and 3) because we apprehend disadvantageous influences of the following process steps on the junction properties. The barrier has to be protected in particular from any interaction with bombarding particles having energies of some hundreds of eV during dry etching. Consequently, the effective oxide barrier is totally covered by resist during the final patterning (steps 9 and 10) in order to prevent affecting adversely the barrier properties by ion beam damage.

3. EXPERIMENTAL INVESTIGATIONS

3.1 Preparation

3.1.1. Material system $\text{Al}/\text{AlO}_x/\text{Al}$

Previous experimental investigations of single-charge phenomena have been carried out mostly using the material system $\text{Al}/\text{AlO}_x/\text{Al}$ the one chosen here as well. We have prepared single junctions and series arrays up to 9 junctions. All fabrication steps except resist processing have been carried out in a high vacuum facility equipped with an ion beam source. For bombarding targets and samples Ar as an inert gas was used. The ion beam was discharged by passing a hot filament after leaving the source in order to prevent damage of the samples by electrical charging-up.

For the sputter deposition of both Al layers (steps 1 and 7) the source was operated at an accelerating voltage of 1kV and a current density of $500 \mu\text{Acm}^{-2}$; for etching the ion beam source has been operated at 0.6kV and $250 \mu\text{Acm}^{-2}$.

To generate AlO_x barriers we have investigated two different methods :

- reactive sputter deposition of AlO_x ,
- Al surface oxidation assisted by neutralized particle impact.

In the first case an Al target was bombarded ($0.6 \text{ kV} / 250 \mu\text{Acm}^{-2}$) in the vacuum chamber containing 20%Ar+80% O_2 at a total pressure of about 10^{-2} Pa . Differing from this, in the latter case the sample instead of a target was bombarded. The ion beam source was operated at its lower limit with respect to the accelerating voltage ($0.1 \text{ kV} / 65 \text{--} 80 \mu\text{Acm}^{-2}$). The vacuum conditions have not been changed.

Both tested processes make it possible to generate junctions of sufficiently large tunnel resistances. It was found, that the oxide growth rate of the first method exceeds the one of the second by approximately one order of magnitude. Taking into consideration the strong dependence of the tunnel resistance on the barrier thickness it becomes obvious that adjusting the resistance becomes more and more difficult with increasing oxide generation rates. Thus we prefer the latter variant.

Present time there was only photolithography used for the preparation of etch masks. That's why the minimum size of tunnel areas is as large as $(30 \times 2000) \text{ nm}^2$.

3.1.2. Material system $\text{Nb}/\text{NbO}_x/\text{PbAuIn}$

Beyond the $\text{Al}/\text{AlO}_x/\text{Al}$ system we have applied the SAIL conception to the preparation of single $\text{Nb}/\text{NbO}_x/\text{PbAuIn}$ Josephson tunnel junctions. This combination is established in the fabrication of SQUIDS^{9,10} and voltage standards¹¹ at the University of Jena. The main differences to the process described in connection with the $\text{Al}/\text{AlO}_x/\text{Al}$ junctions are:

- The Nb electrode deposited first was evaporated under ultra-high vacuum conditions.
- Barrier generation and deposition of the PbAuIn electrode have been carried out in a special vacuum facility reserved for these materials; that's why it was necessary to interrupt the vacuum process after

ion beam milling (step 5). After transfer into the latter facility the samples have been cleaned in an rf plasma of Ar and afterwards oxidized in a plasma containing oxygen. Then the PbAuIn layer was evaporated.

For better comparability with the usually produced window-type Nb/NbO_x/PbAuIn junctions we have fabricated SAIL junctions of relatively large area (approximately $(0.2 \times 5) \mu\text{m}^2$).

3.2 Measurements

3.2.1. Coulomb blockade in Al/AlO_x/Al tunnel junctions connected in series

First indications of having produced tunnel junctions of good quality following the SAIL conception we obtained from I-V characteristics measured at 4.2K in a voltage biased-regime up to 2.5V per junction. Both single junctions and series arrays show a pronounced non-linear behaviour in the current-voltage characteristics (see Fig. 2) as predicted in the theory of metal/insulator/metal tunnel junctions (cf. e.g. Simmons¹², Richter and Seidel¹³). A very useful aid for estimating the tunnel behaviour of Al/AlO_x/Al junctions is the so-called logarithmic conductivity (LC) introduced by Gundlach and Hölzl¹⁴. They investigated the dependence of $d(\ln I_0)/dV$ on the bias voltage V and found a typical shape of curves which is characteristic of the dominance of a tunnel current. The LCs shown in the inset of Fig. 2 are in good accordance with the results of Gundlach and Hölzl.

In the following step we cooled samples down to mK temperatures in order to scrutinize their suitability for single-charge electronics. For that purpose series arrays of 5 SAIL junctions have been used. Area and capacitance of the junctions are roughly estimated to be $0.1 \mu\text{m}^2$ and $5 \times 10^{-15} \text{F}$. The measurements have been carried out in a ³He/⁴He-dilution refrigerator. The superconductivity of the Al electrodes was suppressed by means of a permanent magnet system (cf. Cleland et al.¹⁵). Its magnetic inductance was measured at room temperature to be about 500mT inside the steel yoke exceeding the critical field of bulk aluminium at zero temperature by a factor of 50. We have carried out voltage-biased measurements symmetrically to the ground. The leads (twisted pairs in grease-filled PbSn tubes below and CrNi tubes above 1.3K, respectively) have been filtered at 1.3K.

In the current-voltage characteristic the Coulomb blockade was clearly observed at 14mK as shown in Fig. 3. The series array threshold voltage of approximately $85\text{--}100 \mu\text{V}$ is in good quantitative accordance with the estimated capacitances. Assuming an uniform distribution of capacitances and tunnel resistances within the array the blockade voltage of one junction is $21\text{--}25 \mu\text{V}$ corresponding to an acting capacitance of about $3.5 \times 10^{-15} \text{F}$.

Fig. 2: I-V and LC behaviour of a single junction

Fig. 3: Coulomb blockade at 14mK

3.2.2. Josephson behaviour of self-aligned in-line Nb/NbO_x/PbAuIn tunnel junctions

For single SAIL junctions of Nb/NbO_x/PbAuIn we found the typical I-V behaviour of Josephson junctions (Fig. 4). The critical Josephson current is of the order of 100 μ A corresponding to critical current densities of approximately 10^4 Acm⁻². All measured I-V characteristics are clearly hysteretically. The low normal-state resistances result from adopting the parameters of the barrier generation in standard SQUID technology. However, the barrier generation process is adaptable to applications requiring large resistances (e.g. single-charge electronics) just as requiring low resistances (e.g. SQUIDS).

Fig. 4: Josephson behaviour of a SAIL-junction

4. CONCLUSIONS

In our experiments we have demonstrated the suitability of the SAIL process both for single-charge and Josephson electronics. This fabrication technique offers several technological improvements:

- It opens a rich choice of material systems, sputtered electrodes as well as evaporated ones.
- SAIL junctions are characterized by extremely small parasitic capacitances.
- It is easily possible to connect junctions in series at a very large scale integration level.
- The intrinsic capacitance of island electrodes can be reduced to a minimum.
- Using electron point beam lithography, the reduction of the tunnel area down to less than $0.002 \mu\text{m}^2$ should be realizable.

This latter value corresponds to capacitances below 10^{-16} F. Further reduction of the capacitance makes it possible to increase step by step the temperature which single-charge circuits are operated at.

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