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Low temperature performance of self-aligned "Etched Polysilicon" emitter pseudo-heterojunction bipolar transistors

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Abstract: In this paper we present an investigation of the static performance over the 300K-80K temperature range of pseudo-heterojunction bipolar transistors using an advanced single-polysilicon CMOS compatible self-aligned structure and epitaxial growth for the base and the low doped emitter spacer. These devices exhibit ideal collector currents and non-ideal base currents. By analysing the base leakage current, we have been able to identify the main critical fabrication steps. The bandgap narrowing in the base has been deduced from the temperature dependence of the collector current and the effect of a parasitic boron spike in the base doping profile on the low temperature performance of the transistor has been studied.

1. Introduction

The interest for silicon bipolar transistors operating at liquid nitrogen temperature has grown up due to the development of the BiCMOS technology¹. A well known difficulty in this matter is the decrease of the bipolar transistor current gain with decreasing temperature, which is controlled by the bandgap narrowing difference between the emitter and the base ($\Delta E_g = \Delta E_{ge} - \Delta E_{gb}$, $\Delta E_g > 0$ for conventional devices), the transistor current gain varying as $\exp(-\Delta E_g/kT)$. Advanced epitaxial growth techniques have permitted to introduce a highly doped thin base separated from the highly doped emitter by a low doped "emitter spacer", therefore leading to a negative value for ΔE_g and an increase of the gain with decreasing temperature. The aim of this work was to investigate the static performance over the 300K-80K temperature range of such pseudo-heterojunction bipolar transistors (p-HBTs) fabricated using a self-aligned "etched-polysilicon" emitter technology.

2. Experimental

This work was carried out using our advanced single-polysilicon CMOS compatible self-aligned bipolar structure². In this structure which is very similar to a PMOS device without gate oxide, the emitter region is defined by polysilicon dry etching and the emitter-base junction area is walled by the locos along one direction and bounded along the other direction by PECVD SiO₂ sidewall spacers (Fig. 1). The process technology was derived from the CNET/CNS 0.7/0.5 μm flow charts (Fig. 2). The epitaxial layers were grown by a combination of rapid thermal processing and chemical vapor deposition (RT-CVD) in a 4 inch single-wafer reactor (Jipelec-FUV4) that employs radiant energy and operates at reduced pressure (~ 1 Torr). The machine and experimental details have been described elsewhere³. After locos isolation and gate oxide removal, the silicon wafers were chemically cleaned prior to loading and subsequently hydrogen baked in-situ at 1020°C for 30s. The p⁺ silicon bases were grown using silane and

diborane in a hydrogen carrier gas at 900°C, yielding a nominal growth rate around 150nm/min. The n⁻ silicon emitters were grown at 800°C and using phosphine as the n-type doping gas, yielding a nominal growth rate around 130nm/min . A TEM cross-section of the bipolar device along the emitter length is given in fig. 1c. One can see that the epitaxy is selective over the first 1000Å and exhibits facets at the locos edge. In order to prevent emitter/collector shorts, a conventional base was implanted along the locos edges prior to the epitaxial growth.

Fig. 1: a) Transistor Layout

b) Schematic cross-section along w_E

c) TEM cross section along L_E

Fig. 2: Process flow chart

The targeted structure was a 300Å 10¹⁹ cm⁻³ boron doped base and a 1000Å thick 10¹⁸ cm⁻³ phosphorus doped emitter spacer. Considering a collector doping level of 3 10¹⁶ cm⁻³ at the base/collector junction, the base width measured on the SIMS profile after epitaxy (Fig. 3a) is ~ 600Å. On some samples a large boron spike was observed (2-6 10¹⁷ cm⁻³) increasing the base thickness to 1300Å (Fig. 3b). Modifications in the deposition process have allowed to suppress this parasitic spike.

Once fully processed, the transistors were characterized electrically at different temperatures using a CT105 Cryotest probe station, which allows statistical testing of the wafers over the 400K-77K temperature range.

Fig. 3: SIMS profiles of the epitaxial structure for p-HBTs with (a) or without (b) a boron spike in the base

3. Results

3.1 Analysis of non ideal base currents

Fig. 4 shows Gummel plots recorded at 300K for walled and non-walled p-HBTs. For all the devices the collector current behaviour is ideal while large abnormal base currents are observed in the case of walled devices. A detailed analysis of the dependence of the leakage currents on device geometry and process parameters⁴ shows that these currents originate from the emitter-base junction along the locos edge. They are caused by the emitter-base space charge region being located within the polysilicon or at the polysilicon/silicon interface along the locos edge, as the selectivity of the epitaxial growth leads to a polysilicon emitter thicker, thus less doped, over the locos edge than over the rest of the active area. The use of in-situ doped polysilicon would suppress this problem by providing a uniform dopant distribution without raising the thermal budget. Analysis of the remaining base leakage current for non-walled devices as a function of the device perimeter-to-area ratio shows that this current originates from the emitter-base junction along the PECVD SiO₂ sidewall spacers⁴.

Fig. 4: Gummel plots for walled and non walled p-HBTs

In order to get a deeper insight into the physical mechanisms involved, the base leakage current was fitted as $I_{b\text{leak}} = I_{b\text{leak},0} \exp(qV_{be}/\eta kT)$ for walled and non-walled p-HBTs. As can be seen on fig. 5, over the 300K-200K range, $I_{b\text{leak},0}$ obeys an Arrhenius law of the form $[A \exp(-E_a/kT)]$ typical of a generation-recombination current. The activation energy E_a was found to be equal to 0.3eV for the parasitic current originating from the emitter-base junction along the locos edge, and equal to 0.43eV for the parasitic current originating from the emitter-base junction along the PECVD SiO₂ sidewall spacers.

Fig. 5: $I_{b\text{leak},0}$ versus $1/T$ for walled (a) and non-walled (b) p-HBTs

3.2 Extraction of the bandgap narrowing in the base

Gummel plots recorded at 300K and 80K for non-walled p-HBTs are given in fig. 6. The collector current is ideal over the whole temperature range.

Fig. 6: Gummel plots for non-walled p-HBTs at 300K and 80K

The bandgap narrowing in the base was extracted from the temperature dependence of the collector current using the method developed by P.Ashburn et al.⁵. As shown on fig. 7, for p-HBTs with no parasitic boron spike in the base, a linear characteristic is obtained giving a bandgap narrowing of 41meV which compares well with a theoretical value of 54.6meV from the bandgap narrowing model of Klaassen⁶, considering an average base doping of $6.5 \cdot 10^{18} \text{ cm}^{-3}$. When a parasitic boron spike is present, the characteristic is not linear and two different values of the bandgap narrowing can be extracted: 43 meV

for $T > 150\text{K}$ and 32.4meV for $T < 150\text{K}$, which shows that the contribution of this added profile tail becomes dominant at low temperature, as observed previously in the case of bipolar transistors with a boron implanted base⁷.

Fig. 7: Extraction of the bandgap narrowing in the base for p-HBTs without (a) and with (b) a parasitic boron spike in the base

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