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Si vertical JFET at low temperatures; I-V characteristics and low frequency noise

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Abstract: Measurements of the source to drain current/voltage, $I_d(V_{ds})$, characteristics and low frequency ($f < 100\text{kHz}$) noise spectral density function, $S_V(f)$, were carried out at $77\text{K} < T < 300\text{K}$ on the vertical JFET (BiCMOS-compatible technology). We found that $I_d(V_{ds})$ characteristics do not significantly depend on T , down to 100K , thus low temperature applications of the device are plausible. At $f < 10\text{kHz}$, $S_V(f)$ was found to be dominated by the $1/f$ component. At low T , $S_V(f)$ shows features characteristic for the generation-recombination process, which become stronger at large and negative gate bias polarizations. This suggests that the recombination centers are localized at the interface between the channel and the depletion region near the gate.

1. THE VERTICAL JFET

The vertical junction field effect transistor (V-JFET) is derived from the pMOS structure by a simple removal of the oxide before depositing the polysilicon gate. The polysilicon layer (n^{++} doped by implantation) plays then the role of the source, the p^+ regions, located around the polysilicon, form the JFET's gate, and the n^+ substrate, the drain [1]. This structure bears a striking resemblance to a vacuum triode, with the electrons traversing vertically the n -region (channel) between depletion regions encircling the gate electrodes, whose spatial extension affects the source-drain current, I_d . Because the conductivity, σ , of channel Si is kept high, the V-JFET functions at microwave frequencies [1]. The device was expected to remain operational at low temperatures (LT), because (i) it contains no elements restraining *a priori* its LT performance, with σ remaining appreciable down to about 50K , (ii) its operation principle is similar to that of the FET, known to be an acceptable LT device. The results of this paper confirm that prediction. We also present low frequency (LF) noise characteristics of the V-JFET at LT.

2. STATIC CHARACTERISTICS

The devices we tested have been fabricated at the Centre National d'Etudes des Télécommunications-Meylan, by the process derived from the BiCMOS technology [1-3]. They have a p^+ -type, implanted gate, isolated by SiO_2 spacers from the polysilicon source, and the active area equal to $2 \times (0.7 \times 1.4) \mu\text{m}^2$.

Figure 1. Characteristics of the V-JFET.

I_D versus V_{DS} for various of gate voltages, V_{GS} . The data taken at temperatures marked in the drawings.

Room temperature (RT) characteristics of the device have been discussed in former publications [1-4]. The source-drain current, I_d , dependence on V_{ds} at various gate voltages, V_{gs} , measured at 300K, 200K, 150K, and 100K are presented in Fig. 1. The absence of significant changes in the characteristics, as T is lowered from 300K to 100K, should be emphasized, as being of prime importance for the LT applications of the device. A closer inspection of the characteristics shows that I_d , at fixed V_{ds} and V_{gs} , varies within about a 10% margin. I_{ds} is seen to increase at first; it passes through a maximum at about 150K and subsequently falls, approaching the RT value at 100K. This effect is tractable to the temperature variation of the conductivity, σ , in lightly doped n-type Si, if we assume that the gate depletion regions are not significantly affected by the temperature variation. It is known (cf. e.g. [5]) that at donor concentrations of the order of 10^{16}cm^{-3} (typical for the channel doping of the devices we measured) σ in a non-monotonic function of T . It increases at $300\text{K} < T < 200\text{K}$, due to a reduction of phonon scattering, and then falls, approaching an exponential dependence at sufficiently low T , (carrier freeze-out). Let us note that the current in the V-JFET shows a non-monotonic behavior, similar to that of $\sigma(T)$, in the region of T we explored. It is worthwhile to remark at this point that the device performance below 100K can be inferred from the behavior of $\sigma(T)$. The V-JFET performance is expected to degrade at $T < 50\text{K}$, where both the carrier freeze out and the onset of scattering on ionized impurities strongly reduce σ .

Figure 2. Evolution of the spectral density of the input generator noise voltage *versus* frequency. Measurements taken at room temperature with $V_{ds}=4\text{V}$ and $V_{gs}=0$.

3. LF NOISE MEASUREMENTS

The spectral density function $S_V(f)$ was measured at 300K and 77K at frequencies, f , in the range $250\text{Hz} < f < 100\text{kHz}$. The experimental set-up has been described elsewhere [6]. The noise is expressed in terms of the voltage generated by the equivalent source placed at the input, with the gate load of 50Ω . The current noise effects are disregarded, as at $f < 100\text{MHz}$ they are known to be negligible for the operation of the field-effect device, especially at the 50Ω impedance. The device was tested in a 50Ω -matched microstrip chip carrier that could be immersed in the liquid N_2 . The noise measurements have been taken on devices fabricated as described above, with a bigger active area (dimensions, $0.7 \times 12 \mu\text{m}^2$).

The RT frequency dependence of $S_V(f)$ is shown Fig. 2, for $V_{ds} = 4V$ and $V_{gs}=0$. Below 10kHz the preponderant noise is that of the $1/f$ type. We attribute the upward shift of the data points above the $1/f$ dependence, visible at $f > 10kHz$ to the generation-recombination (G-R) noise source in the device. The data are fitted with a standard function using a noise decomposition into the $1/f$ and the G-R constituents,

$$S_V(f) = A/f + (C_0/f_0)/[1 + (f/f_0)^2] \quad (1)$$

where $A=8.8 \times 10^{-10} \text{ V}^2/\text{Hz}$, C_0 is the $f=0$ plateau value, and f_0 the characteristic frequency of the G-R noise source, expressible through the trap time constant, $\tau_0=1/(2\pi f_0)$.

Figure 3. Spectral density of the input noise voltage measured at 77K at $V_{ds} = 4V$ and four different V_{gs} values, equal to $-1V$ (Δ), $-0.5V$ ($\times$), 0 ($\diamond$), and 0.5 ($\star$).

The LF noise data taken at 77K are presented in Fig. 3, for various gate polarizations. An overall upward shift of the noise level at LT is readily seen, combined with a bowing of the data curve below the $1/f$ line at both the high and low frequency limit. This feature stems from the displacement of the G-R component of the noise, from about 10kHz (Fig. 2) towards about 2kHz at 77K, due to the increase in the trapping time constant, τ_0 . The value of τ_0 at 77K can be read out from the plot in Fig. 4, showing the product $f \cdot S_V(f)$ as a function of $\log_{10} f$, for $100\text{Hz} < f < 100\text{kHz}$. The second term in Eq. (1) takes then a form of a Lorentzian line, centered at $f_0=1/(2\pi\tau_0)$. If the trapping process is activated, and E_a denotes the activation energy,

$$\tau_0 \propto T^{-2} \exp(E_a/kT). \quad (2)$$

Measurements of the temperature dependence of τ_0 , permitting to determine E_a , are under way.

Figure 4. The product $f \cdot S_V(f)$ plotted *versus* $\log_{10} f$.

The maximum of the function, located near 2kHz gives τ_0 of about 80 μ s.

Finally, an attempt was made to locate the G-R source in the device. In order to do that we measured $S_V(f)$, varying V_{gs} , at V_{ds} constant and equal to 4V. The results, shown in Fig. 3 indicate that the LF noise level is higher at higher and negative values of V_{gs} . As at large and negative values of V_{gs} the interface area between the channel and the depletion regions surrounding the gate is larger, it is likely that the G-R noise source is located there.

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