Low temperature CMOS-compatible JFET's

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Abstract: JFETs used as input transistors for CMOS preamplifiers can improve the input sensitivity due to their lower $1/f$ noise. Cryogenic JFET's can be realized by increasing the channel doping concentration to prevent carrier freeze-out. This paper deals with the properties of fabricated cryogenic, CMOS compatible JFET's. Process parameters for a cryogenic JFET technology are presented. Static measurements of these JFET's between room temperature and 4 K made it possible to extract JFET model parameters V_p and β for circuit simulations. These measurement results are compared with the temperature dependence of mobility and ionisation.

Noise parameters could be measured at different temperatures with various geometries and doping levels of JFET's.

1 INTRODUCTION

Infrared detectors, sensors in space and basic physical research experiments operate at very low temperatures [1]. It is convenient to minimize signal loss by placing signal processing electronics operated at low temperatures near the sensors. Cryogenic CMOS-technologies were developed to satisfy these needs [2,3]. Problems for small signal detectors arise due to the $1/f$ noise level of CMOS-preamplifiers. Since JFET's show lower $1/f$ noise than CMOS devices it should be possible to use JFETs to improve circuit performance.

At low temperatures JFET's show carrier freeze-out of the channel doping. This can be overcome. Measurements and theory show lower carrier freeze-out with higher channel doping concentrations, as the ionization energy depends on the doping concentration [4]. An equation for the ionization energy is given by [5]:

$$E_a = 0.0438\text{eV} - 4.08 \cdot 10^{-8}\text{eVcm} (N_A)^{\frac{1}{3}} \quad (1)$$

Increasing the channel doping concentration N_A to $1 \cdot 10^{18}\text{cm}^{-3}$ minimizes the ionization energy E_a . No carrier freeze-out at lower temperatures will occur. Special CMOS-compatible JFET's for low-temperature operation can be fabricated [6].

2 PROCESS PARAMETERS

Process parameters can be determined if channel doping concentration N_A and channel depth a is known. A breakdown voltage of 10 volts limits the maximum channel doping. To achieve a reasonable pinch-off voltage V_P it is necessary to realize a small channel depth a .

$$V_P = \frac{qN_A a^2}{2\epsilon_s} \quad (2)$$

q is the charge of an electron and ϵ_s the dielectric constant of silicon. A channel doping of $1 \cdot 10^{18} \text{ cm}^{-3}$ and a pinch-off-voltage of 1 V leads to a channel depth of 35nm.

Figure 1: Doping profile

Figure 2: Crosssection and geometry of JFET's

CMOS-technology provides drain and source implants which can be used for the gate of the JFET. An additional channel implantation is necessary to control the electrical parameters of the JFET. Process parameters for the channel implantation could be found by ICECREM and SPICES simulations. To achieve a maximum channel doping with a small channel depth, gate and channel should be implanted with a minimal implantation energy and a short annealing time. The resulting doping profile is shown in figure 1. A 90 nm stray oxide was deposited by dry oxidation. A dose of $1 \cdot 10^{15} \text{ cm}^{-2}$ phosphorus was implanted with 70 keV for the gate. The channel was realized by implanting $2 \cdot 10^{14} \text{ cm}^{-2}$ boron with 40 keV. Annealing at 900°C for 20 min activated the dopants.

To develop cryogenic JFET's a test chip was designed. Figure 2 shows a crosssection and three basic layouts of the JFET's. An ring-JFET, where the drain is surrounded by gate and by source brings the advantage of a small gate input capacitance. A checkboard structure provides a large width W with a minimum area needed for the transistor. Also a simple standard design was made. The n-well of a standard CMOS-process forms the isolation and the second gate of the ring-JFET. These designs were realized with different W/L ratios, to compare the dependence between electrical properties and layout.

3 THEORIE AND MEASUREMENTS

A simple JFET-model includes the threshold-voltage V_{TO} , the transconductance β and the output conductance λ .

$$I_{DS} = \begin{cases} 0 & : V_{GS} - V_{TO} \geq 0 \\ \beta (V_{GS} - V_{TO})^2 (1 + \lambda \cdot V_{DS}) & : 0 > V_{DS} > V_{GS} - V_{TO} \\ \beta V_{DS} [2(V_{GS} - V_{TO}) - V_{DS}] (1 + \lambda \cdot V_{DS}) & : 0 > V_{GS} - V_{TO} \geq V_{DS} \end{cases} \quad (3)$$

where

$$\beta = \frac{I_p}{V_p^2} = \frac{q^2 \mu_p N_A^2 W a^3}{\epsilon_s L} \left(\frac{2\epsilon_s}{q N_A a^2} \right)^2 = \frac{4W \mu_p \epsilon_s}{aL} \quad \text{and} \quad V_{TO} = V_{bi} - V_p = V_{bi} - \frac{q N_A a^2}{2\epsilon_s} \quad (4)$$

The temperature dependence of ionized dopants N_A , mobility μ_p and build-in-voltage V_{bi} determine the temperature behaviour of the model parameters β and V_{TO} .

Lengeler shows in [7] the equations for the number of free electrons and the fermi level. Similar expressions can be found for holes.

freeze-out region
compensated

extrinsic
region

intrinsic
region

$$N_D \geq N_A \geq \frac{1}{2} N_C e^{-\frac{E_C - E_D}{kT}}$$

$$kT > \frac{E_C - E_D}{\ln \left(\sqrt{\frac{N_C}{2N_A}} \frac{N_D - N_A}{N_A} \right)}$$

$$n = \frac{N_D - N_A}{2N_A} N_C e^{-\frac{E_C - E_D}{kT}}$$

$$kT < \frac{E_C - E_D}{\ln \frac{N_C}{2N_D}}$$

$$n = \sqrt{\frac{N_D N_C}{2}} e^{-\frac{E_C - E_D}{2kT}}$$

$$\frac{E_C - E_D}{\ln \frac{N_C}{2N_D}} < kT < \frac{E_C - E_V}{\ln \frac{N_C N_V}{N_D^2}} \quad \frac{E_C - E_V}{\ln \frac{N_C N_V}{N_D^2}} < kT$$

$$n = N_D$$

$$n = n_i$$

$$E_F = E_C - E_D + kT \ln \frac{N_D - N_A}{2N_A}$$

$$E_F = E_C - \frac{E_D}{2} + \frac{kT}{2} \ln \frac{N_D}{2N_C}$$

$$E_F = E_C + kT \ln \frac{N_D}{N_C}$$

$$E_F = E_{Fi} \quad (5)$$

N_C and N_V are the effective density of states. Figure 3 shows the calculated temperature dependence of the number of free carriers. At high doping concentration the number of free carriers is proportional to $T^{\frac{3}{2}}$. Lower doping concentrations lead to a steep decrease of free carriers with lower temperatures.

Figure 3: Ionized dopants

Figure 4: Mobility μ_p

Dorkel and Leturcq developed in [8] an model of the mobility μ_p . Results of the modeling are shown in figure 4. The mobility has a maximum. The position of the maximum depends on the

doping concentration. Higher doping concentrations shift the maximum to higher temperatures. Carrier concentration and mobility are compared with the behavior of β and V_{TO} . Transfer and output characteristics at different temperatures of the above mentioned transistors provided the database for automated model parameter extraction of β and V_{TO} (figure 5). β decreases from room temperature to 4 K by a factor of 10000, but there is still a voltage amplification of about 10 at 4 K. This behavior can be basically explained by the decrease of the number of free carriers. Lower channel concentrations due to the gaussian doping profile in the channel, lead to carrier freeze-out in the lower doped region of the channel and reduce the channel depth a . It is difficult to calculate the physical model parameters. A mathematical approach was chosen.

$$\beta = \left(\frac{3.84 \frac{pA}{V^2 K}}{T^{-5.5} + 2.25 p K^{-1} T^{86.5m}} + 23.3 \mu \frac{A}{V^2 K} T \right) \frac{W}{L} \quad (6)$$

The derivation of the modelling to measurements is less than 10 percent.

Figure 5: Temperature dependence of V_p and β

Figure 6: Temperature dependence of V_p and V_{bi}

Threshold voltage V_{TO} has two components: pinch-off-voltage V_P , due to the dopants in the space charge region, and the built-in-voltage V_{bi} , due to the different doping concentrations in the channel and the gate. V_{bi} increases and V_P decreases with lower temperatures. Since it is difficult to determine the correct doping density N_A and channel depth a a mathematical model was chosen.

$$V_{TO} = -97mV \cdot (T K^{-1})^{0.476} - 78.5mV (T K^{-1})^{-0.57} \quad (7)$$

Figure 7 shows some measured and modeled transfer characteristics at different temperatures. The agreement is quiet good.

Figure 7: Transfer characteristics at different temperatures

4 NOISE MEASUREMENTS

Noise measurements with three different cryogenic JFET's were made (table 1).

T [K]	W/L	$\overline{i_{DS}}(1\text{Hz})$ [dBA/ $\sqrt{\text{Hz}}$]	I_{DS} [A]	K_F [A]	g_m [S]	A_F [V ²]	$\overline{e_n}(1\text{Hz})$ [V/ $\sqrt{\text{Hz}}$]
293	40/4	-201	300n	$2.6 \cdot 10^{-14}$	6.7μ	$1.8 \cdot 10^{-10}$	13μ
293	40/4	-185	10μ	$3.1 \cdot 10^{-14}$	75μ	$5.6 \cdot 10^{-11}$	7.5μ
293	40/4	-178	100μ	$1.6 \cdot 10^{-14}$	250μ	$2.5 \cdot 10^{-11}$	5μ
293	20/4	-178	100μ	$1.6 \cdot 10^{-14}$	125μ	$1.0 \cdot 10^{-10}$	10μ
293	20/4	-188	10μ	$1.6 \cdot 10^{-14}$	44μ	$8.2 \cdot 10^{-11}$	9μ
77	40/4	-228	1μ	$1.6 \cdot 10^{-17}$	6μ	$4.4 \cdot 10^{-13}$	664n
77	40/4	-214	3μ	$1.3 \cdot 10^{-16}$	11μ	$3.3 \cdot 10^{-12}$	1.8μ
77	2425/5	-188	100μ	$1.5 \cdot 10^{-15}$	436μ	$8.3 \cdot 10^{-13}$	913n
77	2425/5	-191	30μ	$2.6 \cdot 10^{-15}$	196μ	$2.1 \cdot 10^{-12}$	1.4μ
77	2425/5	-193	3μ	$1.7 \cdot 10^{-14}$	42μ	$2.8 \cdot 10^{-11}$	5.3μ
77	2425/5	-190	1μ	$1.0 \cdot 10^{-13}$	19μ	$2.7 \cdot 10^{-10}$	16μ
4	40/4	-230	30n	$3.3 \cdot 10^{-16}$	57n	$3.1 \cdot 10^{-9}$	55μ
4	2425/5	-212	226n	$2.8 \cdot 10^{-15}$	410n	$3.9 \cdot 10^{-9}$	62μ
4	2425/5	-228	30n	$5.2 \cdot 10^{-16}$	97n	$1.6 \cdot 10^{-9}$	40μ

Table 1: Noise parameters of cryogenic p-channel JFETs for different temperatures

The equivalent input voltage $\overline{e_n}$ decreases with a higher current I_{DS} . $\overline{e_n}$ is very high for these JFET's and equal compared to MOSFET's. At 77 K the noise decreases and the noise data at 77 K show nearly no dependence on W and L. Detailed measurements showed high gate leakage currents. Noise measurements on a chip with a lower channel doping concentration showed also such high noise levels. Probably problems with the fabrication process lead to high leakage currents, due to the metallization process.

5 CONCLUSION

A special fabrication process leads to CMOS compatible JFET's. Normal operation at cryogenic temperatures was measured. Mathematical model parameters for β and V_{TO} could be obtained. Noise levels of fabricated devices were comparable to CMOS devices, due to high reverse gate-drain currents. A different metallization process with a diffusion barrier will probably overcome this problem. A new batch of chips is currently under fabrication.

6 LITERATURE

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