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Hot carrier effects in sub-0.1 μm gate length MOSFETs between room and liquid helium temperatures

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Abstract: The variations of the substrate current and the impact ionization rate in MOS transistors are investigated as a function of channel length and temperature. It is shown that, although a significant enhancement of hot carrier effects is observed by scaling down the devices, a strong reduction of the impact ionization rate is obtained for sub-0.1 μm MOSFETs operated at liquid nitrogen temperature in the low drain voltage range. A thorough study of the electrical properties of these deep submicron devices allows us to gain insight in the physical mechanisms involved in the hot carrier transport in a wide temperature range.

1. INTRODUCTION

Low temperature operation is a very good candidate to improve substantially the performances of deep submicron MOS devices, due to a number of advantages, such as, increase of carrier velocity, reduction of the subthreshold swing, decrease of short channel effects, improvement of thermal conductivity, lower interconnect resistance and latch-up immunity [1]. However, the reduction of temperature is supposed to enhance hot carrier effects. Recent studies have shown that the impact ionization rate is almost independent of temperature [2], or decrease as the temperature is reduced for small drain voltages [3-9]. Moreover, it is not clear if this improvement of hot carrier effects in the low drain voltage range is larger for long or short channel devices [3-6]. Furthermore, some contradictory results have been presented for the dependence of the impact ionization rate as a function of channel length [4,10,11]. An increase or a decrease of this rate has been found in these works by reducing the channel length.

Therefore, it is very valuable to study the hot carrier effects as a function of temperature and channel length in the deep submicron range. We show in this paper the substrate current and impact ionization rate variations for ultra-short channel devices between room and liquid helium temperatures. This detailed study allows us to show the performances of sub-0.1 μm MOSFETs and to gain insight in the physical mechanisms involved in the hot carrier phenomena in a wide temperature range.

2. RESULTS AND DISCUSSION

LDD MOSFETs with gate length ranging from 0.5 to 0.07 μm , fabricated according to a conventional NMOS process in conjunction with a direct write EB lithography and a two step ECR plasma etching, are studied in this work. Poly-Si side wall spacers have been used for these devices. The gate oxide thickness is 50 Å. Further details for the fabrication of these MOS transistors can be found in [10].

Figs. 1a-b show the variations of the maximum substrate current for these very short channel bulk Si LDD MOSFETs. It is clear in these figures that the maximum substrate current $I_{b\text{max}}$ significantly increases by reducing L_g for high (1.8 V) and low (1.5 V) drain voltages. These V_d values have been chosen in order to reduce the kink effect which prevents to measure the substrate current at high drain voltage [3, 12] and to obtain very accurate results at low drain voltage. Moreover, 1.5 V can become a very useful bias in the

sub-0.1 μm gate length range. When the temperature is reduced $I_{b\text{max}}$ is significantly decreased. This reduction is smaller for the shortest devices for both V_d values, and is amplified for the lowest drain voltage for a given channel length. Moreover, with decreasing the gate length, the increase of $I_{b\text{max}}$ is stronger at low temperature. Finally, for a given temperature, the enhancement of $I_{b\text{max}}$ when L_g is reduced is roughly independent of drain voltage. Nevertheless, these features are very useful in order to predict device degradation, but do not reflect the behavior of hot carriers due to the variation of the drain current with temperature and channel length.

Therefore, we have plotted in fig. 2 the dependence of the impact ionization rate M_{max} in the maximum substrate current condition ($I_{b\text{max}}/I_d$). For high drain voltage ($V_d=1.8$ V), M_{max} increases with reducing the gate length whatever the temperature is. However, the enhancement of the ionization rate is very small compared with the variation of $I_{b\text{max}}$ (Fig. 1). As in the maximum substrate current variations, the increase of M_{max} is larger at low temperature for which a smaller ionization rate is always obtained compared with 300 K, and the reduction at low temperature is stronger for long channel MOSFETs. In the case of lower drain voltage ($V_d=1.5$ V), a minimum is obtained for the $M_{\text{max}}(L_g)$ curves in the 0.1-0.3 μm range, this feature being amplified for low temperature operation. As exemplified in Fig. 2b, the impact ionization rate in the sub-0.1 μm channel length range is almost the same as that for long channel (0.5 μm) devices. Therefore, it seems that in the low drain voltage region, hot carrier effects will not be so harmful even for sub-0.1 μm MOSFET's. A similar variation for the impact ionization rate as a function of L_g , with a minimum on the I_b/I_d curve, has also been recently shown at 300 K [13].

However, Figure 3 presents the results of the variations of the impact ionization rate M for a constant (V_g-V_t) value for all the studied temperatures and gate lengths. In these plots, unlike for the M_{max} variations, M is enhanced when L_g is reduced, even for low drain voltage and low temperature operation. This analysis allows us to gain insight in the physical mechanisms involved in the impact ionization processes, because in this case, M is compared for a given (V_g-V_t) which leads to a constant inversion charge. At high drain bias ($V_d=1.8$ V, Fig. 3a), the increase of M when L_g is reduced is stronger at low temperature, but the low temperature values are always smaller than the 300 K ones. For long channels, the decrease of M for a lower temperature is almost the same for both V_d values. However, for very short channels (≤ 0.2 μm), the reduction of M is higher in the low drain voltage regime. Furthermore, at $V_d=1.5$ V (Fig. 3b), a stronger decrease is obtained at low temperature for the shortest devices. Moreover, the enhancement of M when L_g is reduced, is smaller at low temperature (77 K for instance) compared with room temperature.

These significant differences between the behaviors of M and M_{max} are attributed to the dependence of the gate voltage for which I_b is maximum as a function of gate length and temperature. In fig. 4 are shown the variations of the substrate current with gate voltage as a function of V_d for 300 K and 77 K in the case of a 0.07 μm device. As exemplified in fig. 4a for 300K, the substrate current peak is obtained for a V_g value ($V_{g\text{max}}$) which is almost independent of drain voltage, unlike for long channel MOSFETs for which a strong decrease of $V_{g\text{max}}$ is obtained by reducing V_d . On the other hand, at 77 K (Fig. 4b), $V_{g\text{max}}$ substantially increases when V_d is reduced. These features can be understood in figure 5 which presents the variations of M with V_g . It is clear that M shows the most gentle slope with V_g for low V_d and at low temperature. This behavior is also exemplified in Fig. 6, which shows the substrate current variations for a 0.1 μm and a 0.5 μm devices as a function of temperature in the case of a low drain voltage. For the 0.5 μm MOSFET, the dependence of $V_{g\text{max}}$ on temperature is very low, unlike the case of the 0.1 μm MOSFET for which a strong increase of $V_{g\text{max}}$ is observed at low temperature. The comparison of the $M(V_g)$ characteristics as a function of channel length (Fig. 7) shows that, at very low temperature, the slope of the curve for a very short transistor (0.07 μm) is substantially lower than that of a long transistor (0.5 μm). These original features explain the shift of $V_{g\text{max}}$ for higher gate voltage values when the drain bias is reduced at very low temperature. Moreover, it is also worth noticing that I_{submax} is obtained for a V_g value which can be very high compared with V_d , in particular at very low temperature and for low V_d values, which is very different from the conventional $V_g=V_d/2$ value obtained for long channel MOSFETs. This behavior will be very important for the aging conditions of sub-0.1 μm devices.

On the other hand, it is worth noticing that a hump is observed in the $M(V_g)$ characteristics at low gate voltages for the 0.07 μm device (Fig. 7). This hump is due to the accumulation of the LDD regions when V_g is increased due to the fringing field effects associated with the polysilicon spacers. In fact, the

influence of the source-drain series resistance R_{SD} is very high for sub-0.1 μm MOS transistors, even at 300K with no impurity freeze-out in the LDD's, and R_{SD} is substantially reduced when the LDD regions are accumulated. This effect induces an increase of the effective drain voltage and, therefore, an enhancement of the impact ionization rate. This behavior can also be seen of the transfer $I_d(V_g)$ characteristics [14]. It should also be noted that this effect cannot be seen for the 0.07 μm device of Fig. 5 due to important short channel effects in this case, associated with a smaller effective channel length. A higher drain leakage current is thus obtained, which prevents to observe this phenomenon at low gate voltage. Nevertheless, this device is also very useful in order to measure the substrate current at low temperature for relatively high drain voltages due to a significant reduction of the kink effect [15].

These results are explained in terms of pinch-off length and inversion channel dependences versus gate and drain voltages. In fact, by scaling down the devices, velocity saturation effects are very important, and the inversion channel extends farther from the interface [16] which gives a smaller average potential in the inversion layer close to the drain. This means a lower average V_{dsat} value for given V_d and $(V_g - V_t)$ values. It is also worth noticing that the theoretical pinch-off length in our devices (about 700 Å), given by the conventional equation [17], is higher than the effective channel length for the 0.07 μm gate length MOSFET's (about 300-400 Å). It is clear that the previous models, developed for long channel devices, cannot be applied for these sub-0.1 μm transistors. Therefore, this point can also be very important to explain our data for the shortest devices. These behaviors induce an increase of the electric field and explain the enhancement of the impact ionization rate when the devices are scaled down, and are magnified at low temperature due to the increase of velocity saturation effects. Moreover, it should also be mentioned that the electron mean free path increases when the current flow path is deeper in the substrate [18], which also enhances the multiplication factor. Recent Monte-carlo simulations at 300K have shown that, in order to keep a constant maximum lateral electric field in the MOS transistor, the drain voltage must be reduced in the 0.1 μm channel length range [19], which supports our physical explanations of these ultra-short channel phenomena.

On the other hand, non-stationary effects are significant in our MOSFETs due to the small pinch-off length, even for long channel MOSFETs, associated with the small gate oxide thickness and junction depth, and become larger when the temperature is reduced. For not too high drain voltages ($\leq 2\text{V}$) and electric field, the lower electron energy in the initial energy distribution at low temperature gives rise to a reduction in the number of high energy electrons and thus a decrease of the impact ionization rate. For $V_d = 1.8\text{V}$, the reduction of M is stronger for long channels due to the lower electric field in this case compared with sub-0.1 μm devices. For lower V_d ($V_d = 1.5\text{V}$), the substantial reduction of the electric field compared with $V_d = 1.8\text{V}$, together with the smaller pinch-off length for the shortest devices (limited by the effective channel length), induce a strong reduction in the number of high energy electrons. Therefore, for $V_d = 1.5\text{V}$, although the electric field is higher for sub-0.1 μm devices compared with longer transistors, the best low temperature improvement for the impact ionization rate is observed for the shortest MOSFETs. It should also be mentioned that, for low V_d and high V_g , an additional reduction of the pinch-off length seems to be obtained for these deep submicron devices [20], unlike the case of long channel MOSFETs for which the conventional approach can be applied [17]. This behavior can also contribute to the decrease of M for ultra-short channel devices. At low V_d (1.5 V), a dramatic improvement is thus highlighted for sub-0.1 μm transistors operated at liquid nitrogen temperature.

Furthermore, we have recently shown that the drain current at sufficiently high drain voltage in saturation also substantially increases for these LDD devices in the liquid nitrogen temperature range [14]. Therefore, liquid nitrogen operation seems to be a very good candidate for the optimization of the electrical properties of sub-0.1 μm MOSFETs.

3. CONCLUSION

The variations of the substrate current and the impact ionization rate in MOS transistors have been investigated as a function of channel length and temperature. It has been shown that, although a significant enhancement of hot carrier effects is observed by scaling down the devices, a strong improvement of the impact ionization rate is obtained for sub-0.1 μm MOSFETs operated at liquid nitrogen temperature in the low drain voltage range. In these experimental conditions, the performance enhancement at low temperature is larger for the shortest transistor. A thorough study of the electrical properties of these deep submicron devices allowed us to gain insight in the physical mechanisms involved in the hot carrier transport in a wide temperature range.

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Fig. 1 : Variations of the maximum substrate current as a function of gate length for 300, 200 and 77K; (a) $V_d=1.8V$ and (b) $V_d=1.5V$.

Fig. 2 : Variations of the impact ionization rate in the maximum substrate current condition ($M_{max}=I_{bmax}/I_d$) versus L_g at 300, 200 and 77 K; (a) $V_d=1.8V$ and (b) $V_d=1.5V$.

Fig. 3 : Variations of the impact ionization rate ($M=I_b/I_d$) as a function of L_g for a constant (V_g-V_t) value ($V_g-V_t=1.2V$) at 300, 200 and 77 K; (a) $V_d=1.8V$ and (b) $V_d=1.5V$.

Fig. 4 : Substrate current - gate voltage characteristics for a 0.07 μm MOSFET's at (a) 300K, and (b) 77K.

Fig. 5 : Impact ionization rate versus gate voltage of a 0.07 μm MOSFET's for various temperatures and drain voltages.

Fig. 7 : Impact ionization rate versus gate voltage of 0.07 μm and 0.5 μm MOS transistors for low drain voltage (1.5 V) and various temperatures.

Fig. 6 : Substrate current - gate voltage characteristics as a function of temperature for low drain voltage (1.4V), in the case of (a) 0.1 μm and (b) 0.5 μm MOS devices.