High mobility Si_{1-x}Ge_x PMOS transistors to 5K

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Abstract: P-channel Si_{1-x}Ge_x MOSFETs with peak Ge content $x=0.3$, 0.4 , and 0.5 have been fabricated via MBE and experimentally characterized from room temperature down to 5K. Mobility enhancements relative to identically processed Si controls were largest at the lowest temperatures. The highest mobility measured, $\mu_{FE} = 1622 \text{ cm}^2/\text{V}\cdot\text{sec}$ for the $x=0.3$ SiGe device, was approximately a factor of *four* higher than the mobility of the Si control devices. Peak mobility decreased as the fraction of Ge in the SiGe channel layer increased for the range of concentrations studied here.

1. INTRODUCTION

P-channel Si_{1-x}Ge_x MOSFETs, which feature a Si substrate / Si_{1-x}Ge_x channel / Si cap layer structure, may be especially interesting for low temperature applications due to their high hole mobilities, reduced Si/SiO₂ interface scattering and trapping, and potentially steeper subthreshold slopes as compared to Si surface channel devices. Previous work in the MOS area has concentrated on demonstrating the feasibility of such structures (with Ge fraction $x \leq 0.3$) and reporting mobility results for room temperature operation and perhaps one point in the vicinity of 90K.[1][2][3] Not surprisingly, there has been considerable interest in the SiGe PMOS device, since perhaps this technology might be incorporated into CMOS design, where packing density and circuit speed are limited by the intrinsically poorer PMOS device.

Strained SiGe on unstrained Si results in a favorable Type I band lineup, with 97% of the band offset between the smaller gap SiGe and Si occurring in the valence band.[4] The band alignment is favorable for both cryogenic bipolar and MOS design. A SiGe p-type base is ideal for a Si-based npn heterojunction bipolar transistor, since the valence band offset reduces unwanted hole injection back into the emitter, increasing beta, and allows the use of a heavily doped, low resistance base region, resulting in improved high frequency performance. SiGe HBTs have been mentioned as a possible low temperature technology [5] since with higher base doping, beta degradation due to emitter band-gap narrowing and freezeout in the base may be eliminated. In MOS design, the offset in the valence band of the buried SiGe channel sets up a potential well where holes will first accumulate in the buried SiGe layer, then, as the gate voltage is increased, the holes will accumulate at the top Si/SiO₂ interface. Higher hole mobilities are a result of the combination of band perturbations in the strained SiGe layer which allow most holes to travel with lower effective mass [6] and a reduction of Si/SiO₂ interface scattering since hole transport is subsurface. For the same reason, the noise performance of the buried channel devices should also be superior to straight surface channel devices. Operation at cryogenic temperatures should result in very high "bulk-like" hole mobilities, limited by ionized impurity scattering, and to a lesser degree by Si/SiO₂ interface scattering. In this work, we have investigated the performance of high Ge fraction ($x = 0.3$, 0.4 , and 0.5) Si_{1-x}Ge_x channel PMOS transistors at temperatures as low as 5K.

Fig. 1. (a) Cross-section of SiGe buried channel PMOS device and (b) corresponding energy band diagram (for uniform Ge content in channel) with spacer layer thickness t_{sp} and well thickness t_{well} .

2. SIMULATION

A one-dimensional Poisson solver [7] with Fermi-Dirac statistics was used to simulate the hole density vs. gate voltage over temperature for the various SiGe PMOS structures. Figure 1 shows a cross section of the device structure and the corresponding equilibrium energy band diagram through the channel for a uniform content SiGe layer. Simulated results at 5K for the 75 Å graded Si_{1-x}Ge_x ($x=0$ to $x=0.4$) layer and 75 Å Si cap are shown in Figure 2. Initially, the entire hole density is found in the buried Si_{1-x}Ge_x layer, however, as the gate voltage increases, holes begin to accumulate at the Si/SiO₂ interface as well, effectively screening the gate potential and reducing further increase in buried layer charge. Maximum buried layer hole confinement is expected for high Ge content films, thin Si cap layers, and low operating temperatures.

In addition to increased hole mobilities relative to surface channel Si MOS devices, the buried channel SiGe MOS device offers potentially improved subthreshold slopes at cryogenic temperatures. One factor often cited for degraded Si surface channel MOS subthreshold slopes ($\sim 10X$ ideal value) at 4.2K [8] is that the Fermi level at device turn on is very near the band edge, with its associated high density of interface traps. Increases in gate charge are balanced primarily with increased trap charge instead of inversion charge, and the device turn on is sluggish. However, as Figure 3 illustrates, for the SiGe device the Fermi-level at the top Si/SiO₂ surface is displaced from the band edge high density interface trap region (see inset for Si/SiO₂ interface trap density distribution) into a more "midband"-like region. The Fermi level is farther from than band edge than the 77K Si device, which shows nearly ideal subthreshold behavior. The subthreshold slope should be improved if indeed the Si/SiO₂ interface trap density is the limiting factor.

Fig. 2. Simulated hole density vs. gate voltage of SiGe ($x=0$ to $x=0.4$ graded) over 75 Å, $t_{\text{spacer}}=75$ Å, $t_{\text{ox}}=210$ Å) n⁺ poly gate device at 5K.

Fig. 3. Fermi level energy relative to valence band during turn on for Si and SiGe device ($x=0.3$, $t_{\text{ox}}=210$ Å) with various t_{sp} . Inset shows Si/SiO₂ trap density.

Fig. 4. Measured low and high frequency capacitance voltage curves of n^+ -polysilicon gate SiGe PMOS capacitor ($x = 0$ to 0.5 graded over $60 \text{ \AA}$, $t_{\text{spacer}} = 75 \text{ \AA}$, $t_{\text{ox}} = 210 \text{ \AA}$) at room temperature.

3. DEVICE FABRICATION

SiGe PMOS device design and process flow are fundamentally influenced by limitations imposed by the thermodynamics of strained-layer epitaxy and the need to maintain the strained configuration throughout subsequent device processing. Bean has reviewed [9] the various states in which a strained SiGe film may exist and showed that a range of configurations are possible including the stable, equilibrium state, the metastable state, and the partially relaxed, misfit-dislocation-accommodated state. The stable strain configuration is, of course, the most preferable of these, since, theoretically, the SiGe layers will not relax regardless of the thermal budget employed. However, metastable configurations are often required in order to fully realize the benefits of using SiGe in a given device structure. In this work, we achieve a high concentration of Ge at the critical SiGe/Si interface (50% in the most aggressive sample) while still remaining near to or below the critical thickness for equilibrium strained-layer growth through the use of compositional grading. Nevertheless, care was taken throughout the process to eliminate wafer exposure to temperatures in excess of 750°C , so that SiGe layer relaxation and Ge diffusion could not possibly occur.

The device structures were grown epitaxially via MBE on Si (100) n-type $5 \Omega\text{-cm}$ substrates. MBE growth was carried out in a Perkin-Elmer Si MBE chamber capable of co-depositing Si and Ge from a dual e-beam source onto heated substrates. [10] Once inside the growth chamber, the wafer surface is monitored through the use of in situ reflection high energy electron diffraction (RHEED) for the purpose of observing epilayer crystallinity. Si and Ge material fluxes were calibrated through the use of high resolution x-ray diffraction performed on a $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ strained-layer superlattice. All growths for this work were performed at 550°C and 2×10^{-9} torr. The epitaxial layers were not intentionally doped, however, Hall effect measurements on previous samples determined the background doping to be n-type, at about $1 \times 10^{15}/\text{cm}^3$.

The device structures studied here consist of two microns of Si acting as a buffer layer, followed by the SiGe channel, and a Si cap layer. The three channel designs reported take advantage of the ability of MBE to controllably grow thin, graded Ge content layers. Graded layers were used in order to achieve a high Ge content near the Si/SiO₂ surface, where the valence band offset is most effective, while minimizing the integrated Ge dose to ensure structural stability. The SiGe layers were 1) $100 \text{ \AA}$, $x=0.3$ uniform, 2) $75 \text{ \AA}$, $x=0$ to $x=0.4$ graded, and 3) $60 \text{ \AA}$, $x=0$ to $x=0.5$ graded. Also studied were an MBE silicon control sample and a Si Czochralski (CZ) control. Self-aligned devices were fabricated with a non-LOCOS deposited field oxide at 400°C , a 750°C thermal gate oxidation, an in-situ doped n^+ polysilicon gate deposition at 550°C , and heavily doped implanted (at 77K for full amorphization) BF_2 source/drains. A 1 hour 550°C anneal was used for post-implant regrowth/activation, followed by Al/1% Si metallization, and finally a 400°C 30 minute forming gas anneal. The gate oxide and final Si cap thickness were $210 \text{ \AA}$ and $70 \text{ \AA}$, respectively, as extracted from the measured capacitance-voltage characteristics of Figure 3. Hole confinement in the buried SiGe layer is clearly shown as a plateau in the low frequency sweep.

Fig. 5. (a) Drain characteristics and (b) linear transconductances of annular long channel ($L = 50 \mu\text{m}$) SiGe (same as Fig. 2) vs. Si device at 5 K.

4. EXPERIMENTAL RESULTS

4.1 Test Setup

Upon completion of the fabrication process, device operation was verified via wafer level room temperature testing, and then die were packaged in 68 pin Leadless Chip Carrier packages. Devices were tested through the use of a Lakeshore Electronics MTD-130 Modular Test Dewar cryotest system. The system, which includes a high efficiency single stage continuous flow cryostat, autotuning temperature controller, and silicon diode temperature sensor, allows convenient testing from room temperature down to $T < 10\text{K}$.

4.2 Drain Characteristics and Mobility Extraction

All SiGe channel devices as well as the Si MBE and Si CZ controls were functional at room temperature down to 5K. Figure 5 shows the measured drain characteristics at 5K as well as the I_D - V_G and linear transconductance plots of the SiGe (graded $x=0$ to $x=0.4$) and Si $L = 50 \mu\text{m}$ annular devices. Annular devices were used in order to reduce any unwanted edge leakage effects, especially since room-temperature generation currents were higher in the SiGe devices due to the smaller bandgap of SiGe. The SiGe device showed higher current drive and transconductance in both the linear and saturation regions due to the higher mobilities holes attained in the strained, buried SiGe layer. Figure 5(b) shows that the SiGe device turned on approximately 200 mV earlier than the Si control device as holes first accumulated in the buried SiGe layer with less channel band bending ($\sim 2\Phi_F - \Delta E_V$) than in the Si surface channel device. Also note that the conductance and transconductance are larger for the SiGe device throughout the entire gate voltage range, indicating excellent confinement. The relatively high threshold voltages result from oxide charges and the use of an n^+ polysilicon gate. N^+ polysilicon was used instead of p^+ polysilicon since it is the only type of in-situ doped polysilicon available in our laboratory. The as-deposited low resistivity polysilicon allows us to avoid the thermal cycle necessary for implant repair, activation, and dopant-drive in required for implanted gate devices. The threshold shift resulting from the n^+ poly gate, as opposed to the preferred p^+ poly gate, is on the order of the silicon bandgap.

Linear region field effect mobilities were then extracted from the I_D - V_G curves. The equation below defines field effect mobility for an annular device.

$$\mu_{FE} = \left(\frac{\partial I_D}{\partial V_G} \right) \ln(R_{out}/R_{in}) / \left(2\pi C_{OX} V_{DS} \right) \quad (\text{EQ 1})$$

The mobility therefore, depends linearly on the transconductance and hence, will exhibit the same qualitative behavior as a function of gate voltage as shown for the transconductance in Fig 5(b). Figure 6 summarizes the peak field effect mobilities as a function of temperature for the three channel designs considered

Fig. 6. Peak Field-Effect Mobilities vs. Temperature for annular long channel ($L=50 \mu\text{m}$) SiGe devices and Si MBE and CZ controls.

as well as the Si MBE and CZ controls. Clearly, the SiGe devices have significantly higher mobility than the Si devices. The mobilities may be slightly underestimated here since C_{OX} does not take into account the series capacitance term introduced by the silicon cap. We have used C_{OX} for a conservative comparison over temperature, since at higher temperatures a fraction of the holes will be at the Si/SiO₂ interface. The equivalent series capacitance (for $t_{OX}=210 \text{ \AA}$ and $t_{spacer}=70 \text{ \AA}$) gives,

$$C_{eq} = \left(\frac{\epsilon_{ox}\epsilon_o}{t_{ox}} \right) \left(\frac{1}{1 + \frac{\epsilon_{ox}}{\epsilon_{Si}} \cdot \frac{t_{sp}}{t_{ox}}} \right) \cong 0.9 C_{OX} , \quad (\text{EQ } 2)$$

for a maximum error of about 10%. The highest mobility, $\mu_{FE} = 1622 \text{ cm}^2/\text{V}\cdot\text{sec}$ for the $x=0.3$ SiGe device, was approximately a factor of *four* higher than the Si controls. The trend shown here is that the peak mobility decreased as a function of increasing Ge concentration in the range $x=0.3$ to $x=0.5$. The mobilities of the higher Ge content devices may be lower due to either increased alloy scattering in the SiGe channel or perhaps increased SiGe/Si top interface scattering. Alloy scattering, produced by variations in the Si and Ge atomic potentials, varies as $x \cdot (1-x)$ and hence, reaches a maximum for $x=0.5$. Scattering due to SiGe/Si interface roughness may also play a significant role in limiting the hole mobility and is also expected to increase with Ge concentration. While interface scattering is, in principle, controllable, alloy scattering may impose a fundamental upper limit on the amount of Ge in the buried layer.

4.3 Subthreshold Characteristics

The subthreshold slopes of all devices were measured over temperature, with the expectation that at the lowest temperatures the SiGe device would show a greatly improved subthreshold slope relative to the Si surface channel device for the reasons described in Section 2. Unfortunately, measurement did not bear this out and the subthreshold slopes were roughly the same for both devices ($\approx 15 \text{ mV/decade}$) at the lowest temperatures. Theoretically, the subthreshold slope, defined as the change in gate voltage necessary for a one decade change in drain current, is given by

$$S = \frac{kT}{q} \cdot \ln 10 \left(1 + \frac{C_{dep}}{C_{OX}} + \frac{qD_{it}}{C_{OX}} \right) \quad \text{mV/decade} \quad (\text{EQ } 3)$$

where C_{dep} is the depletion region capacitance, D_{it} is the interface trap density, and C_{ox} is the gate oxide capacitance. In the buried channel PMOS device, C_{ox} is replaced by C_{eq} of EQ. 2, the equivalent series capacitance of the gate oxide and Si spacer layer. At 5K, the ideal subthreshold slope is about 1 mV/decade. The roughly equal subthreshold slopes coupled with the fact that the SiGe device showed no improvement over the Si surface channel device indicates that the limiting factor may be different than the presence of Si/SiO₂ interface traps, perhaps a less than ideal SiGe/Si interface. Device self-heating seems unlikely with the small subthreshold currents flowing. Work is continuing to understand these problems.

4.4 Noise Measurements

Low frequency noise measurements over the range 1 Hz to 10 kHz were also made at room temperature and 5K for the $x = 0.4$ device and the Si MBE controls using the test setup described by Kirschman. [11] Measurements were made at $I_d = 20 \mu A$ in order to assure the carriers were in the buried layer for the SiGe device. The noise voltage (referred to the gate of the FET) showed a $1/f^{1/2}$ behavior. At room temperature, the SiGe and Si devices' noise voltages were nearly identical, and at 5K both devices showed higher noise voltages than at 300K. At 5K, the Si device had a lowest frequency noise voltage of about twice as large as the 300K value, while the SiGe device noise voltage was about four times as large. While the expected improvement in noise characteristics were not observed in the SiGe devices, further improvements in the quality of the SiGe/Si interface could allow improvements to be realized in future devices.

5. CONCLUSIONS

In summary, SiGe PMOS devices with three different channel compositions have been fabricated and higher hole mobilities relative to Si surface channel devices have been measured as a function of temperature between room temperature and 5K. Mobility enhancements relative to identically processed Si controls are largest at the lowest temperatures. The highest mobility measured, $\mu_{FE} = 1622 \text{ cm}^2/\text{V}\cdot\text{sec}$ for the $x = 0.3$ SiGe device, was approximately a factor of four higher than the mobility of the Si control devices. Peak mobility decreased as the fraction of Ge in the SiGe channel layer increased. While the expected enhancements in subthreshold slope and noise characteristics for the SiGe device were not observed, further refinements in the growth process resulting in a higher quality SiGe/Si interface will help us to understand the potential of this device, as well as its limitations, at very low temperatures.

6. REFERENCES

- [1] Nayak D.K., Woo J.C.S., Park J.S., Wang K.L., MacWilliams K.P., *IEEE Electron Device Letters* 12(1991) 154-156.
- [2] Garone P.M., Venkataraman V., Sturm J.C., *IEEE Electron Device Letters* 1(1992) 56-58.
- [3] Verdonckt-Vandebroek S., Crabbé E.F., Myerson B.S., Harame D.L., Restle P.J., Stork J.M.C., Johnson J.B., *IEEE Transactions on Electron Devices* 1(1994) 90-101.
- [4] Van de Walle C.G., Martin R.M., *Physics Review B* 34(1986) 5621-5634.
- [5] Cressler J.D., Comfort J.H., Crabbé E.F., Patton G.L., Sun J.Y.-C., Stork J.M.C., Meyerson B.S., "On The Profile Design and Optimization of Epitaxial Si and SiGe-Base Bipolar Transistors for 77K Applications, Part I and II", *IEEE Transactions on Electron Devices* 40(1993) 525-556.
- [6] Hinckley J.M., Sankaran V., Singh J., *Applied Physics Letters* 55(1989) 2008-2010.
- [7] Warren A.C., "HETMOD- Heterostructure Modeling", IBM Research, 1988.
- [8] Tewksbury S.K., *Solid-State Electronics* 28(1985) 255-276.
- [9] Bean J.C., *Proceedings of the IEEE* 4(1992) 571-586.
- [10] Croke E.T., Harrell M.J., Mierzewski M.E., Plummer J.D., "Use of Low Temperature Si MBE Growth Techniques for High Performance SiGe/Si Electronics", Materials Research Symposium, Boston 30 Nov- 4 Dec 1992 (Materials Research Society Proceedings, 1993) pp. 415-420.
- [11] Kirschman R.K., Lemoff S.V., Lipa J.A., "Evaluation of GaAs FETs for Cryogenic Readout", Conference on Infrared Readout Electronics, Orlando 21-22 April 1992 (Proceedings of the SPIE, 1992) pp. 110-130.