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Low temperature operation of silicon-on-insulator inverters

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Abstract : This paper describes the cryogenic operation of partially depleted Silicon-On-Insulator inverters. As is shown, the floating operation yields a degradation of the transfer characteristics, which increases upon cooling. Additionally, at cryogenic temperatures, hysteresis effects further deteriorate the performance. These observations will be discussed in view of the cryogenic SOI MOSFET characteristics and anomalies. Finally, the impact of the so-called twin-gate configuration on the improvement of the inverter characteristics at low temperatures will be demonstrated and discussed.

1. INTRODUCTION

Inverters play a crucial role in both digital and analog CMOS circuits and can be considered as elementary building blocks [1]. Recently, interest in cryogenic CMOS has increased considerably, the driving force being the development of deep submicron (sub 0.1 μm) CMOS technologies [2]. This also gives a new impulse to research activities in cryogenic Silicon-on-Insulator (SOI) technologies. In spite of this, little work has been performed on the cryogenic operation of either bulk [1,3,4], or SOI CMOS [5] inverters. Here, the low temperature DC transfer characteristic of inverters, fabricated in a partially depleted (PD) 1 μm SOI CMOS technology is demonstrated and discussed.

2. EXPERIMENTAL

The inverters have been processed in a 1 μm CMOS SOI technology on SIMOX substrates. The front-gate oxide thickness is 20 nm; the residual film thickness is 180 nm and the film doping density is such that the devices are partially depleted (PD) and thus suffer from floating body effects. Inverters are

constructed by connecting n- and p-channel devices on the same DIL packaged array, having an internally connected common gate and source contact. This is compared with a so-called twin-gate configuration [6], demonstrated in the right part of Fig. 1. Measurements are performed down to liquid helium temperature, with zero back-gate bias. In most cases, the input voltage is varied from low (0 V) to high values (the supply voltage V_{DD}).

Fig. 1. Schematic representation of a PD SOI CMOS inverter without (a) and with (b) a twin-gate n-MOSFET. The master M has a length L_M and the slave S a length L_S .

Fig. 2. Schematic representation of the twin-gate concept. The middle reach-through junction is left floating and provides electrons to recombine with the multiplication generated holes.

3. RESULTS AND DISCUSSION

3.1 The twin-gate concept

Before studying the cryogenic behaviour of PD SOI inverters, a short introduction is given with respect of the twin-gate concept and how it improves the device performance [6]. A schematic representation is depicted in Fig. 2: the twin-gate MOSFET consists of a transistor which contains a middle reach-through junction, left floating. The two channel parts of the structure (master M and slave S) have a common gate. It is the goal of the structure to keep the master part in linear operation for most of the drain voltages (V_{DS}) applied, thereby restricting pinch-off and carrier-multiplication to the slave part. This also implies that undesirable floating-body and hot-carrier effects are confined to the slave part of the structure. As a result, the kink and parasitic bipolar effects are drastically reduced [6]. This is illustrated for instance for an n-MOSFET at room temperature in Fig. 3, showing a flat output characteristic and thus an improved output impedance. Optimal results are obtained for a large

L_M/L_S ratio, with L_M and L_S the length of the master, respectively the slave part.

As shown previously, the twin-gate structure also improves the cryogenic operation of PD SOI MOSFETs [6]. A reduction of the parasitic floating-body effects is observed. Furthermore, the hysteresis is reduced considerably. This can be inferred from Fig. 4, representing a $1\text{ }\mu\text{m}+1\text{ }\mu\text{m}$ twin-gate n-MOSFET at 4.2 K. Particularly in linear operation, the output curves show little hysteresis, while in saturation, some kink and hysteresis effect is still visible, although reduced compared with a single-gate transistor.

It should finally be noted that not only the static characteristics are improved. Recently, it has been demonstrated that the low-frequency noise behaviour is drastically improved in the kink region [7], whereby the kink-related excess-noise overshoot is successfully eliminated. From these studies clearly follows that in addition to the fact that the floating-body effects are restricted to the slave part, another important factor, contributing to the device-performance improvement is the extra electron-hole recombination, taking place through the middle junction [6,7].

Fig. 3. The reduction of the floating-body effects in a PD SOI n-MOSFET, using the twin-gate (TG) concept. A $20\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ single-gate transistor is compared with a $5\text{ }\mu\text{m}+1\text{ }\mu\text{m}$ TG (bold lines).

Fig. 4. Hysteresis and kink in a $1\text{ }\mu\text{m}+1\text{ }\mu\text{m}$ TG n-MOSFET at 4.2 K. The full lines correspond with a low-high sweep, the dotted lines with a high-low sweep.

3.2 PD SOI inverter operation

The transfer characteristics of the inverters studied suffer from the typical floating body effects at room temperature, as shown in Fig. 5. A clear kink is observed, corresponding to the kink in the floating n-MOSFET (see Fig. 3).

Additionally, at cryogenic temperatures typical device artefacts like the threshold voltage (V_T) instability [2,8] and the transient/hysteresis behaviour affect the inverter transfer characteristics. For instance, in Figs. 6 and 7 a subthreshold 'kink' is observed, corresponding with the subthreshold breakdown behaviour of a SOI n-MOSFET. Furthermore a hysteresis is observed, which is most pronounced in the linear operation regions of the n- and the p-MOSFETs [2]. As a result, the inverter characteristics (noise margin, amplification, etc.) are seriously degraded at low temperatures [9].

Fig. 5. DC transfer characteristics of a $L=3\text{ }\mu\text{m}$ standard PD SOI inverter at 300 K (curve 1 and 3) and at 4.2 K (curve 2 and 4). The supply voltage $V_{DD}=5\text{ V}$ (1 and 2) and 3 V (3 and 4).

Fig. 6. Hysteresis in the inverter characteristics at 4.2 K. $W \times L = 20\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$ and $V_{DD}=3\text{ V}$. LH: V_{in} is swept from low to high; HL: V_{in} is swept from high to low.

Fig. 7. Hysteresis in the output characteristics of a $20\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$ PD SOI n-MOSFET at 4.2 K.

Fig. 8. Inverter transfer characteristics at 4.2 K as a function of the supply voltage. $W \times L = 20 \times 1\text{ }\mu\text{m}$.

In Fig. 8, the effect of the supply voltage on the 4.2 K inverter artefacts is demonstrated. The subthreshold kink has a tendency to increase for increasing V_{DD} (Fig. 8), while its position is fixed. Increasing the device length L , shifts both the subthreshold and the normal kink to higher input voltages V_{in} (Fig. 9) in agreement with the behaviour of the corresponding n-MOSFETs. In the case of the subthreshold breakdown, the latter shifts to a higher drain voltage V_{DS} , for increasing L , to yield the same breakdown field. The kink in saturation on the other hand shifts with the saturation voltage V_{DSSAT} .

Fig. 9. Inverter characteristics at 4.2 K as a function of the device length. $V_{DD}=3$ V.

Fig. 10. Comparison of a standard inverter (1) with a twin-gate inverter at $T=4.2$ K and $V_{DD}=3$ V. (2 and 3). Curve 2: LH sweep; curve 3 HL sweep.

A clear improvement of the transfer characteristic is obtained, both at 300 K [9] and at 4.2 K (Fig. 10), when the twin-gate structure of Fig. 1 is used. Both the subthreshold and the normal kink are reduced, while the same applies for the hysteresis [9]. This is in agreement with the improved output characteristics of the n-MOSFETs, represented e.g. in Fig. 3, and 4. It should finally be remarked that no such improvement is observed if a body tie is used, due to the high series resistance of the body-contact, which produces a kink as well [10].

4. CONCLUSION

From the above, it is clear that the DC characteristics of a PD SOI CMOS inverter is improved by using a twin-gate n-MOSFET in combination with a single-gate p-MOSFET. In fact, this approach is preferred over other alternatives, like the use of a body contact, since it allows a denser design and a nearly complete suppression of the floating body and the low-temperature effects is achieved.

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