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Modeling of self-heating effects in thin-film soi MOSFET's as a function of temperature

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Abstract : Self-heating phenomena are studied from room down to near liquid helium temperatures in fully depleted N channel thin film SIMOX MOS devices. A simple theoretical analysis of the self-heating effect is worked out. A method for the extraction of the thermal resistance and the device temperature rise directly from the static output characteristics is derived. Also direct self heating transient measurements are conducted in order to confirm our analysis.

1. INTRODUCTION

SOI MOS devices are well known to suffer from self-heating phenomena arising from the low thermal conductivity of the buried oxide compared to Si substrate. At sufficiently high current levels, this results in the occurrence of negative output conductance in the saturation region [1-6]. Despite much research in this field [1-7], no detailed analysis and/or simple model of self-heating have been carried out for SOI MOSFET's versus temperature.

In this work, self-heating effect are studied from room down to near liquid helium temperatures on fully depleted N channel thin film SIMOX MOS devices. Moreover, a simple self-heating model is proposed enabling the extraction of the thermal resistance and the average temperature rise of the device directly from the static output characteristics.

2. THEORETICAL ANALYSIS

The temperature rise ΔT due to self heating is assumed to be constant along the channel and proportional to the dissipated power such as,

$$\Delta T = R_{th} I_d V_d \quad (1)$$

where R_{th} is the thermal resistance between the channel and the substrate, I_d the drain current and V_d the drain voltage.

The drain current being a function of temperature, gate voltage V_g and drain voltage V_d , the drain current change ΔI_d due to self-heating can be expressed as,

$$\Delta I_d(T, V_d, V_g) = I_d(T + \Delta T, V_d, V_g) - I_{d0}(T, V_d, V_g) \quad (2)$$

where T is the substrate temperature and I_{d0} is the cold device drain current i.e. in the absence of self-heating.

For small enough ΔT with regard to the substrate temperature, the drain current change can be obtained from a first order expansion,

$$\Delta I_d(V_d, V_g) \approx \frac{\partial I_d}{\partial T} \Delta T \approx \frac{\partial I_d}{\partial T} R_{th} I_d V_d \quad (3)$$

where $\partial I_d / \partial T$ is the drain current substrate temperature sensitivity for given biases.

For large device temperature rise compared to the substrate temperature, this first order approximation does not hold. It is better using a small signal analysis as in [7]. So, it is easy to prove from Rels. 1 and 2 that the output conductance of the self-heated device $g_d = dI_d / dV_d$ can be expressed as,

$$g_d = g_{d0} + R_{th} \frac{dI_d / dT}{1 + R_{th} V_d dI_d / dT} (I_d + g_d V_d) \quad (4),$$

where g_{d0} refers to the output conductance of the cold device (without self heating) and dI_d / dT is the temperature sensitivity of the self-heated device.

In the saturation region, the intrinsic output conductance cancels ($g_{d0} \approx 0$), so that the output conductance of the self-heated device g_{dsat} can be equated to

$$g_{dsat} = \frac{dI_d}{dT} R_{th} I_{dsat} \quad (5).$$

Since the drain current decreases generally with temperature, the saturation output conductance g_{dsat} becomes negative for large enough thermal resistance values.

It should be pointed out, unlike previous analyses [1-6] in our approach, the actual temperature dependence of the MOSFET parameters (mobility, saturation velocity, threshold voltage) is accounted for via the temperature sensitivity dI_d / dT which can directly be measured from experiments changing the substrate device temperatures T .

If this analysis is correct, the curves $g_{dsat} / (I_{dsat} dI_d / dT)$ versus V_d should exhibit a plateau in saturation providing the value of the thermal resistance.

Having extracted R_{th} , it is then possible to re-calculate the intrinsic output conductance g_{d0} as a function of drain voltage using Rel. 4. The intrinsic output drain current I_{d0} of the cold device can then be obtained by a further integration of the $g_{d0}(V_d)$ characteristics as :

$$I_{d0}(T, V_d, V_g) = \int_0^{V_d} g_{d0}(u) du \quad (6).$$

3. RESULTS AND DISCUSSION

Self heating phenomena have been studied on fully depleted N channel thin film SIMOX MOSFET devices fabricated at LETI (Grenoble) with 380 nm buried oxide, 17 nm gate oxide, 80 nm Si film, channel width $W=40\mu m$ and channel length $L=0.8\mu m$. The substrate temperature have been changed between 30 K and 300 K using a cryostat from CTI-Cryogenics. The $I(V)$ characteristics were measured using a HP 4145 semiconductor parameter analyzer.

In Fig. 1 are shown typical output characteristics obtained for temperatures ranging between 30 K and 300 K and which demonstrate the increase of the self-heating effect at low temperature.

Fig. 2 reports the corresponding variation with drain voltage of the drain current temperature sensitivity dI_d / dT as measured experimentally from the data of Fig. 1.

In Fig. 3 are displayed typical variations of the quantity $g_d / [I_d (dI_d / dT)]$ with drain voltage which show the existence of a plateau in saturation. From the amplitude of this plateau, it is possible to evaluate using Rel. 5 the value of R_{th} .

Applying this procedure to all the data made it possible to evaluate the device thermal resistance R_{th} for all the temperatures. The thermal resistance is found to increase significantly at low temperature by about a factor of 3 (see Fig. 4). The increase of the thermal resistance at low temperatures can be attributed to the reduction of the thermal conductivity of SiO_2 after cooling, explaining why self heating is accentuated at low temperature.

Given the values of the thermal resistance allows one to calculate the device temperature rise, $\Delta T = R_{th} I_d V_d$, for all the substrate temperatures. The impact of temperature reduction on the temperature rise induced by the self heating is shown in Fig. 5. Note that ΔT can exceed several hundreds of Kelvins for sufficiently large drain current.

The intrinsic characteristics of the cold device have been re-calculated using Rel. 6 for various temperatures and are given in Fig. 6. After correction of the self-heating effect, the output characteristics in saturation do exhibit an ideal behavior with drain voltage without negative conductance.

Fig. 1 : Typical output characteristics $I_d(V_d)$ of SOI MOSFET's illustrating the onset of self heating at various temperatures (device width $W=40\mu\text{m}$, device length $L=0.8\mu\text{m}$, gate voltage $V_g=5\text{ V}$).

Fig. 2 : Variations with drain voltage V_d of the drain current temperature sensitivity dI_d/dT as obtained experimentally for various temperatures ($V_g=5\text{ V}$).

Fig. 3 : Typical variations of the quantity $g_d/[I_d(dI_d/dT)]$ as a function of drain voltage illustrating the observation of a plateau in saturation region ($V_g=5 \text{ V}$).

Fig. 4 : Experimental variation of the thermal resistance R_{th} as deduced from our analysis.

Fig. 5 : Variations of the device temperature rise ΔT with drain voltage as obtained from our analysis for different temperatures ($V_g = 5$ V).

Fig. 6 : Intrinsic output characteristics $I_{d0}(V_d)$ as obtained after correction of the self-heating effects.

In order to confirm the previous analysis, we have also measured the self heating effect by transient current experiment while applying a pulsed drain voltage [3]. In agreement with our analysis, it has been found that the normalized drain current change $\Delta I_d/I_d$ does vary almost linearly with drain voltage with slope providing R_{th} values around 2200 K/W and 5000 K/W for 300K and 77K, respectively (see Fig. 4). These thermal resistance values are slightly larger than those obtained from our static analysis but infers the overall consistency of the proposed self heating approach.

4. CONCLUSION

Self heating phenomena have been characterized on SOI MOSFET's as a function of temperature. Using a simple self heating analysis, it has been possible to extract from the static output characteristics the thermal resistance and the device temperature rise as a function of temperature. Our approach has been confirmed by direct self heating transient measurements. Our results clearly show that self heating is substantially increased at low temperature because of the reduction of the SiO_2 film thermal conductivity.

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