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Abstract

In this paper low temperature electrical characterisation (LTEC) of submicron MOS transistors is proposed as an optional tool to investigate second-order effects. The LTEC allows to prove the link between the carrier multiplication at the source side and the series resistance effects. This link cannot be distinguished when the MOS transistor is operated at room temperature. This way one is able to do a further research on the series resistance effects and their impact on the extraction of the electrical parameters of submicron MOS transistors.

1. INTRODUCTION

The development of new submicron and deep submicron ($\rightarrow 0.1\,\mu m$) CMOS technologies requires also the development of new electrical models. The development of advanced electrical models for submicron CMOS devices, including the contribution of second and third order effects, is going to be crucial for the correct electrical characterisation and modeling of submicron CMOS technologies. Let's mention a couple of examples. The extraction of the overlapping source/drain-gate length ΔL, using standard electrical models, gives negative values for ΔL [1], which means that the effective channel length L_{eff} ($L_{eff}=L_{gate}-2\Delta l$) is larger than the designed gate length L_{gate}. This is, physically, not plausible. Another example is the "*reverse short-channel effect*" RSC [2]. Normally one should expect a decrease in the value of the threshold voltage V_T as L_{gate} decreases. However, when the RSC effect is present, V_T increases when L_{gate} decreases. These second-order effects mask the intrinsic values of the threshold voltage V_T and the effective gate length L_{gate}. This makes the electrical characterisation and modeling of submicron CMOS technologies not reliable. Therefore is necessary to develop new physics-based electrical models for submicron MOS transistors to explain the second-order effects.
As a first step to develop a new model, the LTEC is proposed as a tool to investigate on the physics and the origin of second order effects and their correlation. This will help to understand what is going on inside the submicron MOS transistor.

Carrier multiplication at the source side and the source series effects are here defined as second-order effects. The occurrence of carrier multiplication at the source side is denounced by the presence of the second substrate current hump (SSCH) [3,4] (see Fig. 1). Strictly speaking one should take the substrate current I_{sub} already as a second-order effect and the SSCH as a third-order effect. As the channel length is scaled down, the substrate current becomes more pronounced. For instance, for a 0.7 μm NMOS LDD transistor operated at V_{drain}=5 V, I_{sub} may be as high as 20 % of the drain current I_{drain}. The I_{sub} is a parameter that should be included in circuit simulators, particularly for high-frequency applications that require the use of submicron channel lengths, and also for low-temperature circuit simulators (temperatures below 150 K).
The parasitic bias-dependent source series resistance R_{is} and the drain threshold voltage V_{Td}, are parameters of the series resistance effects. The drain threshold voltage V_{Td} is the minimum V_{drain} voltage required to have a linear I_{drain}-V_{drain} curve with the MOS transistor operating in the linear mode [5] (see Fig. 2). The drain threshold voltage effect, which may occur even at room temperature, is gate length

dependent [1]. This may cause severe distortion in analog integrated circuits.

2. EXPERIMENTAL RESULTS

Submicron MOS transistors fabricated in the 0.7 μm (SC) and 0.5 μm (AC) IMEC CMOS technologies are characterised from 300 K down to 4.2 K. Both are NMOS LDD transistors. The LDD concentration of the SC devices is $2X10^{18}$ cm^{-3} and for the AC devices $4X10^{18}$ cm^{-3}. The gate oxide thickness T_{OX} is 15 nm for the SC devices and 10 nm for the AC devices, the junction depth of the LDD is about 0.1 μm. A CoSi silicide layer is self-aligned through a 0.2 μm width spacer oxide. The bulk doping concentration is $1X10^{17}$ cm^{-3} in both cases.
The temperature was changed by immersing, the chip into a liquid-helium vessel, at different distances from the liquid-helium surface.

3. DISCUSSION

For the AC transistors, the ones with the higher LDD concentration, the extracted value of the parasitic series resistance R_S is 25 Ω, and 72 Ω for the SC transistors.
The resistance R_S is extracted from the output resistance ($\Delta V_{drain}/\Delta I_{drain}$) as a function of V_{gate} and the gate length L_{gate}[6]. The normalised to its room temperature value R_S* as a function of the ambient temperature T_A is shown in Fig. 3. The devices with a higher LDD dose show a normal decrease of R_S as the temperature is lowered from 300 K down to 150 K. This means that the rate of increase in the carrier mobility μ is larger that the rate of decrease in the free carrier concentration n. A further increase of R_S, from 150 K (beginning of freeze-out) down to 4.2 K, is observed. However, from 300 K down to 150 K, the SC devices show practically a constant value for R_S and a further increase of more than 7 times its room temperature value for temperatures below 150 K down to 4.2 K. This may be explained based on the fact that the SC devices have a lower LDD doping concentration, which means that the free carriers will freeze-out at higher temperatures. Therefore, giving a larger rate of decrease of n than the rate of increase of μ.
The larger increase of R_S, in the case of the SC devices, correlates well with the measured V_{Td} voltage as a function of T_A (see Fig. 4). The larger the parasitic resistance the larger is the absolute value of V_{Td}. The drain threshold voltage, which is also gate-length dependent [1], is a result of the partial freeze-out of the overlapping gate-source LDD region, and may be observed, even at room temperature, when there is not enough gate-source everlapping.
The occurrence of the drain threshold voltage also correlates with the temperature dependence of the carrier multiplication factor M (I_{sub}/I_{drain}) (see Fig. 5). Normally one should expect an approximately linear increase of M versus T_A in the temperature range of 300 K-125 K, and then a plateau region from temperatures below 125 K down to 4.2 K as shown by the thick line (theory prediction) [7]. However, experimental data show that M does not saturate. Moreover, as V_{gate} increases M increases with a larger rate. The unexpected increase of M for high V_{gate} voltages is due to the presence of the SSCH, which becomes more pronounced at low temperatures (see Fig. 6). For T_A<50 K, the magnitude of the SSCH is even larger than that of the first peak. The SSCH is a mechanism controlled by the electric field at the source side E_S [4], and linked to the *bias-dependent* series resistance at the source side [8].
Even when the SSCH, in the case of the AC devices, is not visible at room temperature, the deviation of the M-T_A curve from the plateau region indicates that the electric field E_S, or a small fraction of carrier multiplication at the source side, is present in the tail of the I_{sub}-V_{gate} curve.

The SSCH can be used as a monitor of the electric field at the source side E_S, and is a powerful tool to investigate hot-carrier degradation in submicron MOS LDD transistors [9]. The hot-carrier generation, or carrier multiplication, due to the electric field at the source side E_S might be of serious consequences for the long-term reliability of submicron NMOS LDD transistors. The hot-carriers at the source side are generated very close to the surface, which increases the probability of charge injection into the gate oxide. This may result in leakage current, increase of the gate threshold voltage V_T, reduction of the current drive capability, and, en general, in a degradation of the electrical performance of the submicron MOS transistor.

The *bias-dependent series resistance* is another effect which becomes dominant as the physical dimensions are scaled down. This is, partially, due to the incorporation of the LDD structure, which makes the device more sensible to series effects. If we take a MOS transistor with L_{gate}=0.5 μm and ΔL=0.1 μm, the effective channel length L_{eff} (0.3 μm) will be equivalent, in dimensions, to the overlapping regions (0.2 μm). Then the physics of what is going on in the ΔL region, and their influence on the electrical behavior of the MOS transistor, cannot be neglected anymore. Moreover, the *bias-*

dependent series resistance is coupled to the overlapping source-gate length ΔL. This makes the extraction of ΔL and R_S very difficult.

4. CONCLUSION

In conclusion, the devices which show the larger series resistance effects (R_S and V_{Td}) are those which show a more pronounced SSCH. Then, by using LTEC one is able to find that the SSCH, the V_{Td}, and the R_S effects are coupled to each other. Because the low temperature operation exacerbates these second-order effects, the LTEC has been served as a tool to investigate them and to unveil their correlation, which is not distinguishable at room temperature.

The SSCH can be used as a monitor to study the long-term reliability of submicron NMOS LDD transistors.

The experimental results shown in this paper reveal the need for new physics-based electrical models for submicron MOS transistors. The physics-based model should include second-order effects, such as the series resistance effects discussed here. This would be of much help when characterizing and modeling submicron CMOS technologies, particularly in the extraction of the parasitic series resistance R_S and the effective gate length L_{gate}, which are crucial for the IC designers. Moreover, a physics-based model should help to understand the physics of the series resistance effects, how they degrade the electrical performance of the MOS transistor, and how the device can be designed to be less immune to these effects. This would help also to improve the design of IC for high frequency, low noise, and analog applications.

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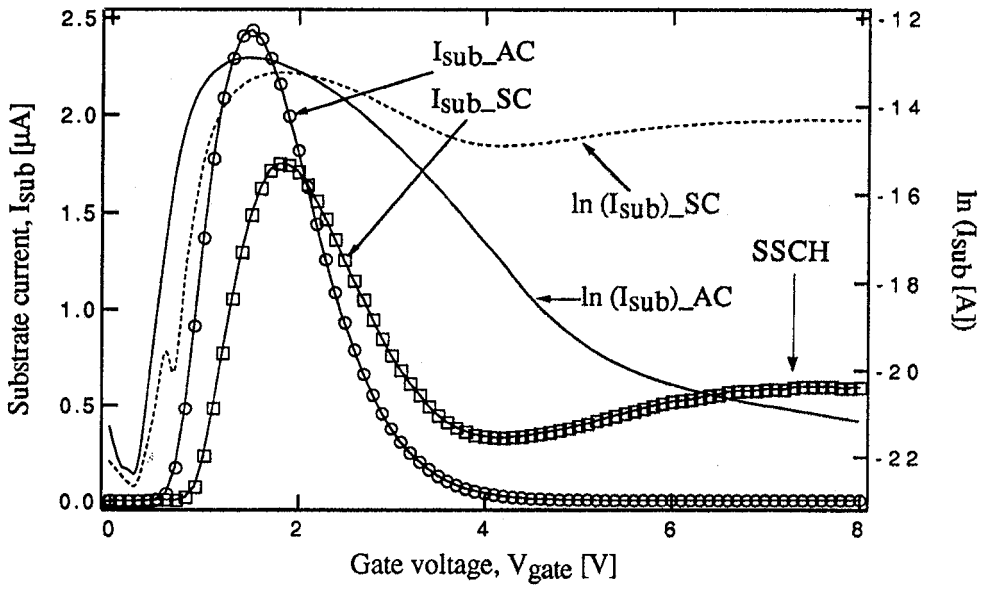

Fig. 1. Experimental results of the substrate current versus the gate voltage I_{sub}-V_{gate} of two different 0.7 μm NMOS LDD transistors operated at V_{drain}=3.5 V and T_A=300 K.

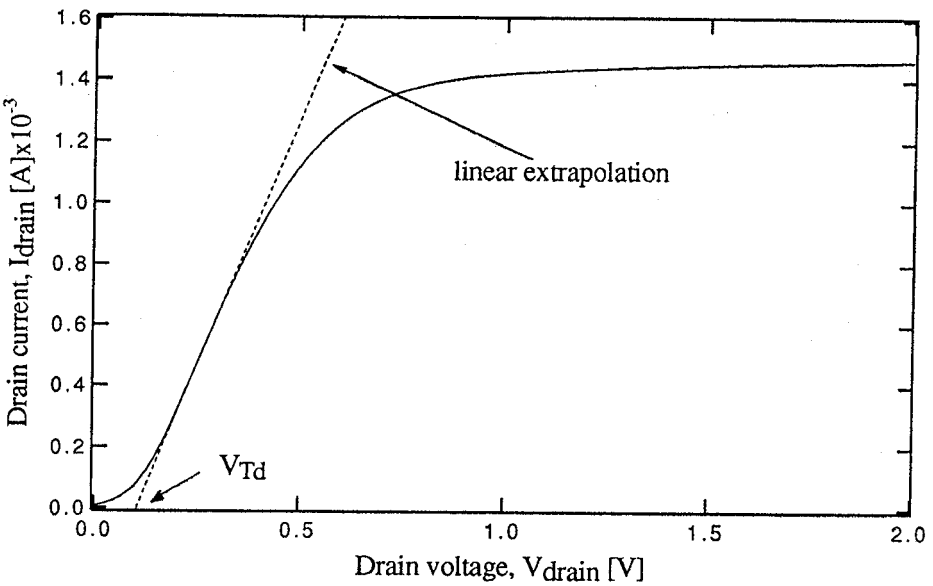

Fig. 2. Experimental results of the drain current versus the drain voltage I_{drain}-V_{drain} of a 0.7 μm NMOS (SC) transistor operated at V_{gate}=2 V and T_A=80 K.

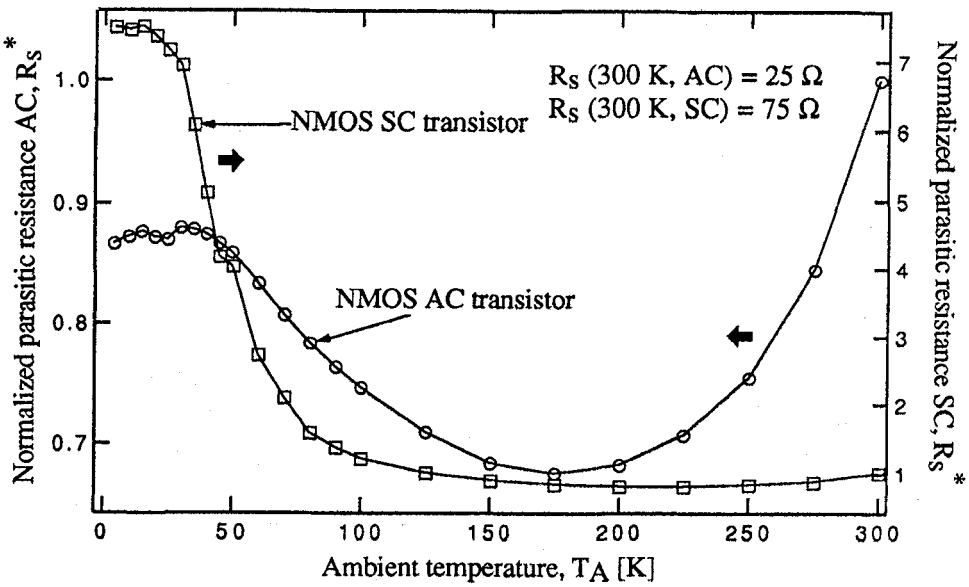

Fig.3. Experimental results of the normalised parasitic series resistance R_S^* as a function of T_A for both submicron CMOS technologies.

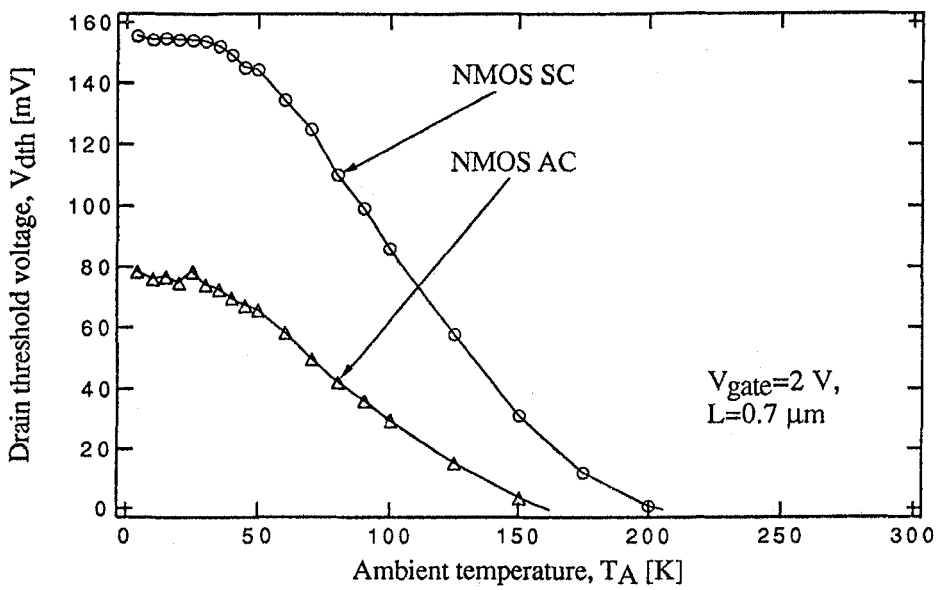

Fig.4. Measured V_{Td} as a function of T_A of MOS transistors fabricated in two different technologies. V_{gate}=2 V, and L=0.7 μm.

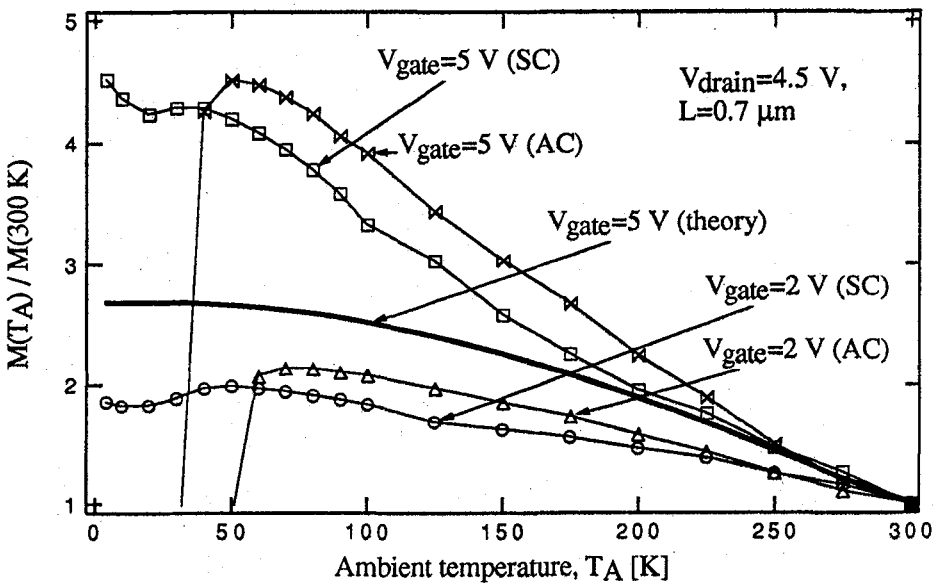

Fig. 5. Experimental results of the normalised to its room temperature value of the multiplication factor M as a function of T_A, for both technologies. V_{drain}=4.5 V, L=0.7 μm, and V_{gate} as a parameter.

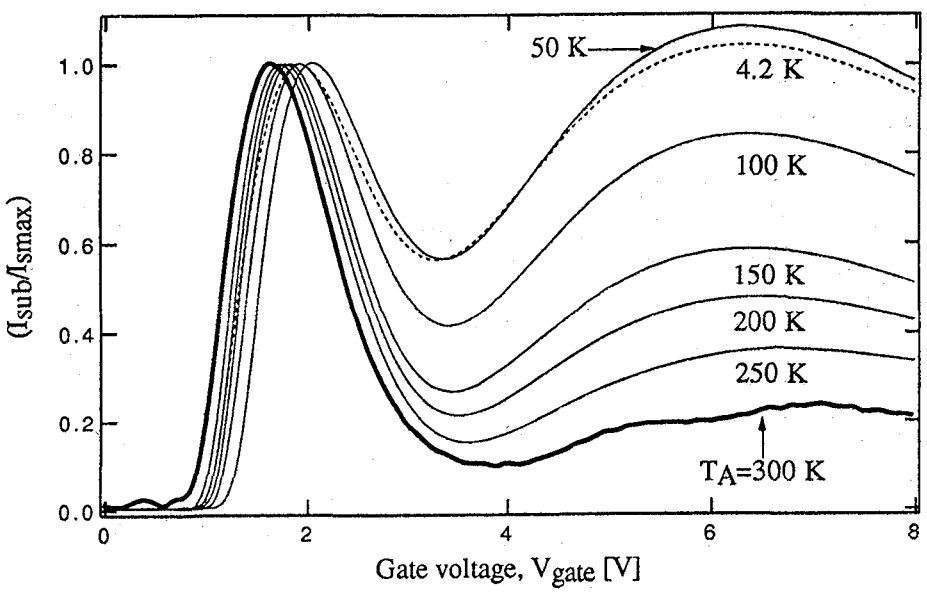

Fig. 6. Experimental results of the normalised to its first-peak value of the substrate current (I_{sub}/I_{smax}) as a function of V_{gate} for a 0.7 μm NMOS (SC) transistor. V_{drain}=3 V, and T_A as a parameter.