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Temperature scaling concept of MOSFET

K. Masu and K. Tsubouchi

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Abstract: Lowering both the threshold voltage ($V_{th}$) and subthreshold swing (S) at the same time is essentially required for 0.1μm and below 0.1μm MOSFETs with low supply voltage. In this paper, we discuss a temperature scaling concept of MOSFET and the device characteristics of the fabricated 77K MOSFETs. In the temperature scaling concept, the physical quantities relating to potential are scaled with operation temperature, while the dimensional quantities are constant. The distribution of mobile carrier concentration are kept constant. In order to design 0.1μm MOSFET with low supply voltage, we proposed the temperature–dimension combination scaling theory (CST). The 77K MOSFET with supply voltage of 1-V has been designed from a 300K parent device on the basis of the combination scaling theory. The fabricated 77K–CST 0.18μm MOSFET has exhibited fully scaled characteristics. The subthreshold swing (S) and the threshold voltage ($V_{th}$) of this device is achieved to be 27mV/dec and 0.21V without degradation of S and $V_{th}$ due to the short–channel–effects degradation.

1. INTRODUCTION

In 0.1μm and below 0.1μm MOSFET era, low–voltage operation (–1V) is essentially required in order to avoid high–electric–field degradation as well as to achieve low power dissipation. The threshold voltage ($V_{th}$) and subthreshold swing (S) should be both scaled down with the reduced supply voltage ($V_{DD}$). Simple requirement is that $V_{th}$ is greater than $(5–6)\times S$ for a sufficient on/off current ratio, and $V_{th}$ is less than $0.2\times V_{DD}$ for high–speed performance, i.e. $V_{th}$ for 1–V operation is needed to be −0.2V. Furthermore, degradation of $V_{th}$ and S due to the short channel effects (SCE) should be substantially suppressed. The scaling rule has been a guiding principle for miniaturizing the device dimensions.1,2) However, at room temperature, scaling of $V_{th}$ and S for low $V_{DD}$ is hardly attainable in simple planar type 0.1μm MOSFETs. The reasons are (1) unscaled S of 60–80mV/dec at room temperature, (2) contradictory requirement for substrate doping: low doping density for low $V_{th}$ and high density for suppression of short channel effects, and (3) unscaleable parameter of built–in potential ($\phi_{bi}$) of $pn$ junction.3)

Low temperature (LT) operation is promising for high–speed MOSFET circuits because of higher transconductance and low wiring resistance.4–10) The significance of LT–MOSFET should be re–recognized as its steep subthreshold swing (S) of S–20mV/dec at 77K. However, lowering $V_{th}$ is still hardly achieved because of the contradictory requirement for substrate doping and the unscaled $\phi_{bi}$. Although 77K 0.1μm MOSFETs with low $V_{DD}$ have been developed, scaling $V_{th}$ and S with the SCE suppression has not been fully addressed.

We have proposed the temperature scaling theory (TST) as a design concept of 77K MOSFET with low supply voltage.11–14)
Simulation and experimental results have shown that $V_{th}$, $S$, and the SCE degradation of 77K–TST device are all scaled down to 77K/300K=1/4, as compared with those of 300K device.\(^{15-17}\) For miniaturizing 77K MOSFET down to 0.1\( \mu \)m regime, we have also proposed the temperature–dimension combination scaling theory (CST).\(^{11,12}\) The fabricated 77K–CST devices have exhibited no SCE degradation of $S$ and $V_{th}$ at the channel length down to 0.18\( \mu \)m.\(^{18,19}\)

In this paper, we discuss the temperature scaling concept and the device characteristics of fabricated 77K MOSFETs designed based on the temperature scaling theory (TST) and the temperature–dimension combination scaling theory (CST).

2. TEMPERATURE SCALING CONCEPT

2.1 Temperature scaling theory (TST)

We have clearly recognized that there are three essential factors in the scaling concept: the scaling quantity, the fundamental equation, and the conservative quantity. As listed in Table 1, in the conventional dimensional scaling, the scaling quantity is dimension and the fundamental equation is Poisson's equation. On the other hand, in the temperature scaling, the scaling quantity is temperature and the fundamental equation is Fermi–Dirac distribution function as discussed in this section in detail. Therefore, the dimensional and the temperature scaling concepts are fundamentally independent of each other. Figure 1 shows the relation between the temperature and the conventional scalings schematically.

The temperature scaling are derived as follows.\(^{11,12}\) At first, we recognized the Fermi–Dirac distribution function as a basis for considering the temperature scaling. The Fermi–Dirac distribution function $f$ is

$$f = \frac{1}{1 + \{ q(\phi - \phi_{F})/kT \}}, \quad (1)$$

where $f$ is the probability and $\phi_{F}$ the quasi Fermi potential. From eq. (1), one can see the probability $f$ is determined by the ratio of the potential to the thermal voltage $kT/q$. In other words, $f$ will not change if the potential is varied in proportion to the temperature. For a MOSFET, since the boundary condition of the mobile carrier is nearly independent of temperature, the distribution of the mobile carrier will be maintained constant. Therefore, the current voltage characteristics will be scaled down if the potential is reduced in proportion to the operation temperature. Although the holes in the bulk region are partly frozen out at 77K, the acceptors in the surface depletion region are completely ionized at 300K and 77K due to the band bending. The electrons in the degenerately doped source and drain regions are not frozen out. Therefore, freeze–out effect in the bulk does not

| Table 1. Three essentials in the scaling concept |
|---|---|---|
| **Scaling quantity** | **Dimensional Scaling** | **Temperature Scaling** |
| | Dimension | Temperature |
| **Fundamental equation** | Poisson's equation | Fermi–Dirac distribution function |
| **Conservation quantity** | Electric field distribution, or potential distribution | Mobile carrier distribution |

Fig. 1.
The relation between the temperature, the dimensional, and combination scalings.
affect the enhancement MOSFET characteristics. We have introduced the temperature scaling factor defined as

\[ \theta = \frac{T^*}{T}, \]

where \( T^* \) is the new temperature, \( T = 300K \) and \( T = 77K \), then \( \theta = \frac{300K}{77K} = 4 \). The new supply voltage \( (V_{DD}) \) should be \( V_{DD}^* = V_{DD}/\theta \). In order to maintain the width of the depletion layer at the pn junction, the substrate doping concentration \( (N_A) \) should be decreased by \( \theta \). The potential barrier of the pn junction can be scaled down by adding the forward substrate bias \( (V_{sb}) \),

\[ \phi_{b1}^* - V_{sb}^* = \left( \frac{\phi_{b1} - V_{sb}}{\theta} \right), \]

where \( \phi_{b1} \) and \( \phi_{b1}^* \) are the built-in potential, \( V_{sb} \) and \( V_{sb}^* \) are the substrate bias. The meaning of applying the forward substrate bias is to scale the built-in potential effectively. The surface potential \( \phi_s = 2\phi_F - V_{sb} \) is also scaled down by the forward substrate bias. The threshold voltage \( (V_{th}) \) is given by

\[ V_{th} = V_{FB} + 2\phi_F + \left( 2\varepsilon_0\varepsilon_r q N_A \right)^{1/2} \left( 2\phi_F - V_{sb} \right)^{1/2}/C_{ox}, \]

where \( V_{FB} \) is the flat-band voltage, \( \varepsilon_0 \) the permittivity of vacuum, \( \varepsilon_r \) the relative permittivity of silicon. \( V_{FB} + 2\phi_F \) is nearly \( 0 \) V for \( n^-\)-poly–Si gate NMOSFET and \( p^-\)-poly–Si gate PMOSFET. The third term of eq. (4) is scaled down by \( \theta \). The threshold voltage \( V_{th} \) is, accordingly, scaled down by \( \theta \) approximately.

The inversion layer thickness is also varied with temperature. If a parabolic potential distribution at the channel region is assumed, it can be approximately given by

\[ t_{inv} = (kT/q)(\varepsilon_r/2qN_A\phi_s)^{1/2}, \]

where \( t_{inv} \) is the thickness of the inversion layer. In eq. (5), the scaling effects of \( T, N_A, \) and \( \phi_s \) cancel out, i.e., the thickness of the inversion layer is kept constant under the temperature scaling.

The temperature scaling factors are summarized in the left column of Table 2. The

| Table 2. Scaling factors of important physical quantities. |
|-------------------|-------------------|-------------------|
|                   | Temperature       | Dimensional       | Combination       |
|                   | Scaling          | Scaling          | Scaling          |
|                   |                   |                   |                  |
| Temperature       | \( T \)           | \( 1/\theta \)    | \( 1/\theta \)    |
| Dimensions        | \( L, W, t_{ox} \)| \( 1 \)           | \( 1/\kappa \)    |
| Voltage           | \( V \)           | \( 1/\theta \)    | \( 1/\kappa \)    |
| Doping conc.      | \( N_A \)         | \( \lambda^2/\kappa \) | \( \lambda^2/\kappa \) |
| \( \phi_s \)      | \( 1/\theta \)    | \( \geq 1/\kappa \) | \( \geq 1/\theta\kappa \) |
| Electric field    | \( E \)           | \( \lambda/\kappa \) | \( \lambda/\theta\kappa \) |
| Subthreshold swing| \( S \)           | \( 1/\theta \)    | \( 1/\theta \)    |
| Threshold voltage | \( V_{th} \)      | \( 1/\theta \)    | \( \geq 1/\theta\kappa \) |
| Drain current     | \( I_{DS} \)      | unsat.           | unsat.           |
|                   | \( \theta_{\mu}/\theta^2 \) |                 | \( \theta_{\mu}/\theta \) |
|                   | \( \theta_{\nu}/\theta \) |                 | \( \theta_{\nu}/\theta \) |
| Gate delay        | \( t_d = CV_{DS} \) | \( \theta_{\mu}/\theta^3 \) | \( \theta_{\mu}/\theta \) |
|                   | \( \theta_{\nu}/\theta \) |                 | \( \theta_{\nu}/\theta \) |
| Power (CMOS)      | \( P_{CMOS} \)    | \( \lambda^2/\kappa \) | \( \lambda^2/\kappa \) |
|                   | \( \theta_{\mu}/\theta \) |                 | \( \theta_{\mu}/\theta \) |
|                   | \( \theta_{\nu}/\theta \) |                 | \( \theta_{\nu}/\theta \) |
| Power-delay product| \( P_t \)      | \( 1/\theta \)    | \( 1/\theta \)    |

\[ f) S = \log_{10}(kT/q)(1+C_D/C_{ox}) \]

\[ g) \text{(unsat.)} \quad I_{DS} = (W/L)\mu C_{ox}(V_G - V_{th})V_{DS} \]

\[ h) \text{(sat.)} \quad I_{DS} = k_{1}C_{ox}\mu C_{ox}V_{DS} \]

\[ i) \text{Frequency } f \text{ is assumed to be proportional to } 1/t_d. \]
temperature scaling theory (TST) is related to the operation temperature, which gives a quantitative relationship between the temperature and device parameters. Since the physical quantities relating to potential is scaled with the temperature, the mobile carrier concentration is maintained constant. In the temperature scaling concept, the scaling quantity is temperature, the fundamental equation is Fermi–Dirac distribution function, and the conservative quantity is the mobile carrier distribution. It can be concluded that the temperature and the conventional scaling concepts relating to device dimension are independent of each other as summarized in Table 1 and Fig. 1.

We have developed the 2–dimensional and 3–dimensional device simulation program (COLD2 and COLD3 (a COmputer simulation program for Low temperature operated Devices in 2 or 3 dimensions) which can be used for the analysis of low temperature MOSFETs.15)

Figure 2 shows simulated $I_D$ vs. $(V_G-V_{th0})$ curves calculated by COLD2. The simulation is performed for an n–channel MOSFET. The upper and lower voltage axes of abscissa correspond to 300K and 77K, respectively. I–V curves of 300K and 77K devices are clearly overlapped, i.e., $I_D$ vs. $(V_G-V_{th0})$ curves of 300K and 77K devices are scaled down with the operation temperature. Figure 3 shows the electron distribution at P (300K, $V_{DS}=V_{G}-V_{th0}=1V$) and P' (77K, $V_{DS}=V_{G}-V_{th0}=0.25V$) for 0.54μm MOSFET, where $V_{DS}$ is the drain–source voltage. It can be confirmed that the distribution of electron concentration is kept constant. The results of Fig. 2 means that the subthreshold swing $S$ and threshold voltage $V_{th}$ is scaled down with the temperature.

Furthermore, we have confirmed by the three dimensional simulation (COLD3) that the $V_{th}$ roll–off and variation of the subthreshold swing $S$ due to the small size effects are also scaled down under the temperature scaling theory.15,16)

![Fig. 2.](image)

$I_D$ vs. $(V_G-V_{th0})$ curves for various channel lengths. Dashed lines are for 300K with $N_A=8\times10^{15}$cm$^{-2}$, $V_{DS}=1V$, $V_{ch}=0V$, and $V_{th0}=1.6V$. Solid lines are for 77K with $N_A=2\times10^{15}$cm$^{-2}$, $V_{DS}=0.25V$, $V_{ch}=0.75V$, and $V_{th0}=1.3V$. The upper and lower axes of the abscissa correspond to 300K and 77K, respectively. $V_{th0}$ is the threshold voltage for 2.68μm channel length. In the calculation, the value of electron mobility were taken to be constant, i.e., 1500 and 3000cm$^2$/Vsec at 300K and 77K, respectively.

![Fig. 3.](image)

Electron distribution of 0.54μm MOSFET in Fig. 2. (P and P')
2.2 Temperature–Dimension Combination Scaling Theory (CST)

Table 2 summarizes the scaling factors of important physical quantities of the temperature scaling theory together with the conventional dimension scaling theory. Circuit performances such as drain current, delay time and power dissipation are also listed. In deep submicron MOSFET, since the electrons flow with the saturation velocity \(v_s\), drain current is given by \(I_{DS}=k_v v_s W (V_G-V_{th}) V_{DS}\). In the temperature scaling regime, the gate delay time \(t_d\) under the velocity saturated case becomes smaller by a factor \(1/\theta_s=0.75\) in spite of the decrease of the supply voltage. Power dissipation of CMOS logic circuit is decreased by a factor of \(1/\epsilon_1^2\).

It is noted that the dimensional quantities are not scaled in the temperature scaling theory. In order to design 77K ultrasmall devices, the dimensional scaling concept should be introduced into the temperature scaling concept. Since the temperature and the conventional dimension scaling concept are fundamentally independent of each other, the temperature–dimension combination scaling theory (CST) can be derived by combining the scaling factors of the temperature and the dimension scaling factors as listed in the right column of Table 2. In Table 2, the generalized dimension scaling theory \(^2\) (DST) is listed; \(\lambda\) is the dimensional scaling factor and \(\kappa\) is the voltage scaling factor. \(\kappa=\lambda\) corresponds to the constant electric-field scaling \(^1\) and \(\kappa=1\) corresponds to the constant voltage scaling.

As shown in Fig. 1, 77K 0.1µm MOSFET can be designed from a 300K device with the combination scaling theory. If the 300K parent device has no degradation of \(V_{th}\) and \(S\) due to the short channel effects (SCE), the 77K CST device is expected to have no SCE degradation. We have already shown by COLD3 that 77K device can be miniaturized to 0.1µm channel length without SCE degradation using CST.\(^{16}\)

3. DEVICE CHARACTERISTICS OF FABRICATED 77K TST MOSFET

In this section, we discuss the fabrication and the measured characteristics of 77K MOSFET's designed only with the temperature scaling theory (TST).\(^{17,18}\)

The device parameters of 77K–TST MOSFETs are designed based on those of 300K devices as listed in Table 3. \(\text{N}^+\)-poly–Si gate n-channel MOSFETs with the arsenic–doped single–drain structure were fabricated. As\(^+\) ion was implanted at 120KeV and the implantation dose was \(2\times10^{15}\text{cm}^{-2}\). After the implantation of As\(^+\) ion, furnace annealing was carried out at 900°C for 30min to activate the implanted impurities. The source and drain \(pn\) junction depths were estimated to be 0.3µm from SUPREM–III (Stanford University Process Engineering Model) simulation. The supply voltages for 300K and 77K were designed to be 4V and 1V, respectively. The channel width \(W\) was 50µm. Here, it is noted that the substrate doping concentration \(N_A\), the gate oxide thickness \(T_{ox}\) and the junction depth \(X_j\) are kept constant with shrinking channel length \(L\), i.e., only the temperature scaling is applied in

<table>
<thead>
<tr>
<th></th>
<th>300K device</th>
<th>Scaling factors</th>
<th>77K–TST device</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T) [K]</td>
<td>300</td>
<td>1/(\theta_s)-1/4</td>
<td>77</td>
</tr>
<tr>
<td>(L_{eff}) [µm]</td>
<td>0.3–10</td>
<td>1</td>
<td>0.2–10</td>
</tr>
<tr>
<td>(T_{ox}) [nm]</td>
<td>25</td>
<td>1</td>
<td>25</td>
</tr>
<tr>
<td>(N_A) [cm(^{-3})]</td>
<td>(4.5\times10^{16})</td>
<td>1/(\theta_s)-1/4</td>
<td>1.1\times10^{16}</td>
</tr>
<tr>
<td>(V_{DD}) [V]</td>
<td>4</td>
<td>1/(\theta_s)-1/4</td>
<td>1</td>
</tr>
<tr>
<td>(V_{sb}) [V]</td>
<td>0</td>
<td>Eq.(3)</td>
<td>+0.7</td>
</tr>
</tbody>
</table>

\(\theta\): the temperature scaling factor, \(T\): temperature, \(L_{eff}\): effective channel length, \(T_{ox}\): gate oxide thickness, \(N_A\): substrate doping concentration, \(V_{sb}\): forward substrate bias, \(X_j\) (source/drain junction depth)=0.3µm, \(W\) (channel width)=50µm.
order to evaluate short-channel effects in TST devices. Electrical measurements at 77K were made with the samples immersed directly in liquid nitrogen. The effective channel length ($L_{\text{eff}}$) is electrically determined by the linear-region channel resistance versus coded gate length curves with varied gate voltage.\textsuperscript{23}

The measured device characteristics of 0.3$\mu$m MOSFET's are summarized in Table 4. Figure 4 shows the measured drain current ($I_{DS}$) as a function of the gate voltage ($V_G$) for 300K and 77K-TST devices. The channel lengths are 0.8$\mu$m and 0.3$\mu$m. The upper and lower axes of the abscissa correspond to the gate voltages for 300K and 77K-TST devices, respectively. The forward substrate bias ($V_{sb}$) for 300K devices is 0V, whereas $V_{sb}$ for 77K devices is +0.7V according to TST. The subthreshold slopes are found to agree well with each other, i.e., $S$ and $V_{th}$ of 77K-TST devices are scaled down to $1/4(\sim 1/4)$ as compared with those of 300K devices.

Figure 5 shows the normalized transconductance ($G_m/W*Cox$) as a function of effective channel length ($L_{\text{eff}}$). Cox is the gate oxide capacitance. $G_m$ is defined as $I_{DS}/V_G$, where $I_{DS}$ is saturation drain current at $V_G=V_{DS}=4V$ for 300K devices and $V_G=V_{DS}=1V$ for 77K devices. The saturation drain current $I_{DS}$ is found to be 12.8mA for a 0.3$\mu$m 300K device.
and 4.8 mA for a 0.3 \mu m 77K–TST device. The saturation drain current ratio $I_{DS}(77K)/I_{DS}(300K)$ is 1.27, which is slightly higher than $1/\sqrt{3}$ predicted by TST. $\theta_s$ is the improvement factor of saturation velocity ($v_s(77K)/v_s(300K)$). The measured low-field mobility of the long-channel 77K–TST devices is found to be about 5 times larger than that of the 300K devices. This improvement is considered to be due to both the low operation temperature and the use of low doping-concentration substrate for the 77K–TST devices. $G_m/W \cdot C_{ox}$ for 77K devices is improved by a factor of 1.5 as compared with that for 300K devices. Although $G_m/W \cdot C_{ox}$ for a 0.2 \mu m 77K–TST device reaches $7.4 \times 10^4$ m/s, $G_m/W \cdot C_{ox}$ does not reach complete saturation. Consequently, the great improvement of $G_m/W \cdot C_{ox}$ for the 77K–TST devices is considered to be due to the increases in both drift mobility and saturation velocity.

The subthreshold swing shift ($\Delta S$) and the threshold voltage roll–off ($\Delta V_{th}$) due to short-channel effects are shown in Figs. 6(a) and 6(b), respectively. In these cases, the dimensional scaling is not applied; the substrate doping concentration and the gate oxide thickness are not changed when the channel length is decreased. $S$ and $V_{th}$ of 77K–TST devices are scaled down to 1/3$^{1/4}$ at any channel length as predicted by TST. It is also found that $\Delta S$ and $\Delta V_{th}$ are nearly scaled down to 1/3$^{1/4}$. Consequently, we have experimentally confirmed that the 77K–TST devices have the scaled characteristics of $S$, $V_{th}$, $\Delta S$ and $\Delta V_{th}$.

**Fig. 6(a).**
Measured subthreshold swing as a function of effective channel length ($L_{eff}$).

**Fig. 6(b).**
Measured threshold voltage as a function of effective channel length ($L_{eff}$).

![Only TST](image-url)
4. DEVICE CHARACTERISTICS OF FABRICATED 77K CST MOSFET

In this section, we discuss the fabrication and the measured characteristics of 77K MOSFET's designed with the temperature–dimension combination scaling theory (CST).\textsuperscript{18,19}

Table 5 lists the device parameters. We first designed the 300K device to have $V_{\text{th}}=0.8V$ and to have no short–channel–effect (SCE) degradation at channel length down to 0.8μm: the gate oxide thickness and the substrate doping concentration were 25nm and $4.5\times10^{16}$ cm$^{-3}$, respectively. The supply voltage ($V_{\text{DD}}$) of 300K device is chosen to be 4V for simplicity. Then, two types of 77K–CST devices, #1 and #2, were designed from the 300K–parent device. The temperature scaling factor is $\theta=4$, the dimensional scaling factor ($h$) is chosen to be $h=2$ for device #1, and $h=8$ for device #2. The voltage scaling factor $\kappa=1$ is adopted in this work for simple verification of CST. $V_{\text{DD}}$ of CST devices is scaled down by $1/\theta=1/4$, i.e., $V_{\text{DD}}=1V$. The forward substrate bias is designed to be $V_{\text{sb}}(77K)-0.8V$ using $V_{\text{sb}}(300K)=0V$, $V_{\text{bi}}(300K)=0.9V$, and $V_{\text{bi}}(77K)=1.1V$ in eq. (3).

The threshold voltage $V_{\text{th}}$ for 77K–CST devices is predicted to be scaled down by $1/\theta$ of that of 300K devices, i.e., $V_{\text{th}}=0.2V$. No SCE degradation is expected to be observed at channel length down to 0.4μm for 77K–CST device #1, and 0.1μm for CST #2. The junction depth of all devices are chosen to be as shallow as possible in order to clearly evaluate SCE degradation. The channel length were 50μm.

N$^+$–poly–silicon gate n–channel MOSFETs were fabricated with a single–drain structure. As$^+$ ion was implanted at 40kV and the implantation dose was $2\times10^{15}$ cm$^{-2}$. The annealing for activation was carried out at 900°C for 30min. The junction depth was estimated to be 0.1μm from SUPREM–III simulation.

Figure 7 shows the measured subthreshold characteristics of the 300K–parent device and the 77K–CST device(#2), respectively. The source–drain voltages ($V_{\text{DS}}$) is 0.4V for the 300K device and 0.1V for the 77K–CST device(#2). The gate voltage axis for 77K device is scaled by a factor of $\theta=4$. The measured effective channel length ($L_{\text{eff}}$) of 300K device is 0.88μm, and that of 77K–CST device(#2) is 0.18μm. It has been clearly confirmed that $S$ and $V_{\text{th}}$ for the 77K–CST device are both scaled down to $1/\theta(=1/4)$ as

![Vd(V) for 300K Device](image)

**Fig. 7.**
Measured subthreshold characteristics for 300K–0.88μm, and 77K–0.18μm–CST MOSFET.

<p>| Table 5. Scaling factors and parameters of 300–K and 77K–CST devices. |
|------------------|------------------|------------------|</p>
<table>
<thead>
<tr>
<th>$T$ [K]</th>
<th>$L_{\text{min}}$ [μm]\textsuperscript{(a)}</th>
<th>$T_{\text{ox}}$ [nm]</th>
<th>$N_A$[cm$^{-3}$]</th>
<th>$V_{\text{DD}}$ [V]</th>
<th>$V_{\text{sb}}$ [V]</th>
<th>$V_{\text{th}}$ [V]</th>
<th>$S$ [mV/dec]</th>
<th>$L_{\text{eff}}$ [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>300–K device</td>
<td>300</td>
<td>0.8</td>
<td>30</td>
<td>$4.5\times10^{16}$</td>
<td>4</td>
<td>0</td>
<td>See eq.(3)</td>
<td>0.8</td>
</tr>
<tr>
<td>CST Scaling factors</td>
<td>$1/\theta$</td>
<td>$1/\lambda$</td>
<td>$1/\lambda$</td>
<td>$\lambda^2/\theta\kappa$</td>
<td>$1/\theta\kappa$</td>
<td>$\lambda^2/\theta\kappa$</td>
<td>$4.5\times10^{16}$</td>
<td>$4.5\times10^{16}$</td>
</tr>
<tr>
<td>77K–CST</td>
<td>77</td>
<td>0.4</td>
<td>13</td>
<td>$4\times10^{17}$</td>
<td>1</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
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<tr>
<td>device(#1)</td>
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<td></td>
</tr>
<tr>
<td>77K–CST</td>
<td>77</td>
<td>0.4</td>
<td>13</td>
<td>$4\times10^{17}$</td>
<td>1</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
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<tr>
<td>device(#2)</td>
<td></td>
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</table>

(a) $L_{\text{min}}$: designed minimum effective channel length without short–channel–effect degradation.
compared with those for the 300K device. In the 77K-CST devices, source/drain punch-through was not observed even at $V_{DS}=2V$.

Figures 8(a), 8(b) and 8(c) show $V_{th}$ and $S$ as a function of $L_{eff}$. $V_{DS}$ is 0.4V for the 300K devices and 0.1V for the 77K-CST devices. $V_{th}$ and $S$ for the 0.88μm 300K device are 0.74V and 100mV/dec. In comparison, $V_{th}$ and $S$ for 0.18μm 77K-CST device#2 are 0.21V and 27mV/dec. As predicted by the combination scaling theory (CST), the 77K-CST devices #1 and #2 exhibit the SCE-free characteristics down to $L_{eff}=0.38\mu m$ and 0.18μm, respectively. It is confirmed that steep $S$ (27mV/dec) and low $V_{th}$ (0.21V) for 1-V operation are obtained without the SCE degradation at $L_{eff}$ down to 0.18μm using CST. In this paper, we have demonstrated the nMOSFET characteristics. Enhancement type pMOSFET with p⁺-poly-Si gate can be designed according to the same manner; The dual-gate CMOS can be designed according to the combination scaling.

Recently, operation of sub-50nm MOSFETs with a supply voltage below 1.5V at room temperature has been reported. This report shows that MOSFET can be miniaturized below 50nm. However, $V_{th}$ has not been sufficiently controlled to be as low as 0.2-0.3V, which is needed for high current drivability with the low supply voltage. As described in this paper, based on the temperature–dimension combination scaling, $V_{th}$, $S$, $\Delta V_{th}$ and $\Delta S$ are scaled down to be adapted to the low–supply–voltage operation. Sub-0.1μm MOSFET circuit with high speed performance is considered to be designed based on the temperature scaling concept.

A promising application of the low–temperature MOSFET is for super engineering workstation. Although a compact cooling machine with cooling capacity of 250W (77K) and efficiency of 8% has been available, the efficiency should be further improved. The new packaging technology as well as the improvement of the efficiency are the most important key issues for the real application of the low–temperature MOSFETs.

Fig. 8. Measured subthreshold swing ($S$) and threshold voltage ($V_{th}$) vs. effective channel length ($L_{eff}$).
5. SUMMARY

We have proposed a temperature scaling concept for 0.1\mu m and below 0.1\mu m MOSFET. The temperature scaling theory is derived from work was partially carried out at the Superclean Room of the Laboratory for Microelectronics, Tohoku University. The temperature scaling theory is derived from the Fermi–Dirac distribution function and the distribution of mobile carrier concentration is maintained unchanged. In the temperature scaling concept, dimensional quantities are not scaled. In order to design 0.1\mu m devices, the temperature–dimension combination scaling theory has been proposed. We have designed and fabricated 77K MOSFET with supply voltage of 1–V on the basis of the combination scaling theory. The subthreshold swing (S) and the threshold voltage (Vth) of the 77K 0.18\mu m MOSFET with 1–V supply voltage are both scaled down to 1/4 (=77K/300K) of those of the 300K 0.88\mu m device with 4–V supply. The 77K MOSFETs exhibit no degradation of S and Vth at the channel length down to 0.18\mu m. The temperature–dimension combination scaling theory gives a design principle for high–performance 77K 0.1\mu m MOSFETs with 1–V supply voltage.

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References