PLANARIZED LOW-STRESS OXIDE/NITRIDE PASSIVATION FOR ULSI DEVICES

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I. Abstract :

A new planarizing passivation scheme has been developed. The passivation sequence consists of a planarized SiO₂ (deposition/etch-back/deposition; similar to that for the intermetal dielectric in-situ planarization) with a sandwich of PSG and low-stress/low-hydrogen silicon nitride on top. The different process steps, and properties of the deposited materials will be described (e.g. mechanical stress and hydrogen content).

II. Introduction

The passivation of VLSI- and ULSI-devices differs from company to company. The deposition sequences used have, either due to the "chemistry" (gases or organic sources) or due to the kind of activation (thermal or plasma), more or fewer drawbacks. They all have in common a relatively poor step coverage and a tendency to the formation of overhangs, resulting in reduced conformality of the layers. The sub- μm -topographies with high aspect ratios stemming from the increasing demands of ULSI technology lead to problems like encapsulation of by-products, holes after pad-etching, etc.. Since the deposition characteristics cannot be drastically improved without considerable efforts, this leads necessarily to urgent actions in transferring the problem "passivation" process to engineering. Different solutions are possible which, like the reduction of layer thicknesses, only shift the problem to future types of devices.

This article describes a new planarizing passivation scheme that has been developed.

III. Experimental :

The passivation sequence consists of a planarized SiO_2 (deposition/etch-back/deposition) with a sandwich of PSG and low-stress/low-hydrogen silicon nitride on top. The planarization for the undoped SiO_2 layer is similar to that for the intermetal dielectric in-situ planarization (refs. 1,2), consisting of a sequence of PECVD- SiO_2 (TEOS-based), magnetron sputter-etch, ozone activated SiO_2 deposition (TEOS-based) and etchback of the planarized SiO_2 layer to the aluminum topography. With this method it is possible to planarize without voids a relatively wide range of aspect ratios .

The process steps are as follows :

1. 400 nm PECVD TEOS- SiO_2
2. tapering of edges by sputter-etching in Ar
3. O_3 -TEOS- SiO_2 deposition
--> void-free filling of remaining gaps
4. oxide back-etching to Al-lines
5. PECVD TEOS- SiO_2 deposition *
6. oxide back-etching for topography smoothening

==> $\approx$ 300 nm remaining oxide-thickness

* thicker layers increase the degree of planarization

The subsequent $\approx$ 400 nm PSG was deposited using TEOS and TMP in a conventional multichamber single-wafer PECVD-system (see Fig. 1). The low-stress SiN_x top layer was deposited with a thickness of $\approx$ 750 nm in a different chamber of the same PECVD-system, using SiH_4 and N_2 as source material. Photolithography and standard etch-processes were used to pattern the devices.

Fig. 1 : Schematic drawing of the single-wafer multichamber system

- I : undoped PEVDC- and O_3 - SiO_2 deposition chamber
- II : PECVD-PSG deposition chamber
- III : PECVD- SiN_x deposition chamber
- IV : Etch-chamber

IV. Results

Using device structure with a two-level metallization it could be shown that the planarized passivation is not disadvantageous to the electrical performance of the device (see table 1, ref. 2).

Table 1 :

n-channel thick oxide transistor	1.2 μm GDD*	1.0 μm LDD*	0.8 μm LDD
lifetime/lifetime std. sandwich passivation	1	1	1
lifetime/lifetime std. planarized low-stress sandwich passivation	---	≈ 0.8	≈ 0.9

GDD = graded doped drain (shallow pn-junction)
LDD = lightly doped drain (steep pn-junction)

(see Fig. 2; ref. 2).

standard passivation
(high-stress)

planarized passivation
(low-stress)

Fig. 2 : SEM cross-sections of devices with different passivation types

Table 2 :

Properties of the deposited layers :

	PSG	SiN _x
dep. rate	923.3 nm/min	261.6 nm/min
uniformity	± 2.6% (3σ)	± 3.3% (3σ)
P-content	3.3 wt%	---
H ₂ -content	---	8.3 at%
stress	-1.8*10 ⁷ Pa	-6.6*10 ⁷ Pa

Most of the current technologies for the passivation of ULSI devices do not take into account the geometric dimensions of the peripheral regions of the ICs. Because of a larger distance between conduction lines at rectangular corners (see mark in Fig.3) it is not possible to provide a void-free passivation layer on the metal lines. This effect can be detected even in an optical microscope as "optical distortions" (see Fig.3). After patterning the device by standard plasma-etching and/or wet-etching, the metal lines are exposed to environmental atmosphere or packaging material. Consequently, this might lead to corrosion of the aluminum and failure of the devices (see Fig. 4).

Fig. 3 : Light-microscopic top-view on the peripheral regions of a 4Mbit DRAM IC after standard passivation

Fig. 4 : Holes in passivation layer after patterning the device

Due to the upper limit of 450 °C for the deposition of passivation layers (e.g., spiking of aluminum at higher temperatures), CVD-methods based on SiH_4 for oxides (APCVD) or plasma enhanced CVD (TEOS-based for oxides; SiH_4 -based for nitrides) have to be used. Since these methods do not provide a sufficient step coverage, overhangs at corners of small gaps lead to voids or key-holes by coalescing layers. These voids may contain byproducts of the deposition.

In regions of the devices where the aspect ratios are more relaxed, the voids have an opening to the surface of the chip. Resist or packaging material may intrude and lead to additional stress on the aluminum lines (see Fig. 5)

Fig. 5 : Standard passivation on a 4Mbit DRAM IC

Furthermore, due to the reduced step coverage of conventional passivation layers, there is the possibility of reduced isolation between conductive layers in contact holes (see Fig. 6).

* 1 : PECVD-SiN_x (conventional)

* 2 : APCVD-PSG (SiH₄-based)

Fig. 6 : Contact holes after standard passivation

Using a SIEMENS 4Mbit DRAM IC as test module it was shown that the new scheme has several advantages compared to standard passivation techniques :

- * planarization without voids of a relatively wide range of aspect ratios.
- * absence of "optical distortions" or holes in the passivation layer (see Fig. 7)
- * void-free filling of gaps with aspect ratios > 1 in-between conduction lines (see Fig. 8)
- * no channel-like connection between keyholes and chip-surface in contact-holes (see Fig. 9)
- * no degradation of electrical device properties (ref. 2)

= = = > drastic increase of device production yield

Fig. 7 : Light-microscopic top-view of the peripheral regions of a 4Mbit DRAM IC after planarized passivation

Fig. 8 : SEM cross-section of a 4Mbit DRAM IC after planarized passivation

- * 1 : PECVD-SiN_x(low-stress)
- * 2 : PECVD-PSG (TEOS-based)
- * 3 : planarized SiO₂ (IMD-process)

Fig. 9 : Planarized passivation over a contact hole

V. Summary

Using the novel planarizing passivation sequence, it is possible to fill gaps void-free with aspect ratios > 1 in the top metallization level over a wide range. Encapsulation of by-products or holes in the top-layer can be avoided. Even if the throughput is reduced, the implementation of a passivation scheme as proposed improves the reliability and the yield in device production of ULSI devices drastically.

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