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CONDITIONS FOR OBTAINING IN-SITU PHOSPHORUS DOPED LPCVD POLYSILICON LAYERS WITH HIGH CONDUCTIVITY ONTO GLASS SUBSTRATES

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Abstract - In order to obtain low in-situ phosphorus doped LPCVD polysilicon thin films having good conductivity, it is necessary to obtain an amorphous layer which is crystallized after deposition. This condition limits the choice of both temperature and pressure. An appropriate selection of deposition parameters has led to a phosphorus atom incorporation in the range $2 \times 10^{18} - 2 \times 10^{20}$ for a phosphine/silane mole ratio in the range $4 \times 10^{-6} - 4 \times 10^{-4}$. With these conditions, the resistivity varies from 1 to 2×10^{-3} Ω cm.

1.- Introduction

Low Pressure Chemical Vapor Deposition (LPCVD) is a widespread technique and well adapted to the deposition to doped or undoped polysilicon films on crystalline silicon substrates [1-3]. Deposition onto glass substrate at low temperature is quite difficult to control; indeed, the substrate being transparent to infrared radiations emitted by the furnace, it is difficult to control the temperature of the substrate. The fabrication of thin film transistors (TFT) onto glass substrates requires a knowledge of the incorporation level of the doping atoms. A low doping level is needed in the channel region of the TFT whereas high doping is needed for good contacts in the drain and source regions.

In this paper, we analyse the deposition rate of the film onto glass substrates as well as onto a monocrystalline silicon substrate as a function of the PH₃/SiH₄ flow ratio. We correlate the resistivity of the film with the phosphorus atom incorporation.

2.- Experimental procedure

Phosphorus doped polysilicon films are deposited onto 7059 Corning glass substrates by thermal decomposition of a mixture of pure silane and phophine diluted in helium inside a thermal LPCVD reactor. The test samples are held vertically and are perpendicular to the gas flow. These samples are surrounded by ten substrates on both side tand these play the role of a thermal black screen to take into account thermal constraints. The system operates at total a pressure of 100 microbars, the gas flow of pure silane is fixed at 50 s.c.c.m. and 1/°° diluted phosphine flow is varied from 0.1 to 10

s.c.c.m.. This gives a phosphine/silane mole ratio in the range $4 \times 10^{-6} - 4 \times 10^{-4}$. The 0.4 µm thick films are amorphous as deposited at 550°C and then crystallized at 600°C for 12 hours.

The sheet resistance of the films is determined from four-point probe measurements. The solid phase phosphorus concentration is determined from SIMS analysis. The carrier density is deduced from Hall effect measurement at 20°C.

3.- Results

The deposition rates are measured on two 2 inch square glass substrates and on one oxidized monocrystalline silicon substrate. The samples obtained under deposition conditions as mentioned above, that is to say when the thermal problems are minimized, shows a measured deposition rate which is the same whatever the nature of the substrate (glass or oxidized silicon wafer) as shown in figure 1.

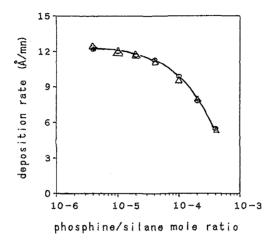
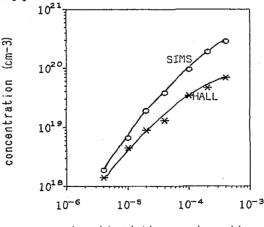


Fig 1- Deposition rate onto glass substrate and crystalline silicon wafer versus PH₃/SiH₄ mole ratio. The depositon conditions are: total pressure 100 microbars, temperature 550°C. (Δ) crystalline silicon wafer (o) glass substrate

Figure 2 shows the dependence of the solid-phase phosphorus concentration and of the free electron concentration versus the phosphine/silane mole ratio. The operating conditions seem to be well chosen to get a low doping level in the studied range because we do not observe any saturation as mentioned by CHIK et al [2].



phosphine/silane mole ratio

Fig 2 - a) Phosphorus concentration determined by SIMS and b) free carrier concentration deduced from Hall effect measurement, as a function of PH_3/SiH_4 mole ratio.

Figure 3 shows a quasi-linear variation of the free carrier concentration, deduced from Hall effect measurement, versus the phosphorus concentration measured by SIMS. The deviation from the ideal curve (dashed-line) arises from the non activation of some proportion of phophorus atoms. These atoms may occupy non-substitutionnal sites or may be trapped by the defects such as grain boundaries, dislocations, etc...

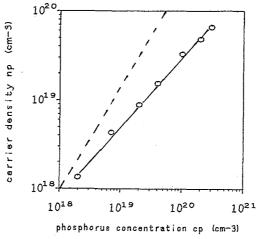


Fig 3 - Free carrier concentration versus phosphorus atomic incorporation concentration. Dashed line: ideal curve.

The electron mobility deduced from Hall measurements and shown in Figure 4 varies by a factor 4 when the phosphine/silane ratio varies by a factor 100. At a low ratio, the mobility is limited both by the presence of grain boundaries and by the intrinsic mobility of the crystalline material. At an intermediate ratio, mobility increases as the doping level because the barrier heights at grain boundaries decrease. At a high ratio, corresponding to a high doping level, the mobility tends to a saturation probably due to the defects induced by the doping atoms.

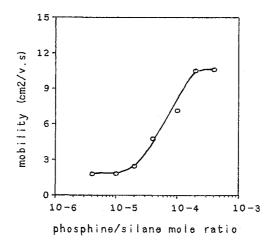


Fig.- 4 Mobility deduced from Hall measurement versus PH₃/SiH₄ mole ratio.

The sheet resistance of the films before annealing is larger than $10^8 \Omega$ and decreases by 3 or 4 decades after annealing. This behaviour is linked to the structural transition of the film material from the amorphous state to the polycrystalline state. This transition is confirmed by a Raman analysis,

as shown Figure 5, which gives evidence of the crystallization of the films. This indicates that the annealing at 600°C during 12 hours is well adapted to induce crystallization.

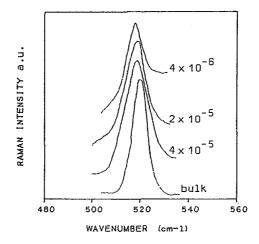


Fig.5 - Raman line intensity of phophorus doped layer versus wavenumber with PH₃/SiH₄ mole ratio as a parameter. The layers are deposited at low temperature (550°C) and annealed at 600°C.

The resistivity of annealed films, deduced from four-point probe measurement, as a function of the total phosphorus concentration is shown in Figure 6. The resistivity decreases down to $2 \text{ m}\Omega$ cm at high levels of concentration. The resistivity measurements on Van der Pauw test structures are in good agreement, the accuracy being +/-15%, with those reported in Figure 6 when the PH₃/SiH₄ mole ratio is larger than 10⁻⁵.

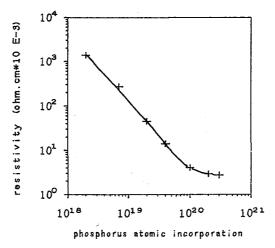


Fig.6 - Resistivity of 0.4 μ m thick annealed films versus phosphorus atomic incorporation.

When the PH₃/SiH₄ mole ratio equals 4×10^{-6} , we have observed that the resistivity deduced from sheet resistance measurement is about 2.5 times higher than that deduced from Hall measurement. This discrepancy may be explained by the fact that the measurement conditions are quite different. First, the Van der Pauw test structures are annealed in forming gas; this treatment being necessary to form contacts induces an increase of the conductivity by decreasing the dangling bound density. Second, the resistivity Hall measurements are performed in secondary vacuum conditions whereas the usual resistivity is performed in ambient conditions. The vacuum limits the oxygen adsorption at the surface of the layer. The adsorbed oxygen atoms capture free electrons at the surface of the film. When the doping level is low, the adsorption induces the formation of a depleted region and consequently an increase of the apparent resistivity [4-5]; when the doping level is high, this effect is negligible.

We have also measured at ambient conditions the resistivity as a function of the thickness of films etched by a plasma technique with the PH₃/SiH₄ mole ratio as a parameter (Figure 7). The thicknesses are measured with a Taylor Hobson Talystep. Notice that the resistivity is almost constant for a large thickness range which means that there is both a uniform distribution of doping concentration which is in accordance with the SIMS analysis, and a homogeneity of crystalline

structure. We may also remark on the increase of the resistivity for thicknesses lower than 0.1 μ m; this behaviour may be interpreted as a result of a decrease of the grain size close to the glass/film interface [6] and/or of the field effect occurring between the front and back interfaces similar to a SOI structure.

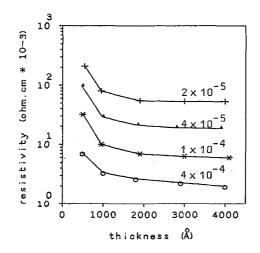


Fig.7 - Resistivity of films deposited at 550° C, annealed and in-situ doped versus the thickness which is controled by plasma etching. The PH₃/SiH₄ mole ratio is mentioned.

4.- Discussion and conclusion

We have presented a set of operating conditions and experimental results in order to obtain in-situ phosphorus doped polysilicon thin films having good conductivity even at low doping concentration.

To this end, the necessary condition is to have a low phosphine/silane flow ratio, but, even if this ratio is fixed, the total flow affects drastically the deposition kinetics via the transport and the transformation of species in the gas phase as well as at the surface of the susbtrate. As a consequence, this condition is not sufficient; besides, several authors had reported high and low limitations in the phosphorus incorporation level [2].

The main step to get undoped and high conductive polysilicon layers, as mentioned by P. JOUBERT et al [7], is to obtain an amorphous layer which is crystallized after deposition. This necessarily limits the choice of the both temperature and pressure. We have selected the 550°C and 100 microbar (total pressure) in order to be at the frontier of the "as deposited" polysilicon conditions. This choice implies a low deposition rate and requires a good reproducibility of the reactor control parameters.

Thus, to obtain low in-situ doped polysilicon films, we have chosen the following parameters : 100 microbar fixed total pressure, 550°C temperature, pure silane flow fixed at 50 s.c.c.m. and phosphine flow $1/^{\circ\circ}$ diluted in He varying from 0.1 to 10 s.c.m.. We have obtained a phosphorus atom incorporation in the range $2 \times 10^{18} - 2 \times 10^{20}$ for a phosphine/silane mole ratio in the range $4 \times 10^{-6} - 4 \times 10^{-4}$, with an almost linear relation. In these conditions, the resistivity varies from

1 to 0.002 Ω cm. The control of a low resistivity and low doping concentration at low temperature allows several applications, especially for the fabrication of thin film transistors onto glass substrates.

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