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THE SELECTIVE EPITAXIAL GROWTH OF SILICON

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Abstract - The SEG technique and its extension epitaxial lateral overgrowth (ELO) have already found many applications in device fabrication both in terms of process simplification and new device structures. The basic processes involve substrate preparation, ex-situ cleaning, in-situ surface oxide removal and SEG/ELO growth. Substrate preparation involves fabrication of the necessary "seed-windows" in, e.g. oxide or nitride layers down to the single crystal substrate: this is usually achieved using a reactive ion etch (RIE) process followed by the growth and subsequent etching of a sacrificial oxide (SO) for surface damage removal. Ex-situ cleaning usually consists of a wet chemical treatment, e.g. RCA, with the final RCA-2 step leaving the silicon surface coated with a reproducible thin oxide layer which also serves to remove various contaminants. The in-situ clean removes the latter oxide through a low pressure H₂ prebake, using a temperature which effectively etches the oxide via the $\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO} \uparrow$ disproportionation reaction, but which minimises the concomitant undercutting of the exposed SiO₂/Si oxide - substrate interface by the same reaction. The growth process involves optimisation of the main parameters, i.e. temperature, pressure and gas flows, to obtain full control of selectivity (i.e. polysilicon nucleation on the field area), sidewall faceting, defect generation and autodoping. This paper will review the technique of selective silicon epitaxy and discuss the results obtained during the optimisation of the above parameters for device applications using a modified Applied Materials LPCVD vertical barrel epitaxial reactor system.

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(1) Introduction

In recent years the LSI fabrication of devices such as bipolar and CMOS has relied upon the local oxidation of Si (LOCOS) for the necessary dielectric isolation. However as device features are scaled down to submicron levels, it follows that the respective isolation scheme must concomitantly be scaled. In this respect the scalability of LOCOS is limited due to lateral oxidation under the nitride mask, resulting in "bird's beak" formation and oxide encroachment into the adjacent "active" device areas: the latter decreases the effective channel width and restricts fine isolation for submicron geometries.

More recently several new dielectric isolation technologies have been described, e.g. trench isolation, which provides effective fine isolation with a high aspect ratio (ref /1/ and refs therein). One other such technique is the selective epitaxial growth of Si, which provides zero lateral encroachment by enabling the deposition of good quality single crystal material into exposed "seed - windows" in a dielectric layer, whilst suppressing concomitant polysilicon nucleation onto adjacent field areas. This provides the capability of fine isolation with a high aspect ratio coupled with relatively small deviations from design limits: SEG can also be used to deposit active device areas. Derivatives of the SEG technique, i.e. epitaxial lateral overgrowth (ELO) /2,3/ and simultaneous single/poly deposition (SSPD or SPEG) /4/ have also been developed: ELO involves the epitaxial growth extending outside the upper bounds of the seed-window, with continued growth both vertically and laterally over the field area. SSPD involves the simultaneous growth of SEG within the seed-window and polysilicon on the field.

Since Si SEG was first reported by Joyce and Baldrey /5/ in 1962 using the SiCl_4/H_2 system at 1200°C and atmospheric pressure, the use of several other systems has been reported using the full range of source gases (i.e. SiCl_4 , SiCl_3 , SiH_2Cl_2 and SiH_4) under similar conditions (see /6/ and refs therein). More recently however, SEG processes using the $\text{SiH}_2\text{Cl}_2/\text{HCl}/\text{H}_2$, $\text{SiH}_2\text{Cl}_2/\text{H}_2$ and $\text{SiH}_4/\text{HCl}/\text{H}_2$ systems at lower temperatures ($\leq 1000^\circ\text{C}$) and pressures ($\leq 80\tau$) have been reported /6/, resulting in considerable material improvements; e.g. layer thickness uniformity and surface morphology /7,8/, selectivity /1/ and quality of the Si/ SiO_2 sidewall interface /9,10,11/. Borland /11/ has presented a paper entitled "Historical Review of SEG and Future Trends in Silicon Epi Technology" and Jastrzebski /2,3/ has published excellent reviews of the ELO process covering the basic aspects of selective Si growth, to which the reader are referred. The present paper will review the basics of the SEG/ELO processes incorporating data from the literature and the author's own work. The latter centers around an investigation of SEG for advanced VLSI bipolar applications, using a modified Applied Materials 7811 RPCVD vertical barrel reactor system with the $\text{SiH}_2\text{Cl}_2/\text{HCl}/\text{H}_2$ system over the temperature range 850°C - 1150°C and pressure range $8-30\tau$. The fundamentals of SEG will be discussed under the main headings of in-situ surface oxide removal, selectivity control, film thickness uniformity, sidewall facet and defect control, in-situ doping and basic electrical characteristics, in respect of prebake and growth parameters and substrate pattern orientation: the discussions will be limited to growth onto (001) orientated substrates.

(2) Experimental Details

The epitaxial deposition system comprised a modified commercial Applied Materials AMC7811 RPCVD vertical barrel reactor fitted with an upgraded pumping system, consisting of an Edwards E250 backing pump coupled with a 2600m³/hr hydrokinetic Roots blower. The system enabled the use of prebake/growth temperatures and pressures within the ranges $850^{\circ} \leq T_G \leq 1200^{\circ}\text{C}$ and $8 \leq P_G \leq 760\tau$ respectively, with H₂ carrier gas flows up to ~35slm at the lowest pressures. The reactor quartzware was modified to incorporate a "center-inject" system, which essentially changed the reactor gas flow pattern for improved epilayer thickness uniformity at the lower (surface kinetic limited) growth temperatures.

The SEG substrates were prepared by growing upto 1.2 μm of thermal oxide (1000°C, O₂/HCl/H₂) onto 25 Ωcm p-type (001) wafers, followed in some cases by ~325Å of Si₃N₄ deposition. After nitride etching, the oxide seed-windows were dry etched (CF₄/H₂) using a two stage process to produce relatively steep sidewalls, followed by the growth of an ~200Å sacrificial oxide on the Si surfaces thus exposed, for etch damage removal; the SO was left intact as a protective layer until the substrates were required for use. Prior to loading, the SO was removed using 15:1 BHF followed by an RCA clean /12/, with all wafers being handled using back surface pickup and VESPEL handling tools.

The Si source and HCl gases used were Union Carbide "Ultrapure" (>250 Ωcm) SiH₂Cl₂ (DCS), and high purity HCl. The main H₂ carrier gas was supplied by a Johnson Matthey HM2 diffuser, with a specified output <0.5ppm O₂, <-70°C dew point for an input O₂ of 50ppm. The SEG/ELO thicknesses were measured by removing the oxide/nitride masking layers and using a Dektak profiler: the growth rates of the SEG layers were calculated by dividing the latter values by the growth time.

A JEOL 120CX transmission electron microscope (TEM) operating at 120keV was used to determine the extent of oxide undercutting after prebake, together with the SEG/ELO layer profiles and defect levels after growth. Representative samples were prepared in [110] cross-section to reveal the undercut regions, with the images being mostly obtained from the (000) undiffracted beam at the [110] zone axis. Cross section and standard plan view samples were prepared to assess defect levels. SEM cross sections and plan views were also obtained using a JEOL IC845 microscope.

(3) In-Situ Surface Oxide Removal

In conventional "blanket" epitaxial growth, the necessary in-situ removal of surface oxide prior to deposition is normally performed using a relatively high temperature (e.g. 1150°C) H₂ reduction or HCl etch procedure at either atmospheric or reduced pressure. However considering a SEG growth procedure, this in-situ cleaning stage must now be carefully controlled at a much lower temperature, since the substrate surface contains etched oxide features with exposed Si-SiO₂ interfaces where undercutting reactions can occur. The typical TEM cross section of Figure 1(a) demonstrates the considerable oxide undercutting (~0.47 μm) obtained when using a lower temperature 5 min. 1050°C H₂ prebake at 10 τ total pressure: these values are significantly higher

compared with the $0.3\mu\text{m}$ at $1050^\circ\text{C}/50\tau$ reported by Liu et al /13/ due to the higher prebake pressures used by these authors.

The possible basic chemical reactions for SiO_2 reduction under prebake conditions are given by Oldham and Holmstrom /14/ as;

where (s) and (g) denote solid and gaseous species respectively. However although thermodynamically favourable at the higher deposition temperatures, the rates of the reduction reactions (a) and (b) are relatively small under low temperature prebake conditions /14/, as evidenced by the unmeasurable loss of material from the oxide sidewalls shown in Figure 1(a) (the relatively small etchback from the nitride top surface occurs during removal of the S.O.). This leaves the disproportionation reaction (c) as the basic mechanism for SiO_2 removal via the volatile SiO product /13,15/ in respect of both the cleaning of the RAC-2 "chemical" oxide from the seed-window Si substrate surfaces and the undercutting of the exposed SiO_2 -Si interfaces as shown in Figure 1: i.e., a small oxide undercut is unavoidable if a good quality Si surface is to be produced within the seed-window, as the same removal mechanism is involved in both cases. It is also noted from the latter figure that the undercut demonstrates a significantly faster lateral compared with vertical etch rate, as also reported by Liu et al /13/ using 50τ of H_2 at 1150°C .

The undercut oxide feature of Figure 1(a) demonstrates a number of interesting features, including the formation of a (usually faceted) Si "cusp" located at the etched extremity of the undercut region in contact with the oxide, and an etched substrate trough: the SEM plan view of Figure 1(b) shows the above cusps and troughs after removal of the nitride/oxide layers. Similar effects have been observed and reported by Tromp et al /16/ and Liehr et al /17/, during investigations of the kinetics of high temperature thermal decomposition of SiO_2 on Si(001) substrates. In the present work the cusps are observed to have a non-uniform variable shape in 3D (i.e. note the thickness fringes on the cusps shown in Figures 1(a) and 2(e)) and appear to possess a periodicity around the periphery of the SiO_2 /Si interface: both the cusps and troughs were observed to be common but variable features of all the undercut structures studied. The oxide surfaces of the undercut regions are also observed to exhibit a "scalloped" appearance as shown in Figure 1(c) for a 2 min. $1100^\circ\text{C}/10\tau\text{H}_2$ prebake. It is considered that the cusps are mobile in 3D, with the magnitude and height of the undercut being variable and dependent upon the cusp size, shape and speed of motion, as dictated primarily by the particular prebake conditions being used. Each scallop in the oxide undercut surface is then considered to relate to the movement of a cusp through that particular area of cross section, with the cusps continuously "cutting" inwards as they move around the periphery of the SiO_2 /Si interface: the foregoing forms the basis of a future publication.

The TEM cross sections of Figure 2(a) to (e) show the effects of increasing the 5 min. H_2 prebake temperature from 850°C to 1050°C at 10τ . Both the length and height of the undercut and the magnitude of the trough are observed to decrease with decreasing prebake temperature T_p , with no undercut or trough being measurable at 850°C . With reference to the schematic diagrams of Figure

Figure 1 (a) and (b) cross section and SEM plan views respectively of the main features observed following a 5 minute H_2 prebake at $1050^{\circ}C/10\tau$ (c) 2 minute $1100^{\circ}C/10\tau$

2500Å

Figure 2 (a) to (e) TEM cross sections of oxide undercut regions after a range of 5 minute H_2 prebakes at 10τ .

3(a) and (b) and the measured cusp/trough profile of Figure 3(c) (5 mins. 1050°C/30 τ prebake), various parameters are defined: i.e. the undercut length X_u and maximum height X_h , the variable trough depth X_t and maximum depth X_{TM} . To a first approximation, the amount of Si lost from a trough of unit width can be represented by the parameter $(X_{TM})^2$, although the latter becomes a less reliable measure as the trough widens considerably relative to X_{TM} at the higher prebake temperatures: the data of Figure 4(a) shows plots of $(X_{TM})^2$ versus the corrected prebake time t_p to be linear for two prebake temperatures $T_p = 900^\circ\text{C}$ and 950°C . It is also noted that the lateral position of X_{TM} relative to the original oxide-substrate interface is observed to increase with increasing prebake temperature. Similarly, the data of Figure 4(b) shows corresponding plots for the undercut length X_u also to display a linear dependence. The corrected prebake times used allow for the variable rates of both undercutting and trough formation occurring during the ramps up to and down from the respective prebake temperatures.

On the basis of the above linear prebake time dependences, the data of Figure 5(a) shows Arrhenius plots of the rates of both the undercut $X_{RU} = X_u/t_p$ and trough formation $X_{RT} = (X_{TM})^2/t_p$, giving the respective activation energies $\Delta E_u = 4.3\text{eV}$ and $\Delta E_t = 2.8\text{eV}$. These values are close to the two "boundary" activation energies of 3.9eV (upper) and 3.0eV (lower) respectively, reported by Ghidini and Smith /18/ for the reaction of Si with its native oxide in a low partial pressure of H_2O ; i.e. etching via the $\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO}\uparrow$ disproportionation reaction forming volatile SiO. The above data referring to H_2O is applied to the present system, as considering the present carrier gas used, the Si surface will be covered by a layer of H_2 , with any residual O_2 being expected to form H_2O . The data of Figure 5(b) shows the value of X_h (i.e. the maximum height of any scallop within an undercut region) plotted versus the prebake temperature T_p for a set of 5 min. prebakes at 10 τ ; the data is seen to display a good linear dependence. However this latter dependence is noted to be fortuitous, as at the lower prebake temperatures where the values of X_{RU} and hence X_u are relatively low (i.e., scalloping of the undercut oxide surface has not yet occurred as demonstrated in Figure 2(a) - (d)), X_h is observed to increase with increasing prebake time; e.g., for $T_p = 950^\circ\text{C}$, $X_h = 433\text{\AA}$ for $t_p = 5$ mins, and $X_h = 1491\text{\AA}$ for $t_p = 99$ mins, suggesting that the cusp height increases with time towards some "equilibrium" value X_{he} . However at the higher prebake temperatures, e.g., $1100^\circ\text{C}/10\tau$, X_h is found to have the same value of $\sim 1100\text{\AA}$ for both a 2 min. and a 5 min. prebake, hence showing the respective cusps to have attained the equilibrium value for $t_p < 2$ mins: i.e. in this case $X_h = X_{he}$. Hence it would appear that although the prebake temperature influences the rates of both undercut and trough formation, X_h tends to an equilibrium value X_{he} which is independent of temperature. The data of Figure 6 shows TEM cross-sections of undercut regions as a function of prebake pressure P_p , for $T_p = 1050^\circ\text{C}$ (a-c) and 950°C (d-f): the data clearly demonstrates a reduction in the value of X_u with increasing P_p for both sets of data. It is also observed that X_{TM} shows the same trend with P_p . The data of Figure 6 (d) - (e) for $T_p = 950^\circ\text{C}$ shows a decreasing value of X_h with increasing P_p ; however in this case because of the relatively low X_u values, X_h has not yet reached the equilibrium value. Alternatively considering the data of Figure 6 (a) to (c) for $T_p = 1050^\circ\text{C}$ where oxide scalloping has occurred, X_h is found to be approximately constant at $\sim 1100\text{\AA}$ in all cases, i.e., identical to the 2 min. and 5 min. 1100°C

Figure 3 Definitions of measured parameters before and after H_2 prebake.

Figure 4 (a) Square of maximum trough depth $(X_{TM})^2$ and (b) undercut length X_u , plotted versus the corrected prebake time t_p .

Figure 5 (a) Arrhenius behaviours of undercut X_{RT} and trough formation X_{RU} and (b) Linear plot of maximum undercut height X_h versus prebake temp. T_p .

Figure 6 TEM cross sections of oxide undercut regions as a function of prebake pressure at (a) - (c) 1050°C, (d) - (f) 950°C: 5 minute bakes.

Figure 7 (a) and (b) SIMS O₂/C interface profiles as a function of prebake conditions, growth 850°C/10τ.

/10 τ samples. Hence, a decreasing pressure and an increasing temperature during prebake both demonstrate similar X_{RU} and X_{RT} dependences, but with the undercut height tending towards a constant equilibrium value in both cases.

The foregoing data has demonstrated that to minimise oxide undercutting at reduced pressure, the H₂ prebake must be performed at a relatively low temperature, with no undercutting being observed for a 5 min. prebake at 850°C/10 τ : the data also shows that undercutting is reduced at the higher pressures. However as demonstrated by Silvestri et al /19/, a 5 min. 850°C/10 τ H₂ prebake is not capable of fully removing the surface oxide prior to growth, even when using an HF dip for native oxide removal immediately prior to reactor loading, with an interfacial oxygen peak of $\sim 7 \times 10^{17} \text{cm}^{-3}$ being observed. The present investigation confirms this result, with the SIMS profiles after epitaxial growth shown in Figure 7(a) and (b) demonstrating respectively, incomplete surface (RCA2 regrown) oxide removal after a 20 min. H₂ prebake at 850°C/8.6 τ , and complete removal (above the SIMS detection limit of $\sim 1.5 \times 10^{17} \text{cm}^{-3}$) after a 10 min. prebake at 900°C/10 τ ; the rise in oxygen level at the epi/CZ substrate interface confirms the sensitivity quoted. In contrast, significant levels of carbon are observed to remain both within the epitaxial layer and at the epi/substrate interface for both prebake temperatures, with the 900°C sample exhibiting lower respective levels: Figures 7(a) and (b) show epilayer carbon concentrations of $\sim 10^{17} \text{cm}^{-3}$ (900°C) and $\sim 2.2 \times 10^{17} \text{cm}^{-3}$ (850°C), and interfacial peak concentrations of $\sim 1.2 \times 10^{17} \text{cm}^{-3}$ (900°C) and $\sim 10^{18} \text{cm}^{-3}$ (850°C): the SIMS C background levels are $\sim 7 \times 10^{16} \text{cm}^{-3}$ and $\sim 1.2 \times 10^{17} \text{cm}^{-3}$ respectively. This interfacial carbon has also been observed by cross section SEM analysis of SEG/ELO structures (see Figure 24(a), Section 4.4); in this respect it is very important to note that the above figures also establish that the carbon does not impair the structural perfection of the SEG/ELO layers.

(4) Selective Epitaxial Growth

An optimised procedure as described in the preceding section results in atomically clean damage-free single crystal Si surfaces within the seed-windows and clean oxide (or nitride) field areas. In this section the parameters which control the subsequent selective growth (i.e. differential nucleation) on these surfaces are considered, together with the effects of layer thickness uniformity, sidewall faceting and defect generation.

(4.1) Selectivity Control

Considering a chlorinated Si source gas such as DCS, the decomposition reaction is given by /20/;

where (g) is a gaseous species, (*) is a free surface site, k are the reaction coefficients and $\text{SiCl}_2(*)$ represents a molecule adsorbed onto the Si surface. This three stage reaction occurs because the absorption energy of an SiH_2Cl_2 molecule is much smaller than that of an SiCl_2 molecule /20/.

The basis of a SEG growth process is to arrange suitable deposition conditions such that single crystal growth occurs at a reasonable rate within the seed-windows, but with the etching action of the HCl either produced from the source gas reaction as above or supplemented from an external source, keeping the dielectric field free of polysilicon nuclei. Selectivity is achieved due to the HCl reducing the effective supersaturation of Si in the gas phase, with the latter requiring to be higher for polysilicon nucleation compared with single crystal growth /20/. Over the single crystal seed-window areas nucleation of Si takes place almost instantaneously; however over the oxide surface, a certain delay time t_D is required before spontaneous Si deposition occurs, with an additional time t_C being necessary for these adatoms to condense to form stable polysilicon nuclei. Claassen and Bloem /20,21/ investigated the spontaneous nucleation of Si over both oxide and nitride surfaces as functions of time, gas composition and temperature. With reference to Figure 8(a), a total critical time $t_1 = t_D + t_C$, termed the spontaneous or homogeneous nucleation time must elapse before stable polysilicon nuclei are formed on the dielectric surface, with a subsequent very rapid increase up to a saturation density N_S . However with reference to Figure 8(b) a second critical time t_2 is in evidence, relating to condensation around localised areas on the oxide surface, e.g. contamination, topographical defects, pinholes, etc, and hence depends upon the general oxide quality, wafer cleaning and handling procedures. In this case N rises gradually towards N_S , due to the superimposition of several different nucleation processes.

By the correct choice of deposition parameters and the use of high quality materials, both t_1 and t_2 can be made relatively long, hence allowing good selectivity during the growth of reasonably thick epilayers. If however nucleation on, e.g. oxide is not fully suppressed, then with reference to Figure 9, polysilicon-free bands are observed to form around seed-windows /22/. The formation of these bands is due to the Si atoms deposited onto the oxide surface within one diffusion length of the seed-window boundary being transported to the lower energy single crystal front: this causes reductions in the local Si gas phase supersaturation, resulting in a relatively lower level of oxide surface adatom concentration and hence no polysilicon nucleation within this region; atoms deposited at distances greater than the diffusion distance away from the solid/gas interface will agglomerate into polysilicon islands. The band widths vary significantly in size depending upon the particular growth temperature and hence Si diffusion distance; e.g. Jastrzebski /2/ reported an $\sim 10\mu\text{m}$ wide band on oxide when using DCS at $1100^\circ\text{C}/760\tau$ and Bean /23/ reported an $\sim 47\mu\text{m}$ band when using TCS at $1150^\circ\text{C}/760\tau$. The effect was used to advantage in 1971 by Blumenfeld et al /22/ in the fabrication of epicon camera targets (Figure 9), where SEG structures were obtained using non-selective epitaxial growth conditions, by spacing the seed-windows within the respective width of the polysilicon-free band.

The value of N_S is observed to be dependent upon the Si source gas used, the growth temperature and the partial pressure of HCl /20,21/. The nett concentration of Si adatoms $[\text{Si}_{AD}]$ on the oxide surface is controlled by the rates of adsorption and etching, and by the density of free surface sites

Figure 8 Critical times for (a) Homogeneous and (b) Heterogeneous polysilicon nucleation (Schematic) (After Ref. 21).

Figure 9 Formation of polysilicon free band (After Ref. 22)

Figure 10 Silicon saturation nucleation density N_s as functions of growth temperature and source gas type. (After Ref. 20)

Figure 11 (a) to (c) selectivity to oxide as functions of growth temperature, pressure and HCl flow rate for DCS source gas. (After Ref. 1).

available. Considering silane, to a first approximation $[Si_{AD}]$ is independent of T_G ; the observed decrease of N_S with increasing T_G shown in Figure 10 is attributed to an increase in the nuclei size by virtue of an increased Si surface mobility /20/, with the total amount of Si deposit remaining constant. Similarly, the presence of HCl significantly reduces N_S by also increasing the nuclei size. However, the use of high growth temperatures is not desirable for a number of reasons, e.g. oxide reactions, solid state diffusion of dopants, etc. In this respect the data of Figure 10 shows the opposite trend of N_S with temperature for DCS and TCS, due mainly to the rapidly decreasing $SiCl_2$ decomposition rate with decrease of T_G , thus making the use of the desirable lower growth temperatures possible for these chlorinated source gases.

Borland and Drowley /1/ investigated the selectivity of the DCS/HCl/ H_2 system as functions of growth temperature, pressure and HCl flow rate. With reference to the data of Figure 11(a) to (c) which shows the epitaxial Si growth/substrate etch rates within the seed-window plotted versus HCl flow rate, Figure 11(a) shows no selectivity at atmospheric pressure over the growth temperature range $900^\circ < T_G < 1000^\circ C$, for HCl flow rates from zero to the point where etching of the Si substrate occurred. However as the total pressure is reduced, selectivity is observed as shown in Figures 11(b) and 11(c) respectively for $P_G = 80\tau$ and 25τ : this data demonstrates that for any specific growth temperature, the HCl flow rate necessary to achieve selectivity decreases as the total pressure decreases, hence giving improved selectivity. With reference to the data of Figure 12, Silvestri /24/ compared the results of Borland et al /1/ with equivalent data for the $SiCl_4$ /HCl/ H_2 system, obtained during an investigation of SEG for trench refill. The data shows a relatively large selectivity range for $SiCl_4$ at atmospheric pressure, compared with none observed for DCS, with Silvestri concluding that if a relatively high SEG deposition rate is desired, the $SiCl_4$ /HCl/ H_2 system provides the most extensive selectivity options (see discussion).

Using a conventional radiantly heated cylindrical reactor, Pagliaro et al /7/ reported good quality uniform single crystal SEG using $T_G = 850^\circ C$, for $P_G < 50\tau$: above this pressure, the polysilicon growth rate was found to be inversely proportional to the seed-window width. Using $850^\circ C/30\tau$ growth conditions, these authors investigated the effects of both HCl and DCS flow rates on crystallinity and selectivity. For $G_R > 0.07 \mu m/min$, non-selective polysilicon growth was obtained, but even without HCl injection, the maintenance of crystallinity, planarity and selectivity were reported for DCS flow rates $< 0.5 slm$. Using growth pressures $< 2\tau$ and a limited reaction processing (LRP) reactor system, Regolini et al /25/ reported Si SEG within the temperature range $650^\circ \leq T_G \leq 1100^\circ C$ using the DCS/ H_2 system with no added HCl. These authors reported no defects such as dislocations or stacking faults (SF's) to be observed during preliminary TEM of layers grown at $650^\circ C$. It was concluded that etching of the polysilicon by the HCl is enhanced at the lower growth pressures, thereby enabling SEG with no additional HCl input. Similarly, it has also been observed in the present investigation that when using $850^\circ C/10\tau$ growth conditions, selectivity can be achieved using the DCS/ H_2 system with no external HCl injection, provided the oxide field surface is of high quality. In comparison, considering the alternative use of silane source gas, selectivity with no HCl input was only observed by Regolini et al for $T_G > 950^\circ C$; below this temperature, an HCl flow of $\sim 10\%$ SiH_4 was required to maintain selectivity. In contrast with the above Sedgwick et al /26/ reported selectivity to oxide at atmospheric pressure over the growth temperature range $600^\circ \leq T_G \leq 850^\circ C$, using the DCS/ H_2 system with no

additional HCl injection. Using an ultraclean horizontally arranged load-locked reactor system with purified H₂ carrier gas, these authors suggested that the relatively low H₂O partial pressures (30-100ppb) during deposition enabled the growth of good quality SEG down to 600°C. The use of unpurified H₂ was reported to either considerably reduce the growth rate or result in no deposition. It was however noted that even in the presence of relatively high impurity levels, selectivity was unaffected. Using TEM analysis, these authors reported defect free SEG layers with featureless interfaces and no discernable oxide above the SIMS background level of $\sim 8 \times 10^{17} \text{cm}^{-3}$. However it was noted that the number of spurious grains on the oxide increased somewhat with decreasing temperature; this may infer that the system reported was not truly selective (cf the results of Borland and Drowley /1/ (Figure 11), where the DCS/HCl/H₂ system was reported to have no selective range at atmospheric pressure), or that the field material was of relatively poor quality.

The nucleation of polysilicon on the field area is also dependent upon the nature of the material used, e.g. oxide or nitride. Considering the latter materials, Claassen and Bloem /20/ showed that the value of N_g is always lower for oxide, with the largest effect being observed when using pure H₂ carrier gas: the effect of field material is shown in the data of Figure 13 and the TEM plan views of Figures 14(a) and (b) for oxide and nitride field areas respectively. It was considered that a strong absorption of atomic hydrogen on the oxide surface would explain the substantial differences in nucleation observed.

(4.2) Film Thickness Uniformity

The early SEG work performed using relatively high growth temperatures highlighted a specific problem with epilayer thickness control termed the "local-loading effect". The latter basically relates to modification of the SEG growth rate depending upon the substrate pattern detail of masked to unmasked areas (see Figure 15 (a)), and has been discussed by Ishitani et al /8/, Pagliaro et al /7/ and Drowley /27/. Ishitani et al attributed the effect to the Si species spatial concentration variation generated by the coexistence of the masked and unmasked areas; to suppress the effect, these authors recommended increasing the HCl injection to make the Si concentration profile more uniform, increasing the surface ratio of unmasked to masked area and optimising the repetition or mark-space ratio of the seed-well structures. However, as the HCl flow is increased, the SEG growth rate decreases approximately linearly, thereby making the process increasingly sensitive to slight variations in the HCl flow rate.

The spatial non-uniformity of growth rate can be understood by considering the rate limiting steps in the epitaxial deposition process. With reference to the growth rate data of Figure 15(b) /28/, the 950°C/50 τ growth conditions used by Ishitani et al would have been within the gas phase diffusion controlled regime, where the supply of reactants to the growing surface is rate limiting. At the lower temperatures, the growth process becomes surface reaction rate (kinetically) limited, with a relatively higher activation energy as shown. The operational mode of a CVD process in relation to the relative rates of the diffusion and kinetically limited components has been discussed by Bollen et al /29/ in terms of the Sherwood number, Sh: the latter is defined as kl/D , where k is the mass transport coefficient, l is a characteristic dimension (i.e. seed-window width) and D is the gas phase diffusivity of the Si containing species. Bollen et al showed that the shape of a deposited SEG layer is governed by the actual value of Sh, with the latter being dependent upon the substrate (i.e. seed-window) geometry and process conditions. For values of $Sh < 1$ relating to narrow seed-

▲ Figure 12 Comparison of selectivity ranges for DCS and SiCl_4 . (After Ref. 24).

▲▲ Figure 13 Silicon saturation nucleation density N_s as functions of carrier gas (H_2/N_2) concentration and oxide/nitride field material. (After Ref. 20).

Figure 14 Comparison of polysilicon nucleation density over (a) oxide and (b) nitride field areas (SEM plan view)

Figure 15 (a) The effect of growth temperature on growth rate and planarity (After Ref. 7) (b) temperature dependence of silicon growth rate using DCS/H_2 at 40τ . (After ref. 28).

windows and/or a relatively slow surface reaction rate, uniform growth results, whereas for values of $Sh > 1$ relating to gas-phase diffusion control, non-uniform growth is obtained.

The above effects are evident in the data of Pagliaro et al /7/ shown in Figure 15(a), where edge cusping and non-uniform growth are observed under diffusion control at 1050°C/30 τ : the edge cusping is due to Si supply from the field regions coupled with the relatively high reaction rate at 1050°C. However as discussed by Drowley /27/, the above model does not explain data where the growth rate into a patterned structure is observed to be less than that onto a blank (unpatterned) bulk Si substrate, where an excess of etching species would need to be supplied from the field regions to the seed-windows. Using SEG growth conditions within the diffusion controlled regime, Drowley demonstrated that for low HCl flow rates, the growth rate onto a patterned wafer is much higher than that onto an unpatterned bulk wafer as shown in the data of Figure 16(a) to (c). However as the HCl flow is increased, the comparative growth rate on the patterned wafer decreases more rapidly until a crossover point is reached, where the growth rate becomes pattern independent. At the crossover point the contributions of Si-containing and Si-etching species from the field regions are balanced, such that the influence of the field is minimised. The HCl flow is found to be slightly greater than or equal to that required to achieve selectivity, and to vary somewhat with area of the field oxide; the largest area resulted in the lowest HCl value at crossover showing the growth to be more pattern sensitive. Using thermochemical data and considering the SEG process with no solid Si present on the oxide surface, Drowley found that the equilibrium HCl partial pressure over the oxide is expected to be 2-4 x higher than the SiCl₂ partial pressure, hence agreeing with the observed growth behaviour. The SiCl₂ concentration was calculated to decrease with deposition temperature, shifting the crossover to lower HCl inputs. Drowley concluded that the optimum SEG conditions occur near to the minimum HCl input required for selectivity, thereby minimising deposition sensitivity to growth temperature and HCl flow rate.

The foregoing has demonstrated that when using diffusion controlled growth conditions uniform SEG can be obtained, but with the process lacking flexibility and operational scope. In contrast, the data of Pagliaro et al /7/ (Figure 15(a)) shows that by using SEG growth conditions within the kinetic regime, flat growth profiles can be obtained with no sensitivity to Si/SiO₂ area ratio or seed-window dimensions; similar results have been obtained by the present author and have been discussed by Ishitani et al /8/.

(4.3) Facet Control

The morphology of SEG layers is highly dependent upon the crystallographic orientation and nature of the dielectric sidewalls with respect to the underlying (001) substrate /9,10,27/. Surface non-planarity occurs due to facet formation along the Si/SiO₂ interface at the window periphery, with the development of these facets being dependent upon process parameters, e.g. growth time, temperature and HCl partial pressure. During SEG, the facets are generated from the bottom edge of the {110} orientated sidewall and are always observed to be {311} regardless of the window-shape, depth and crystallographic orientation of the patterns, as shown typically in the SEM cross section of Figure 17(a). In contrast, there is no facet development along the main {100} orientated sidewalls, as shown in the equivalent cross section of Figure 17(b).

The occurrence of facets is observed to depend upon whether the seed-well pattern is positive or negative /9,10/; i.e. with reference to the SEM plan view of Figure 18(a) and (b), the 15 μ m square windows with 3 μ m wide oxide isolation representing positive patterns with main {110} and {100}

Figure 16 Growth rate versus normalised HCl flow for patterned and bare Si ("Bulk") wafers at (a) 1000°C/50τ (b) 1000°C/100τ and (c) 950°C/50τ: DCS flows are indicated flows. (After Ref. 27).

Figure 17 Facet formation during SEG in the (a) <110> and (b) <100> sidewall directions.

Figure 18 SEM plan views of SEG grown into 15μm square windows (positive pattern) with main sidewall orientations (a) {110} (b) {100} : (c) and (d) similar plan views of growth into opposite (negative) patterns, respectively. (After Ref. 9).

orientated sidewalls respectively, display four symmetrical facet planes in the $\langle 110 \rangle$ directions. The actual facet size for main $\{100\}$ orientation depends upon the curvature of the corners achieved by reactive ion etching /9,10/. In contrast, the SEM plan views of Figure 18(c) and (d) show SEG growth onto substrates patterned opposite to those of Figure 18(a) and (b), with the square features now being oxide islands rather than seed-windows, thereby representing a negative pattern. Figure 18(c) shows unfilled regions adjacent to the $\{110\}$ sidewalls; however, Figure 18(d) now shows facet free SEG for the negative pattern with main $\{100\}$ orientated sidewalls. Similar effects have been observed by the present author.

It has been demonstrated by a number of authors that facet development depends upon growth temperature, time and HCl partial pressure. It was reported by Kitajima et al /30/ that by lowering the SEG growth temperature, the $\{311\}$ facet in the vicinity of the $\{110\}$ orientated sidewall is enlarged. Considering the growth time, Ishitani et al /6,9,10/ reported that facets are formed at an early stage in the growth process, being generated from the bottom edge of the sidewall and developing in proportion to layer thickness, due to the growth rate difference between the $\{100\}$ and $\{311\}$ planes. It was reported by Stivers et al /31/, Borland et al /32/ and Ishitani et al /6/ that the facets (i.e. surface angle) adjacent to $\{110\}$ orientated sidewalls shrank considerably when the HCl partial pressure was reduced during growth, with $\sim 7^\circ \{11,1,1\}$ facets being reported for the lower flows /32/.

Ishitani et al /6/ reported no differences in faceting adjacent to either oxide or nitride sidewalls. However with a polysilicon sidewall coating, SEG layers were reported to exhibit fairly flat surfaces in the $\langle 110 \rangle$ direction; i.e., the polysilicon reduced the orientation dependence of the growth. Unfortunately however, apart from increasing process complexity, the above coatings were reported to induce defects at the SEG/sidewall interface (see Section 4.4).

Drowley et al /33/ proposed an atomistic model for facet (and sidewall defect) formation during SEG growth of (001) silicon, based upon the influence of the oxide on the nucleation of $\{110\}$ planes: i.e. in the presence of a $\{110\}$ oxide sidewall, the nucleation of the $\{111\}$ planes is speeded up, with rapid growth occurring until the next slowest $\{113\}$ plane is reached /34/, thus accounting for the observed morphology. Ishitani et al /9,10/ developed a model of facet formation based upon the concept of growth interruption at "hollow-bridge" (HB) sites: the latter are defined as epitaxial growth sites located between two surface atoms on the (001) plane as shown schematically in Figure 19(a). According to this model, when epitaxial growth at the HB sites is interrupted by the sidewall, i.e. for $\{110\}$ orientation, a $\{111\}$ surface is generated on which step growth takes place from the sidewall to the (001) top surface to form the $\{113\}$ facet plane, as shown schematically in Figure 19(b). However if the sidewall is at an oblique angle to the HB site, i.e. for $\{100\}$ orientation, the $\{111\}$ surface is not generated and the $\{113\}$ facet is not formed. This model also explains why facet formation is independent of sidewall material, field oxide thickness and SEG growth conditions, as it depends solely upon the angle between the HB site orientation and the sidewall direction.

If SEG is allowed to continue growing vertically past the top of the oxide surface, it also begins to seed laterally, thereby forming an ELO structure. The latter, now unbounded overgrowth, is observed to exhibit facets in both the $\langle 100 \rangle$ and $\langle 110 \rangle$ sidewall directions, depending upon the growth conditions and seed-window dimensions. Using $850^\circ\text{C}/8\tau$ growth conditions (20slm H_2) with no added HCl, the SEM cross section of Figure 10(a) (oxide removed) relating to a $\langle 110 \rangle$ sidewall direction exhibits symmetrical $\sim 76^\circ \{331\}$, $\sim 25^\circ \{113\}$ and $\sim 11^\circ \{117\}$ facets for ELO

Figure 19 The development of $\{311\}$ facets adjacent to $\langle 110 \rangle$ orientation sidewalls. (After Ref. 10).

Figure 20

ELO structures grown at $850^\circ\text{C}/8\tau$ (5 min. $950^\circ\text{C}/8\tau$ H_2 prebake) into seed windows of differing size, using different HCl flow rates and main sidewall orientations
 (a) no HCl, $\langle 110 \rangle$
 (b) No HCl, $\langle 100 \rangle$
 (c) 150 SCCM HCl, $\langle 110 \rangle$
 (d) 150 SCCM HCl, $\langle 100 \rangle$.

Figure 21 Growth pressure dependence of the $\{011\}$ facet plane in the $\langle 100 \rangle$ sidewall direction for growth temperature 850°C , HCl flow rate 300 SCCM, H_2 flow rate 50 SLM.

growth into a $5\mu\text{m}$ wide seed-window. The cross section of Figure 20(b) relating to a $\langle 100 \rangle$ sidewall direction exhibits symmetrical $\sim 45^\circ$ $\{011\}$ facets, together with very shallow $1-2^\circ$ surface planes. The fact that no facets are observed in the $\langle 100 \rangle$ direction prior to overgrowth suggests that the presence of the oxide sidewall aids $\{011\}$ nucleation /33/. On increasing the HCl flow rate, e.g. to 150sccm, the equivalent SEM cross sections of Figure 20(c) and (d) (oxide removed) exhibit only $\{113\}$ and $\{011\}$ facets respectively in the $\langle 110 \rangle$ and $\langle 100 \rangle$ sidewall directions: note the comparable variability of the $\{113\}$ facets. Using $850^\circ\text{C}/8\tau$ growth conditions, it was observed by the present author that the above facets were maintained for all ELO structures and HCl flows up to conditions of substrate etch. However, by increasing the total pressure and hence the HCl partial pressure during growth, the $\{010\}$ facet becomes stable, with the proportion of $\{010\}$ to $\{011\}$ facet surface increasing with pressure until a complete $\{010\}$ bounding surface is achieved; i.e. the relative growth rate of the $\{010\}$ plane decreases with increasing HCl partial pressure. The latter is demonstrated in the SEM cross sections of Figure 21(a) to (c) (oxide removed), corresponding to three ELO structures grown at 20τ , 25τ and 30τ respectively. Using a horizontal reactor at 1030°C - 1050°C (SiH_4/H_2), Bradbury et al /35/ demonstrated similar effects at atmospheric pressure for HCl input flow rates between 0.05-0.30slm. With reference to the SEM plan view of Figure 22(a) which shows an ELO structure containing both $\{110\}$ and $\{100\}$ orientated sidewalls, variable faceting is observed along the $\langle 110 \rangle$ direction only giving a comparatively roughened edge.

Considering $\{100\}$ orientated sidewalls, the facet-free nature of SEG growth (see Figure 17(b)) is observed to depend critically upon the SiO_2/Si profile at the seed-well bottom. If this interface contains a rounded profile or tail as shown in the SEM cross section of Figure 22(b), ELO growth will be initiated at the onset of deposition, thereby generating the 45° $\{011\}$ facet at the bottom of the well which will enlarge with continued growth: under these conditions, SEG growth in the $\langle 100 \rangle$ sidewall direction can exhibit a faceted structure, with control of the dry etching process to produce sharp well profiles hence representing an integral part of the SEG technique. The above effect has also been discussed by Kitajima et al /30/.

(4.4) Defect Control

Crystalline defects in SEG layers have been investigated by several authors, notably Kitajima et al /30,36,37/, Ishitani et al /6,9,10/, Drowley et al /33/, Borland and Drowley /1/ and Jastrzebski et al /2,38/. Borland and Drowley /1/ discussed two methods of removing the Si surface damage (formed during the oxide dry etching to produce the required well structure), which would otherwise result in the growth of defective epilayers. The techniques involved either a partial (e.g. 90%) dry etch followed by a wet chemical etch (BHF) to remove the remaining $\sim 200\text{\AA}$ of oxide, or after complete dry etching, using the growth and etch removal of an $\sim 200\text{\AA}$ sacrificial oxide: both of these methods resulted in an improved surface morphology, with the latter technique having been discussed by Liaw et al /39,40/ and used by the present author.

The generation of sidewall defects during selective growth was observed to depend critically upon the crystallographic orientation of the sidewalls with respect to the underlying (001) silicon /10,30/. In particular, at the lower processing temperatures, few defects were observed for $\{100\}$ orientation, but many for $\{110\}$ and intermediate orientations (i.e. between the $\{110\}$ and $\{100\}$). Drowley et al /33/ proposed an atomistic growth model for defect (and facet) formation from the sidewall surface during SEG, based upon the stability of the Si/SiO_2 interface. Using the

DCS/H₂/HCl system, Kitajima et al /30,36,37/ and Ishitani et al /6,9,10/ studied oxide isolated structures with Si₃N₄ coated (0.1 μ m) oxide sidewalls: depending upon deposition conditions, these authors reported the main growth defects to be pairs of stacking faults (SF's) generated from the bottom edges of {110} orientated sidewalls by virtue of the oxide undercut along the substrate interface (see Section 3). V-shaped defects and a number of smaller SF's were also observed originating from the sidewall surface, being dependent upon the quality of the dry etched surfaces. The defect density was observed to decrease with decreasing growth temperature ($950^\circ \leq T_G \leq 1050^\circ\text{C}$) and increasing HCl partial pressure, but with a significant number of SF's ultimately remaining at the rounded (i.e. off-orientation) corners of the structures. Ishitani et al /10/ reported no defects along a $\langle 110 \rangle$ sidewall direction when using $T_G = 950^\circ\text{C}$, but with a considerable number when using $T = 1050^\circ\text{C}$. This is explained in terms of the capability of the nitride sidewalls to protect the oxide-substrate interface from undercut only for $T_G \leq 950^\circ\text{C}$. (see Section 3). When using oxide sidewalls, SF's were observed for {110} and off-orientations when using $T_G = 950^\circ\text{C}$, due to the finite undercut present. However in general, silicon nitride sidewall coatings are observed to induce comparatively more defects at the SEG/sidewall interface /1,30/.

Ishitani et al /10/ also reported SF's generated adjacent to {100} orientated oxide sidewalls when using growth temperatures within the range $950^\circ \leq T_G \leq 1050^\circ\text{C}$ at 50τ (gas-phase diffusion control). These authors described a two-stage growth experiment where two distinguishable sets of SF's were evident, having been generated from the different magnitudes of oxide undercut formed by virtue of the 950°C and 1050°C growth temperatures used. The defect generation was explained by the fact that even though the oxide sidewalls were {100} orientated macroscopically, the "rough" undercut surfaces would possess various crystallographic orientations microscopically, where SF's could hence be generated. The latter is evident in the TEM cross section of Figure 1(c), where the 2 min. $1100^\circ\text{C}/10\tau$ H₂ prebake has produced a very uneven "scalloped" oxide surface (see also Section 3). This effect would reduce with lowering of the prebake and/or growth temperature, making overall low temperature operation desirable.

In a similar manner to facet formation, Ishitani et al /10/ explained SF generation at an oxide undercut in terms of epitaxial growth at displaced HB sites, formed by virtue of the rough nature of the etched oxide surface. With reference to Figure 23, this rough surface enhances Si atom incorporation at the displaced HB sites, thereby generating many SF's as depicted schematically by A-C. However, even in the absence of undercut, off-orientated sidewalls produce a lot of displaced HB sites (e.g. at seed-window corners) where SF's can be generated. Generally, {100} orientated sidewalls contain no displaced HB sites and hence SF generation is suppressed; however, the rough undercut oxide surfaces produced using the higher prebake /growth temperatures can still nucleate SF's in the $\langle 100 \rangle$ sidewall direction as described above.

With respect to the foregoing, defect generation during SEG is minimised by using the lower prebake/growth temperatures (at the lower pressures), the higher HCl partial pressures and main {100} orientated oxide sidewalls. However, Kitajima et al /30/ reported no defects for {110} orientated sidewalls when using low temperature $850^\circ\text{C}/50\tau$ (i.e. kinetically controlled) growth conditions; the prebake conditions were not specified. In a similar manner it has been observed by the present author that when using SEG growth conditions within the kinetic regime, i.e. $850^\circ\text{C}/10\tau$, relatively high prebake temperatures and hence large oxide undercuts can be employed with both

Figure 22 (a) ELO structure showing variable faceting in the $\langle 110 \rangle$ compared with $\langle 100 \rangle$ sidewall direction, (b) SEG growth showing the development of a $45^\circ \{011\}$ ELO type facet at a "Rounded" seed window base.

Figure 23 A cross-sectional view of a stacking fault A-C generated from a $\{110\}$ sidewall edge on an (001) substrate. Squares and circles represent silicon atoms. The arrow indicates the undercut. The lines are chemical bonds between silicon atoms. (After Ref. 10).

Figure 24 (a) TEM cross section showing ELO growth at $850^\circ\text{C}/10\tau$, prebake 5 min. $1050^\circ\text{C}/10\tau$, using $\{100\}$ sidewall orientation: Note the void formation due to the scalloped nature of the oxide undercut surface (b) TEM plan view of the above structure, showing a corner area with main $\{110\}$ sidewall orientation.

{100} and {110} orientated sidewalls, with generally no defect generation being observed. This is demonstrated for {100} sidewall orientation in the TEM cross section of Figure 24(a) for an ELO structure, where a 5 min. 1050°C/10 τ prebake produced an ~5500Å oxide undercut prior to growth at 850°C/10 τ . The SEG is observed to fill the undercut region, with the exception of a small void being evident adjacent to the oxide surface due to the scalloped nature of this interface having "isolated" this particular area during growth: however, it is noted that the entire SEG/ELO regions contain no defects. The latter is further demonstrated for a similarly grown sample shown in Figure 24(b), where the TEM plan view shows no defects to be emanating from the ~5500Å undercut areas into the SEG regions of this ELO structure, regardless of the continuously changing crystallographic orientation of the oxide sidewalls at the rounded corner of the seed-window. Such defect-free growth is considered to be a possible direct consequence of the kinetic nature of the growth process.

Whereas SF's are the dominant defects observed in SEG layers, twins represent the dominant defects observed in ELO regions /30/. Similarly to SEG layers, few defects are observed in ELO regions adjacent to {100} orientated sidewalls, as demonstrated in the TEM plan views of Figure 25(a): the growth conditions were 850°C/10 τ . (5 min 1050°C/10 τ Prebake). However considering {110} orientated sidewalls, the TEM plan view of Figure 25(b) shows a mass of twins extending from the top edge of the oxide into the ELO regions only, together with a few SF's generated from the same area and propagating into both the SEG and ELO regions. Kitajima et al /30/ explained this phenomenon in terms of the stability of the Si/SiO₂ interface: i.e., as the growth direction changes from vertical to lateral, the Si orientation at the interface changes from {110} to {001} via {111}. These latter Si surfaces make more stable interfaces with SiO₂ compared with the intermediate directions, with the unstable surfaces emerging synchronously along the oxide edges generating twins. Once the twins form, the orientation of the Si at the interface lies between {110} and {111}. The orientation of the Si at the interface fluctuates during growth even within the 850°-900°C range, due to the disproportionation reaction (equation (c) section 3) removing 10-20Å from the oxide surface; this reaction would be suppressed as the lateral growth proceeds. Twinning as above is also observed in the plan view of Figure 25(a) where the crystallographic orientation of the main {100} sidewall changes continuously at the seed-window corner. Note also the uniform nature of ELO in the <100> direction compared with the rough structure and variable faceting observed in the corner section: the ELO growth rate is also observed to be comparatively faster in the <100> direction. Kitajima et al /30/ have published similar results, and report defect generation adjacent to {110} orientated sidewalls to be present down to a growth temperature of at least 800°C (30-50 τ). These authors also commented that when diverting the lateral growth direction by rotating the sidewall orientation by 15°-20° off the {110}, the density of planar defects decreased significantly. Furthermore, for 8-10° off the {110}, the lateral to vertical growth ratio was reported to increase, being normally within the range 1.0 to 1.5 for the DCS/HCl/H₂ system /41/. In Section 4.3 it was commented that a rounded oxide profile at the bottom of a seed-window would induce an immediate ELO growth mode and hence facet formation: such a growth mode will also generate twins within the SEG region, with many defects being observed at the base of {110} orientated sidewalls even for the lower growth temperatures /2/.

If ELO growth is allowed to proceed continuously, then eventually, the two growth fronts seeded from opposite sides of the oxide islands will meet and coalesce. Considering approaching fronts containing large contributions from the horizontally growing {100} planes (see Figure 21(c)), the gas-phase transport of Si atoms to these fronts is inhibited, with the eventual formation of a void

Figure 25 (a) TEM plan view showing an ELO structure grown at 850°C/10τ, prebake 5 mins. 1050°C/10τ, using {100} sidewall orientation (b) as above using {110} sidewall orientation.

Figure 26 (a) TEM of a coalesced ELO structure grown at 850°C/10τ, prebake 10 mins. 1050°C/10τ, showing large voids but no defects evident around the structure. (b) As above but with defects evident.

Figure 27 SIMS profiles relating to ~0.8μm SEG layers grown at 850°C/10τ over arsenic implanted regions, 3×10^{15} cm⁻², 40 keV As⁷⁵: 4hrs @ 1150°C drive in. (a) A typical as-measured profile, prebake 5 mins. 900°C/10τ. (b) A plot of average arsenic autodoping level N_A versus prebake temperature.

/2/. It was demonstrated by Bradbury et al /35/ that by adjusting the shapes of the growing interfaces by varying the HCl partial pressure during specific stages of the ELO process, the void formation on coalescence could be eliminated and the surface perturbation or dip, planarised. Jastrzebski /2/ commented that planar ELO surfaces are obtained when the epitaxial layer thickness is increased by ~100% above that required for complete overgrowth. However as commented by Kitajima et al /30/, elimination of the voids may not necessarily result in the elimination of the dislocations; the latter authors reported that small voids and dislocations were always observed in the coalesced region irrespective of the growth temperature, with the cause not being stress relaxation, but possibly fluctuation of the local atomic position induced by roughness of the SiO₂ surface. The TEM cross section of Figure 26(a) shows an ELO structure grown at 850°C/10 τ after a 10 min prebake at 1050°C/10 τ , which produced relatively large oxide undercuts of ~1.25 μ m: using these growth conditions within the kinetic regime, the undercut regions are observed to be only partially filled with relatively large voids remaining, but with no defects observed to be emanating from these regions. Due to the relatively low (50sccm) HCl flow rate during growth, the two approaching fronts contained large {110} components as is evident in Figure 26(a), with no void hence being formed: the TEM data also shows no defects to be evident in the coalesced region for this particular cross section. However, the equivalent cross section of Figure 26(b) does show defects both within the coalesced and other regions, hence demonstrating the variability of the system as discussed by Kitajima et al /30/.

4.5 In-Situ Doping

SEG/ELO can be in-situ doped in the conventional way using the respective dopant gases; e.g. Borland /42/ has reported SEG dopant ranges of P-type boron 10¹⁴-10²⁰cm⁻³, N-type arsenic 10¹⁴-3x10¹⁹cm⁻³ and N-type phosphorous 10¹⁴-10²¹cm⁻³. Alternatively, if using a buried-layer structure for device applications, the SEG layer can be doped via gas-phase autodoping of the buried layer species: e.g. considering arsenic, then depending upon the prebake conditions used, growth within the kinetic regime will result in a relatively flat epilayer dopant profile due to the evaporated gas phase dopant atoms acting as a reservoir /28,43/. This is demonstrated by the SIMS data of Figure 27(a), which shows an as-deposited "intrinsic" SEG profile (10 mins 900°C/10 τ prebake: 850°C/10 τ growth) to have a relatively flat arsenic autodoping level of ~2.18x10¹⁶cm⁻³ for an ~0.9 μ m epilayer grown onto an As-implanted substrate. The data of Figure 27(b) demonstrates an exponential variation of the average autodoping level with prebake temperature (10 mins, 10 τ), which will obviously depend upon the initial implant surface concentration together with the particular exposed area of buried layer during prebake.

5. Electrical Characterisation

The basic electrical characteristics of SEG layers have been investigated by Kitajima et al /36/ and Ishitani et al /10/. Considering reverse biased p-n junction diodes, Kitajima et al /36/ reported lower junction leakage currents and higher breakdown voltages for SEG layers (Si₃N₄ sidewalls) produced using the lower growth temperatures, consistent with the relative levels of defect density observed by TEM. The SEG layers were grown using temperatures between 950°-1050°C at 50 τ , using the DCS/HCl/H₂ system: it was however reported that for all SEG diodes investigated, the leakage currents were larger when compared with similar LOCOS isolated devices. Ishitani et al /10/ reported that the leakage current depended upon growth temperature, sidewall orientation and

material, with {100} orientation displaying superior junction leakage characteristics compared with {110} orientation. This is demonstrated by the data of Figure 28(a), which shows the temperature variation of junction leakage current as a function of sidewall orientation. It was also reported that an oxide was superior to a nitride sidewall, as the latter contains a lot of fixed charges and induces a relatively higher level of defects at the SEG/sidewall interface /1/.

Ishitani et al /10/ investigated the origin of the leakage current by fabricating sets of p-n junction diodes having the same total area of 1mm^2 , but with the individual diode dimensions varying from set to set: this produced different numbers of square diodes per set, with each set being characterised by a variable total length of sidewall and number of corners. The data of Figure 28(b) which shows the junction leakage current histogram at 5v reverse bias, demonstrates that the total leakage current depends upon the total length of sidewall and number of corners (both increasing from 1 to 6 in Figure 28(b)), and is hence controlled by the interface between the SEG layer and the sidewall surface. The excess leakage compared with the LOCOS control was considered as probably being due to the off-orientated sidewalls at the corners of the square windows, together with the corrugated nature of the sidewall surface achieved by reactive ion etching. However more recently, it has been demonstrated by Applied Materials and Intel /42/ that when using comparatively lower growth temperatures, i.e. 875°C (950°C H_2 prebake), the reverse bias (10v) leakage of SEG diodes is superior to equivalent LOCOS isolated structures.

During recent years a variety of devices have been fabricated using selective growth techniques; e.g. SOI structures /41,44,45/, CMOS transistors /46-52/, bipolar transistors /53,54/, MOSFET structures /56,57/, BiCMOS devices /58/ and DRAMS /59,60,61/. Figure 29(a) to (d) shows typical examples of a submicron dual buried layer twin-well CMOS SEG structure /50/, an ELO bipolar transistor /54/ and proposed DRAM cells beyond 4Mb of stacked switching-transistor (SSS), with a horizontal and a vertical switching transistor respectively /59,61/. Such device applications require the use of SEG/ELO materials with the highest quality Si/insulator interfaces: hence as discussed in the preceding sections, the SEG/ELO prebake/growth conditions must minimise facet/defect formation and hence device leakage currents. However, as discussed by Kitajima et al /30/, the relatively smaller dimensions for VLSI technology arrange relatively higher percentages of {110} orientated sidewalls at the seed-window corners, making the control of defects a necessity for all sidewall orientations. In this respect, although the lower growth temperatures are reported to reduce defect levels, the facet is enlarged in the vicinity of {110} orientated sidewalls /30/; as discussed in Section 4.3 this effect can be eliminated by using a negative oxide pattern (Figure 18(d)) or alternatively the technique of mechanical polishing after ELO growth /52,60/.

6. Summary and Discussion

The basics of the selective epitaxial growth process of Si using the CVD technique have been reviewed. Using a combination of dry etching, sacrificial oxide, ex-situ RCA and in-situ H_2 prebaking techniques, good quality single crystal Si and field (oxide or nitride) surfaces can be produced for SEG, whilst causing minimal undercutting of the exposed SiO_2 -Si interfaces: the RCA-2 oxide passivates the Si surface thereby reducing the accumulation of other impurities such as metals and carbon /12/. The activation energy $\Delta E_{\text{a}} = 4.3\text{eV}$ derived for the latter process is close to the value 3.9eV reported by Ghidini and Smith /18/: the latter specifies the upper boundary between regions III and II, which separates the areas of complete SiO_2 passivation (passive) and SiO_2 etching via SiO production (non passivating $\text{Si}_x\text{O}_y\text{H}_z$ film) respectively in a low

Figure 28 Diode junction leakage histograms as functions of (a) growth temperature and main sidewall orientation (b) varying seed-window size (total length of sidewall and number of corners) for a growth temperature of 950°C: SEG versus LOCOS Isolation. (After Ref. 10).

Figure 29 SEG/ELO devices (a) Twin-Well CMOS structure (After Ref. 50) (b) ELO bipolar transistor (After Ref. 54) (c) and (d) DRAM cells (After Refs. 58, 60)

partial pressure of H_2O , according to the disproportionation reaction $\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO}\uparrow$. The present ΔE_{u} value is also close to the 3.83 eV reported by Smith and Ghidini /62/ for the reaction of Si with its native oxide in a low partial pressure of O_2 : however as previously mentioned, because of the H_2 coverage of the Si surface (i.e. 100% H_2 carrier gas used), the present data is not considered to relate to these particular conditions. The $\Delta E_{\text{u}} = 4.3\text{eV}$ is also considerably higher than the value of 3.3eV reported by Liu et al /13/ (H_2 catalyst) for similar oxide undercutting (3 min. 1050°-1150°C, 50 τ H_2 prebakes). The activation energy $\Delta E_{\text{t}} = 2.8\text{eV}$ derived for the trough formation is close to the value of 3.0eV reported by Ghidini and Smith /18/, specifying the lower boundary between region II above, and the clean (active) Si surface of region I. It is therefore considered that the disproportionation reaction is the key element in both the undercut and trough formation mechanisms, compared with the alternative $\text{H}_2\text{O} + \text{Si} \rightarrow \text{SiO} + \text{H}_2$ etching reaction which also has a quoted activation energy of 2.0eV /18/. The maximum undercut height X_{h} tends to an "equilibrium" value X_{he} , which is independent of both the prebake temperature and pressure.

Considering the residual H_2O and O_2 background levels within a reactor system, then because of the comparatively lower levels of H_2O partial pressure necessary to maintain oxide free Si surfaces within the reactor, the presence of H_2O rather than O_2 represents one of the major concerns of low temperature epitaxial (SEG) growth: i.e. the $p(\text{H}_2\text{O})$ has to be approximately an order of magnitude lower compared with an equivalent $p(\text{O}_2)$ level for a similar Si-SiO₂ reaction /18/. Water can enter a reactor system either with the input gases, or be adsorbed onto various surfaces if the system is opened to the atmosphere: however, whereas the former level can be reduced by reducing the reactor total pressure the latter cannot, with the evaporation rate depending upon the various surface temperatures concerned and the gas flow rates. The H_2O background due to water adsorption can hence remain for relatively long periods within the reactor system, but with the work of Sedgwick et al /16/ demonstrating the control of this parameter by careful reactor design; i.e. by using a load-locked system.

The undercut and trough formation mechanisms are hence considered to relate to an interfacial $\text{Si}(\text{cusp}) + \text{SiO}_2$ reaction involving;

- (a) the diffusion of Si across the substrate surface to the oxide interface with the formation of a trough and cusp,
- (b) a solid-state $\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO}\uparrow$ reaction occurring along the cusp-oxide interface, and
- (c) the evaporation and removal of the volatile SiO product.

Considering diffusion, the present activation energies are significantly higher than the 2.0eV reported by Liehr et al /17/, for Si self-diffusion across the substrate surface during the process of thermal decomposition of thermal SiO₂ (50-500Å on Si(100)) within the temperature range 600°-1200°C at $\sim 4 \times 10^{-10} \tau$: the latter mechanism is hence not rate limiting for the present experiments, probably due to the much reduced rate of the $\text{Si} + \text{SiO}_2$ reaction by virtue of the comparatively higher $\sim 10^{-7}$ pressures (and hence relatively lower rates of X_{RU} and X_{RT}) used in the present investigation. The foregoing thus indicates that considering both undercut and trough formation, the most likely rate limiting step is the removal of oxide via the $\text{Si} + \text{SiO}_2 \rightarrow 2\text{SiO}\uparrow$ disproportionation reaction along the cusp-oxide interface, involving the breaking of Si-Si bonds ($E = 3.38\text{eV}$, Liu et al /13/); the rate of SiO removal from the gas phase would account for the observed undercut prebake pressure dependences of Figure 6.

In general therefore, undercutting is minimised by using the lower prebake temperatures and higher H_2 pressures, consistent with the maintenance of an adequate surface clean; however, the results of the present investigation confirm the published results of Kitajimi et al /30/, by showing that when using growth conditions within the lower temperature surface-kinetic regime, relatively large (e.g. $0.5\mu\text{m}$) oxide undercuts do not necessarily induce defects into the growing SEG layer. When using a 10 min. $900^\circ\text{C}/10\tau$ H_2 prebake and $850^\circ\text{C}/10\tau$ growth, carbon was detected at a relatively constant level of $\sim 10^{17}\text{cm}^{-3}$ within the epilayer with a small peak of $\sim 1.2 \times 10^{17}\text{cm}^{-3}$ at the substrate interface; however, TEM analyses showed no disruption of epitaxial growth or evidence of defects at the interface.

Considering alternative ex-situ cleaning techniques, Miyauchi et al /63/ dipped the wafers in a 5% HF solution for 20 secs. (with no subsequent water rinse) immediately prior to reactor loading. It was reported that impurities such as C, O, F and Cl could not be detected at the substrate interface after a 30 min. $900^\circ\text{C}/100\tau$ H_2 prebake and growth under the same conditions: however, the SIMS O_2 and C background levels were approximately two and one order of magnitude higher respectively, compared with those of the present investigation (Figure 7). Sedgewick et al /26/ used an ex-situ RCA clean followed by a 10 sec. dip in 0.5% HF prior to placing the wafers in a load-lock for 10 mins. in Ar. The wafers were subsequently prebaked in H_2 for 10 mins. at $950^\circ\text{C}/760\tau$ followed by SEG growth using the DCS/ H_2 system within the temperature range 600°C - 850°C : the SEG layers were reported to be of good quality with featureless substrate interfaces (TEM). However, it is well known that aqueous HF treatments can result in various surface contamination, e.g. particulate, heavy metal and carbon. Using an alternative HF-vapour treatment (5 secs. 1:2 ; H_2O : 49% HF) immediately prior to reactor loading, Lou et al /64/ concluded that a native (or chemically regrown) oxide is removed and replaced by a temporary passivating layer of HF or other fluorine species, which makes the subsequent in-situ clean more efficient (15 mins. $900^\circ\text{C}/6\tau$). Similar vapour etching of oxide layers on Si has been reported by Van der Heide /65/ (HF/ H_2O , N_2 carrier) and Miki et al /66/ (anhydrous HF gas): the latter authors reported that native oxides were selectively removed without affecting thermal or CVD oxides, and CVD borosilicate glass (BSG).

Following the ex-situ HF-vapour treatment and in-situ H_2 prebake discussed above, Lou et al /64/ reported improvements in both the quality and reproducibility of subsequent epitaxial growth (800°C - $830^\circ\text{C}/0.6\tau$) by adding a small (0.025%) amount of DCS to the H_2 ambient shortly after reaching the prebake temperature. These authors suggested a number of explanations for this; i.e. gettering of residual H_2O , by the "burying" of SiO_2 nuclei before growth into large islands or a coherent film, or via a gaseous reaction with effective by-product removal. The latter could possibly occur via the disproportionation reaction (c) at the oxide surface due to the reaction of dissociated source-gas atoms, in addition to that occurring at the oxide-substrate interface: a similar precleaning mechanism has been discussed by Kunii and Sakakibara /67/ using the Si_2H_6 - H_2 system. Lou et al further suggested that the addition of DCS in some way "protected" the exposed SiO_2 -Si interfaces from undercut during prebake, although no suggested mechanism was given.

Other in-situ cleaning techniques include the use of various plasmas to remove the surface oxide; e.g. Anthony et al /68/ reported that a remote H_2 plasma cleaning technique ($250^\circ C$, $45m\tau$) was effective in removing C,N and O from a Si surface that had been ex-situ RCA cleaned and given a final dilute HF dip with UHP water rinse (60 secs. 40:1, $H_2O:HF$): the best results were reported for minimum exposure (~ 10 mins) of the wafers to air following the HF dip. The above work has been extended more recently by Hsu et al /69/. Yew and Reif /70/ used an ex-situ aqueous HF and UV-ozone /71-73/ treatment to grow a $9-12\text{\AA}$ protective oxide layer and reduce the surface carbon contamination, followed by an in-situ H_2 -Ar plasma sputter to remove the latter oxide.

Using the above treatments, these authors reported the growth of high quality SEG layers at $800^\circ C$ using ULPCVD of SiH_4/H_2 through growth-sputter cycles (cf Jastrzebski et al /74/) with the sputter being performed using the same H_2 -Ar plasma process used for the initial oxide removal. Burns /75/ reported the low temperature removal of native oxide from Si by passing a gas mixture of NF_3 and H_2 for 30 mins. over a substrate held at $580^\circ C$ (0.25τ): following this prebake, the growth of good quality epitaxial layers was reported using SiH_4-H_2 at $800^\circ C/0.25\tau$. Nagira et al /76/ reported that after an ex-situ H_2 prebake at $900^\circ C/60\tau$, good quality single crystal Si could be grown at temperatures down to $800^\circ C$ (60τ) using a conventional barrel-type reactor with the DCS- $SiH_2F_2-H_2$ gas system. These authors proposed that the added difluorosilane acted to remove any remaining oxide (i.e. RCA regrown) from the Si surface (presumably in the initial stages of deposition), thus allowing good quality epitaxial growth.

De-Boer and Meyer /77/ have reported the epitaxial growth of Si and SiGe at atmospheric pressure down to a temperature of $600^\circ C$ (DCS- GeH_4-H_2) and as previously mentioned, Sedgewick et al /26/ have also reported low temperature SEG at atmospheric pressure ($600^\circ-800^\circ C$: DCS- H_2): in both cases, the reported H_2O partial pressures during growth of $\sim 8.0 \times 10^{-6}\tau$ and $\sim 2.0-8.0 \times 10^{-5}\tau$ respectively, are orders of magnitude higher compared with the extrapolated values taken from the data of Ghidini and Smith /18/ where SiO_2 would be expected to form; i.e. $\sim 10^{-6}\tau$ at $850^\circ C$ and $\sim 10^{-10}\tau$ at $600^\circ C$. Hence, a UHVCVD system as designed and reported by Meyerson et al /80/ may not be necessary for the production of low temperature SEG layers.

The present data shows that when using a combination of ex-situ RCA and in-situ H_2 prebaking techniques, the Si surface oxide can be effectively removed, thus allowing the growth of excellent quality single crystal SEG at temperatures at least down to $850^\circ C$: the quality of the latter materials has been established by the present author using a range of techniques including defect etching, TEM, atomic absorption, SIMS and photoluminescence /78/ and by other authors, e.g. Silvestri et al, /79/ for similarly grown material. However, the foregoing demonstrates that by the use of more sophisticated ex-situ and in-situ precleaning techniques involving HF treatments, reactive plasmas and/or the use of additional gases during the prebake and/or deposition phase, the growth of good quality epitaxial material (SEG) can be extended down to temperatures in the region of $600^\circ C$: this can be achieved using either a UHVCVD system, or alternatively, a conventional atmospheric reactor where the H_2O partial pressure within the growth chamber is minimised using a load-lock.

Having provided a satisfactory preclean, the growth of good quality SEG now depends upon the optimisation of a new set of variables, including the main ones of temperature, pressure and gas flow, to obtain full control of selectively, thickness uniformity, sidewall faceting, defect generation and autodoping. Selectivity is achieved at the higher growth pressures using DCS-H₂ with additional HCl injection (as used mainly in the present investigation) or at the lower growth pressures using just DCS-H₂ /25/. In both cases, the HCl injected and/or naturally produced by the chemical reactions occurring during deposition suppresses the polysilicon nucleation on the oxide and/or etches any nuclei formed. Selectivity is also improved by using an oxide as opposed to a nitride field area, and pure H₂ carrier gas /20/. Unlike SiCl₄ /24/, DCS was reported by Borland and Drowley /1/ to exhibit no selective range at atmospheric pressure; however as mentioned above, this has now been reported by Sedgewick et al /26/. Considering the alternative use of the SiH₄-H₂ system, Regolini et al /25/ reported SEG (oxide field) over the temperature range 950°-1100°C at 1.87(G_R-0.4μm.min⁻¹): however, for growth temperatures below 950°C it was found necessary to add ~10% HCl to the source gas to maintain selectivity down to 650°C (G_R ~10Å.min⁻¹). Yew and Reif /70/ reported SEG (oxide field) at 800°C using a ULPCVD system with either pure SiH₄ or SiH₄-H₂. Using 3.5-110m⁷ of SiH₄, a critical SEG thickness of ~800Å could be grown before polysilicon nucleation occurred on the oxide: the critical thickness was increased to 1300Å by the use of SiH₄-H₂ (2-6m⁷ SiH₄ ; 7m⁷ H₂). The above work was extended by Yew and Reif /81,82/ to incorporate growth-sputter cycles, using an H₂/Ar plasma (cf Jastrzebski et al /74/)hence giving an extended layer thickness range: the sputter etch was reported not to induce any observable damage or defects into the SEG layer.

With respect to the foregoing, a chlorinated source gas system such as DCS/H₂ would appear to offer the most versatile operational capability for the production of selective Si layers at low growth temperatures, using a conventional reactor system at either reduced or atmospheric pressure.

The film thickness uniformity of SEG layers depends significantly upon the growth conditions. At the higher growth temperatures within the diffusion controlled regime, the local-loading effect /8/ causes a variable growth rate depending upon the pattern detail of masked to unmasked areas. Under these conditions, the effect can be controlled by using a specific HCl flow rate where the growth rate becomes pattern insensitive: however, a more versatile approach is the elimination of local-loading by the use of the lower growth temperatures within the kinetic regime. The operational mode of an epitaxial reactor system can be characterised by the value of the Sherwood number /29/.

Sidewall faceting is dependent upon the dielectric material (or sidewall coating) used, the substrate interface profile, sidewall orientation, growth temperature, time and HCl partial pressure. For growth confined within seed-windows, facet free SEG is obtained when using oxide or nitride sidewalls with main {100} orientation having sharp profiles at the oxide-substrate interface. Faceting at the off-orientated corners of the structures can be reduced by using the lower HCl flows /32/ or eliminated by using a negative field area pattern /9,10/. ELO structures display a number of different facets, with the latter being controlled by the HCl partial pressure during growth. Coalesced ELO structures can be produced void-free by varying the shape of the approaching growth fronts to possess large {011} components /30/.

Defect generation during both SEG and ELO depends upon the crystallographic orientation of the sidewall and the deposition conditions: in general, no defects are observed for {100} but many for {110} orientation. For SEG regions, the level of defects generated for {110} orientation when using the higher growth temperatures (i.e. diffusion control), is observed to decrease with decreasing temperature and increasing HCl flow. However, the latter level of defects can be considerably reduced by using the lower growth temperatures (and hence normally the lower pressures) within the kinetic control regime, even in the presence of relatively large oxide undercuts: under these conditions, the HCl flow used depends upon the particular source gas and total pressure used. Oxide sidewalls produce the lowest defect densities, with nitride and polysilicon coatings inducing increasing levels respectively /1/. The generation of defects is related to the formation of displaced hollow-bridge sites /9,10/: these occur predominantly at undercut regions in the $\langle 110 \rangle$ sidewall direction, but are also generated for off-orientated sidewalls and at "rough" undercut regions in the $\langle 100 \rangle$ direction. In contrast, ELO regions are observed to exhibit twins in the {110} sidewall direction down to a growth temperature of at least 800°C /30/, with non observed for {100} orientation.

SEG layers can be conventionally in-situ doped using an external dopant source, or via autodoping from, e.g. a "buried layer" structure. Basic p-n junction device characteristics show junction leakage currents to depend significantly upon the exact nature of the sidewalls in terms of their total length, number of corners and orientation, with main {100} orientation displaying comparatively superior characteristics /10/: the latter basically relates to lower levels of sidewall faceting and defect generation. In this respect, when using the lower growth temperatures within the kinetic regime, SEG isolated devices have displayed superior leakage characteristics compared with equivalent LOCOS isolated structures, /42/.

A number of significant breakthroughs have been made in the growth of selective silicon epitaxial layers using low temperature/low pressure conditions, and more recently, load-locked atmospheric pressure reactors. Both ex-situ and in-situ pre-cleaning techniques have been developed and optimised, which provide high quality surfaces for growth. The DCS-H₂-HCl and DCS-H₂ SEG processes as used in the present work are considered to provide the best compromise between ease of use, growth rate, selectivity and other operational parameters for the deposition of submicron SEG layers for advanced submicron VLSI applications: the process could be further improved by using more advanced ex-situ and in-situ cleaning techniques enabling growth down to lower temperatures. Specific problems still need to be solved, but SEG holds great promise for future VLSI and ULSI technologies, where the technique has the capability to produce novel device structures with simplified processing schedules and downscaling capability.

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