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MOCVD OF TANTALUM PENTOXIDE FOR LARGE-AREA ULSI CIRCUIT WAFERS

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Abstract - Ta$_2$O$_5$ films of 10-150 nm thickness were prepared by oxygen-assisted pyrolytic LPCVD at 450-490°C from tantalum penta ethoxide and O$_2$ with N$_2$ diluent. Silicon wafers 150 mm in diameter were used as substrates with a novel LPCVD reactor. The films were annealed in dry O$_2$ at 700-800°C. Compositional, structural, and electrical evaluations demonstrate that these uniform, pure, and conformal Ta$_2$O$_5$ films are a viable alternative dielectric suitable for advanced megabit DRAM applications.

Introduction

Current types of silicon MOS memory devices use SiO$_2$ or Si$_3$N$_4$/SiO$_2$ thin films as capacitor dielectrics. Since future generation ULSI circuits with decreased feature sizes would require excessively thin films for these low-dielectric constant materials, dielectrics with much higher dielectric constants are a logical alternative. The properties of tantalum pentoxide, Ta$_2$O$_5$, are especially attractive for this application.

The formation of Ta$_2$O$_5$ films has been studied extensively over the years by anodic oxidation [1] and thermal oxidation [2] of tantalum films, by rf sputtering [3,4], and by chemical vapor deposition [5-8]. The formation of Ta$_2$O$_5$ (and other high-dielectric constant films) from metal halides and organometallic reactants by CVD has been reviewed recently [5]. Previous CVD studies based on the metalorganic compound tantalum penta ethoxide, Ta(OC$_2$H$_5$)$_5$, as the starting reactant have led to encouraging results [6-8]. However, as-deposited films did not have sufficiently high dielectric breakdown strength, probably due to carbon contamination from the source reactant, and required annealing at 800-850°C in O$_2$ or O$_3$. Furthermore, in these feasibility studies, film deposition parameters were not optimized for the large-area substrates required in ULSI fabrication.

In this paper, we describe the formation of Ta$_2$O$_5$ films by thermal LPCVD in a novel, single-pass, laminar flow reactor from Ta(OC$_2$H$_5$)$_5$ as the source material. The keys to obtaining excellent uniformity of the films over large-area substrates are control of residence time, precise temperature control, and optimal oxygen-to-Ta source ratio.
Experimental

The tantalum penta ethoxide source (Cerac) was 99.999% pure and was used without further purification. The vaporized source liquid was carried by nitrogen and mixed with oxygen just before being introduced into the reaction chamber. Both O\textsubscript{2} and N\textsubscript{2} must be ultradry and ultrapure. Typical deposition and annealing conditions are listed in Table 1. Both planar and trench etched 150-mm diameter silicon wafers were used as test substrates.

The reactor is an automated, thermal LPCVD disk system from Lam Research Corporation. It is designed for precise control of gas flow dynamics, reactant concentration across the wafer load, process temperature, and system pressure. Gas flow is laminar, single-pass and cross-flow. Gas-phase nucleation of particles is minimized since no gas recirculation occurs.

The films have been characterized by x-ray photoelectron spectroscopy (XPS, ESCA), x-ray diffraction (XRD), Rutherford backscatter spectroscopy (RBS), and scanning electron microscopy (SEM). The film thickness and refractive index were measured by ellipsometry. Particle densities were scanned with a standard particle counting instrument. Electrical characteristics were measured from metal-oxide-semiconductor (MOS) capacitors fabricated from the Ta\textsubscript{2}O\textsubscript{5} films on Si with Al gate electrodes of 1 mm in diameter. A post-metallization anneal of 30 min in forming gas at 450°C was applied. The MOS capacitors were then measured for dc current-voltage (I-V), high-frequency (1 MHz) capacitance-voltage (C-V) characteristics, and leakage current density vs. gate voltage properties.

Results and Discussion

The rate of film deposition as a function of substrate temperature is shown in Fig. 1 for the working range of 450-490°C. The Arrhenius relation over this narrow, optimal temperature interval indicates an energy of activation of 31.5 kcal/mol. The uniformity of film thickness over 150-mm diameter substrate wafers is $\leq$2% at 1 s for films of approximately 30-nm thickness (within wafer and wafer-to-wafer). Average added particle density (calculated from 100 runs) is less than 0.2/cm\textsuperscript{2} for particle sizes of 0.3 $\mu$m and larger (with 6-mm edge exclusion). Since the film deposition under the conditions stated in this low pressure reactor are surface-controlled, one can expect excellent conformality. Figure 2 demonstrates that this is indeed the case. The SEM cross-section micrograph with 7.2 $\mu$m deep trenches of 0.78-$\mu$m center width shows a uniform 0.15 $\mu$m thick conformal film of Ta\textsubscript{2}O\textsubscript{5} on Si.

The ESCA survey spectrum in Fig. 3 is that for a typical Ta\textsubscript{2}O\textsubscript{5} film deposited at 470°C followed by 2 min of sputter etching with Ar$^+$ ions at 4 KV energy to remove surface impurities. No detectable carbon or other impurities are contained in the interior of the film. The Ta:O ratio derived from ESCA data is 1:2.6. The as-deposited films are amorphous and relatively dense, with an index of refraction of 2.19 and a low etch rate of 8.0 nm/min in 25% aqueous HF solution at room temperature.

An 8.0 nm thick mixed region of Ta, Si, and O was detected in the RBS spectrum of Fig. 4. The presence of a thin layer of SiO\textsubscript{2} below the Ta\textsubscript{2}O\textsubscript{5} film was reported previously and is thought to grow mainly in the oxygen atmosphere of the CVD process.
reactor immediately prior to deposition of the Ta$_2$O$_5$ film, or it could be due to the oxidation of Si by Ta$_2$O$_5$ at the interface [6-8].

Figure 5 shows the compound index of refraction as a function of film thickness for Ta$_2$O$_5$ layers deposited at 470°C. A similar plot of effective dielectric constant *versus* film thickness for a large number of samples from different process runs is presented in Fig. 6. Calculated curves based on 2.0 nm and 3.5 nm of SiO$_2$ interface layers have been included to show their effects on the Ta$_2$O$_5$ dielectric constant values. The above data were obtained with an Hg probe electrode. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of thin Ta$_2$O$_5$ films (13.0 nm) had a C/Cox of 0.95 at zero flatband voltage and an actual dielectric strength of 2.8 MV/cm at 1E-6 A.

Figure 7 shows a Schottky plot of the leakage current density for a MOS capacitor fabricated with evaporated aluminum gate electrodes. The film was annealed at 800°C for 10 min in dry O$_2$ prior to electrode formation. The leakage current density is lower for annealed films compared with those that are as-deposited. The leakage current density appears to be lower for films deposited in this system than those from cold wall reactors. We believe this is due to higher oxygen incorporation in the as-deposited films using the single-pass cross-flow LPCVD reactor. Detailed experiments are underway to quantify these effects.

Annealing studies were performed to investigate the effects of post-deposition heat treatment on electrical properties of the films that may occur due to changes in their structure. As-deposited Ta$_2$O$_5$ films were found to be amorphous by XRD. It is known that annealing causes crystallization of the films to β-Ta$_2$O$_5$ [8]. The dielectric breakdown strength was observed to increase with higher anneal temperature. Furthermore, the feasibility was demonstrated for dry-etching vertical profile patterns in photoresist-masked Ta$_2$O$_5$ layers by CF$_4$/CHF$_3$/Ar chemistry in a commercial etcher (Rainbow 4500, [9]).

We have also successfully deposited thin films of niobium pentoxide by oxygen-assisted pyrolysis of niobium penta ethoxide, Nb(OC$_2$H$_5$)$_5$, analogous to the conditions described for Ta$_2$O$_5$.

Conclusions

A process has been presented for depositing films of Ta$_2$O$_5$ over large-area substrates. Optimum temperature under LPCVD conditions is 470°C. These films are amorphous as-deposited and yield, for our samples, the highest dielectric breakdown strength of >4.0 MV/cm when annealed at 800°C in O$_2$. I-V characteristics of MOS capacitors from typical as-deposited films show low leakage currents and dielectric breakdown fields centered at 2.8 MV/cm. The dielectric constant of the films is about 23, and thickness uniformity over 150-mm substrate wafers has variations of only 2% or lower. Particle density is less than 0.2 added (≥0.3-μm) particles per cm$^2$, and the films are conformal, even in deep and narrow trenches. The keys to uniform deposition over large-area substrates are precise control of residence time, temperature, and O$_2$ incorporation by means of a special LPCVD reactor system designed for optimal film deposition.

Preliminary electrical characterization of the films indicate that they are potentially applicable as a storage capacitor dielectric for advanced 64 megabit DRAM devices.
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References


/9/ Rainbow 4500 Oxide Etcher, Lam Research Corporation.
### Table 1

**Typical Deposition and Annealing Conditions**

#### Deposition:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
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<tr>
<td>Ta (OC$_2$H$_5$)$_5$ source temperature</td>
<td>40°C</td>
</tr>
<tr>
<td>Source vaporizer temperature</td>
<td>200°C</td>
</tr>
<tr>
<td>Delivery tubing temperature</td>
<td>120-140°C</td>
</tr>
<tr>
<td>Gas flow rate (N$_2$+O$_2$)</td>
<td>3-6 slpm</td>
</tr>
<tr>
<td>Mole ratio O$_2$/Ta (OC$_2$H$_5$)$_5$</td>
<td>120:1</td>
</tr>
<tr>
<td>System pressure</td>
<td>0.4-0.6 torr</td>
</tr>
<tr>
<td>Deposition temperature</td>
<td>450-490°C</td>
</tr>
<tr>
<td>Deposition time</td>
<td>5-40 min</td>
</tr>
<tr>
<td>Deposition rate</td>
<td>2.0-10.0 nm/min</td>
</tr>
<tr>
<td>Ta$_2$O$_5$ film thickness</td>
<td>10-150 nm</td>
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</table>

#### Annealing:

<table>
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<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Oxygen flow rate</td>
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<tr>
<td>Substrate temperature</td>
<td>700-800°C</td>
</tr>
<tr>
<td>System pressure</td>
<td>760 torr</td>
</tr>
<tr>
<td>Annealing time</td>
<td>10-30 min</td>
</tr>
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</table>
Figure 1. Ta2O5 deposition rate as a function of deposition temperature. The curve shows the process is surface reaction rate limited.

Figure 2. Backscatter image of test sample cross-section showing uniform and conformal coverage of deep trenches in silicon with LPCVD Ta2O5. The scale indicates a dimension of 2.00 μm.

Figure 3. ESCA survey spectrum of a typical Ta2O5 film deposited at 470°C.
Figure 4. RBS spectrum of Ta2O5 on Si showing a thin interface mixed region containing Ta, Si, and O.

Figure 5. Dependence of compound index of refraction on film thickness.

Figure 6. Dependence of effective dielectric constant on film thickness for as-deposited Ta2O5. Calculated values based on 2.0 nm and 3.5 nm of SiO2 interlayer are shown for comparison.

Figure 7. Leakage current density vs gate voltage for MOS capacitors fabricated from a Ta2O5 film annealed for 10 min at 800 °C in dry O2.