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Fabrication of 30 nm inter-electrode gap co-planar tunnel junctions with buried electrodes

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Résumé. — Des jonctions tunnels co-planaires avec une largeur de coupure inférieure à 30 nm ont été fabriquées en utilisant un masqueur électronique à 20 keV et un procédé de lift-off d'un alliage Au-Pd. Les électrodes de la jonction ont moins de 200 nm de largeur et sont enterrées à la surface de SiO₂. La mesure de la topographie de la surface de la coupure avec un microscope à force atomique montre une rugosité de moins de 1 nm.

Abstract. — Co-planar tunnel junctions with a gap length in the 30 nm range have been fabricated using a 20 keV scanning electron microscope and a Au-Pd lift-off. The junction electrodes are less than 200 nm in width and are buried in the SiO₂ substrate. This makes the gap surface accessible for atomic force microscope characterization and for local modification.

1. Introduction.

There is a growing interest in the fabrication of very small tunneling junctions. These junctions are required to make high temperature superconductor Josephson junctions [1], to observe the Coulomb blockade at room temperature [2], to study the conductance properties of split gate field effect transistor [3] and to measure the resistance of a molecule [4] or of a single chain of atoms [5]. For many of these applications, like Josephson junction or Coulomb blockade, layered (sandwiched) tunnel junctions pioneered by Giavert and co-worker [6] are well appropriated. But for split gate transistors and for atomic or molecular electronic, co-planar tunnel junctions are necessary [4].

A co-planar tunnel junction is often formed when a lift-off does not work well [7]. In this case, one can randomly observe 7 to 40 nm cuts in fabricated metallic nanowires [7, 8]. Reproducible co-planar junctions with a 100 nm gap length were first produced by Schyfter and co-worker using e-beam lithography and sputter etching [9]. The 10 nm range was recently reached by Fischer and co-worker using e-beam nanolithography and lift-off processes to

fabricate very narrow quantum transistor gates [10]. In their structures, the access to the gap surface is difficult for example with an atomic force microscope (AFM) due to the large 15 nm height of the electrodes.

This is a problem for applications like molecular electronic which would require a measurement of the surface gap corrugation.

We present here a process to fabricate co-planar tunnel junctions with a gap length in the 30 nm range and with the junction electrodes buried in the substrate. The advantage is that the surface of the gap can be made at the same or higher in altitude than the electrodes. Therefore, AFM images of the surface of the gap are readily obtained because the access of the AFM tip to the gap is no more crowded by lateral interactions between the tip apex and the edge of these electrodes.

2. Co-planar tunnel junctions fabrication.

In standard e-beam lithography, a positive resist is exposed to a very small diameter e-beam to draw pixel by pixel the desired patterns. The smallest in width lines are obtained by a single passage of the beam. Therefore, with a positive resist, an obvious way to fabricate a small break in such a line is to stop the resist exposure during a determined number of pixels at the position, in the wire, where the tunnel gap has to be fabricated [11]. Ideally, the number of pixels jumped corresponds to the desired break length W_0 . But the break length is limited by proximity effects which enlarged the effective beam exposure diameter in the resist. Therefore, even after a perfect lift-off, the observed break length W_g in the wire will be always different from W_0 . Moreover, the minimum W_g value with a PMMA resist will be around 4 nm due to the finite 2 nm PMMA molecule diameter [12]. This pixel jump technique was used to define the junction gap on the SiO_2 surface.

A Si(100) wafer was washed with a HF solution to remove the native oxide layer. A controlled in thickness and in composition SiO_2 oxide layer was then formed at 1 100 °C under an oxygen flux during 40 minutes after a 30 minutes heating. The 110 nm thickness of the SiO_2 layer so deposited was controlled by ellipsometry. A 50 nm in thickness 950 K 2 % solid PMMA layer was directly deposited on the SiO_2 layer surface, annealed for 90 s at 150 °C on hot plate and controlled by ellipsometry. The patterns were drawn in the PMMA resist using an electron pattern generator EPG 102 from Thomson equipped with a Cameca electron beam column. The electron beam in the column is generated by a heated tungsten filament. The dose used is 131 $\mu\text{C}/\text{cm}^2$ with an accelerating potential of 20 kV.

Each pattern (a junction + the electrodes + the connection pads) is a 41 μm long and 2.8 μm width line with in the middle a 1 μm long and around 100 nm width wire. To fabricate this wire, the PMMA exposure was done with a single e-beam scan. The tunnel gap is fabricated during this scan in the middle of the wire. The beam blanking of the EPG 102 was used to stop the exposure for a certain number of pixels corresponding to a guess W_0 . The writing field is a $75 \times 75 \mu\text{m}^2$ square. The EPG 102 pattern generator divides each field in $4\,096 \times 4\,096$ pixels. This leads to a minimum W_0 increment of 18.30 nm. We have not tried to optimize the width of the central 100 nm wires. But we can fabricate 40 nm in width buried nanowires [8].

Following its exposure, the PMMA was etched with a standard developer [8]. In a standard lift-off process, metallization follows the PMMA development. But to bury the full metal pattern in the SiO_2 layer, the SiO_2 surface discovered by the developed PMMA was etched in an ammonium fluoride solution. This etching shortens also the gap length since it occurs vertically in the SiO_2 surface but also laterally in the SiO_2 under the PMMA layer. With a good control of the etching rate (presently 5.3 nm per minute), the gap length will be smaller than the 18.30 nm increment provided by the EPG 102. The inconvenient is that the width of

the junction electrodes increases also with this under-etching since it is not orientation selective in SiO_2 .

Different etching durations were tried between 60 and 240 s to test this idea, a 100 s duration corresponding to a 10 nm etched depth. The lift-off was done as previously [8] after 15 nm gold/palladium alloy evaporation, lifting only the PMMA and not the SiO_2 layer. Using a standard optic micro-lithography, aluminium pads can be printed on the gold/palladium buried patterns to get the large area required for the ultrasonic bonding of the electrical contacts. This last process do not changed the apparence of the gap nor of the 100 nm wires.

3. Process characterizations.

Using a JEOL 840-A SEM, the relationship between W_0 and W_g was investigated, starting from a large 370 nm W_0 value corresponding to a jump of 20 pixels (Fig. 1). In general, around 1 400 junctions were fabricated on a single wafer. For each run, more than 200 were investigated to get the values reported in figure 1. In general, there is a small 10 nm dispersion in the width of the 2 μm pads and 100 nm wires. But a large 30 to 50 nm dispersion is observed on the gap length which preclude yet any characterization of the under-etching step (see Fig. 1). This dispersion seems to be due to mechanical vibrations of the EPG 102 not enough compensated by the interferometry control of the wafer position.

Fig. 1. — Experimental variation of the gap length W_g as a function of the number of pixel jumped reported in the W_0 equivalent length. The gap length were SEM measured. (O) is for a run with a 120 s under-etching and (+) for a 180 s under-etching. The line follows the average value of these measurements.

The AFM Nanoscope II was used to confirm the SEM measurement of the gap length and to characterize the surface corrugation in the gap. Figure 2a presents a large AFM top view of a 28 nm gap co-planar tunnel junction with its 160 nm electrodes and the beginning of its large contact pads with a 2.8 μm width. The tunnel gap is apparent in the middle of these electrodes, but not resolved. Figure 2b presents a more detail AFM image of the same junction, but in the gap region. The pic to valley corrugation of the SiO_2 surface is 1.6 nm and the corrugation of

a)

b)

Fig. 2. — a) A top view AFM constant force image of a 28 nm gap in a gold/palladium 160 nm in width wire. The 2.8 μm contact pads are also imaged. Image size is $4 \times 4 \mu\text{m}^2$ and altitude is 15 nm from black to white. b) A 3D view AFM constant force image of the same 28 nm junction but taken in the junction region. The M and M' end of each junction metallic electrode is indicated by the superposed a-a' and b-b' black lines. Image size is $128 \times 128 \text{ nm}^2$.

the metallic wire surface is 3.4 nm, indicating the presence of small grains due to the gold/palladium metallization.

It is difficult in figure 2b to identify the SiO_2 surface in the gap between the end of the two electrodes since the local topography is perturbed by a small 1 nm protuberance as in many junctions of an equivalent size fabricated with this process. Therefore, there is an incertitude on the real gap length in such a small gap junction. If this bump is a metallic lift-off residue, the gap length is certainly lower than 20 nm. If this bump is non metallic, the gap length is around 28 nm. Different tip apex were used to better resolve the surface gap corrugation. But we did not succeed in determining the composition of this protuberance. A cross section of this junction along its axis indicates that beside this protuberance, there is less than 0.5 nm difference between the metal electrode surface altitude and the average SiO_2 gap altitude.

Figure 3a presents a 3D view of a large 34 nm gap. The shape of the electrodes in this junction corresponds well to an under-etching process controlled by the restricted diffusion of the etcher at the PMMA- SiO_2 interface. The gap surface altitude measured in average on single AFM scans is higher by 1 nm than the surface of the two electrodes. On this gap, the surface pic to valley corrugation is lower than 0.63 nm and comparable to the original SiO_2 layer surface corrugation before the process. As expected, detailed AFM constant force images of the gap surface can be obtained as presented in figure 3b. For this gap length, there is no incertitude on the length measured as compared with the gap presented in figure 2b.

For an amorphous SiO_2 surface, it is difficult to reach atomic resolution. Therefore, the 0.5 nm surface corrugation measured on the gap (Fig. 3b) is a proof that, after the lift-off, we have succeeded in well cleaning the wafer. For each gap region, this was facilitated by the gap

Fig. 3. — a) A 3D view AFM constant force image of a 34 nm gap length junction. The end of each junction metallic electrodes is indicated by the letter M and M'. Image size is $300 \times 300 \text{ nm}^2$. b) A detail 3D view AFM constant force image of the surface corrugation on this gap. Image size is $35 \times 35 \text{ nm}^2$. The superposed a-a' and b-b' black lines indicate the termination of the junction electrodes.

b)

Fig. 3 (continued)

altitude which decreases the probability of resist accumulation between the edge of the electrodes. This opens the way of AFM (or STM) atomic resolution in such a gap if our process is transferred on the surface of more appropriate materials.

4. Conclusion.

We have shown the possibility to fabricate co-planar tunnel junction with a gap in the 30 nm range where the tunnel junction electrodes are buried in the surface layer. On the top, this makes apparent the surface of the junction gap for further AFM characterization or local transformation.

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