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Speed optimization of Josephson direct coupled logic

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Résumé. — Une conception nouvelle en logique Josephson à couplage direct (ADCL) est développée qui réalise l'optimisation en vitesse avec des jonctions supraconductrices picosecondes ($R_N \times C = 2\text{ps}$). Chaque porte est constituée par une cellule d'entrée logique et d'un buffer de sortie (porte OU), ce qui apporte une standardisation efficace de la conception. La conception minimise les effets de retard à la commutation, les effets d'entrance et de sortance, pour réduire les dégradations de vitesse dans les conditions opératoires de circuits. On présente la méthodologie de l'optimisation en vitesse qui est obtenue simultanément avec des marges statiques et dynamiques importantes, une faible dissipation de puissance, une capacité d'intégration élevée. Les caractéristiques principales de la conception ADCL sont une suppression du shunt d'entrée de la porte OU, une impédance de ligne signal importante, une amplification en tension et en courant, une standardisation des portes. La vitesse maximum à une polarisation voisine du seuil ($\geq 95\%$) est 2,5 ps pour la porte OU et 5 ps pour la porte ET. Avec une entrance/sortance de 2/2 et à une polarisation à 80 % du seuil qui donne des marges $\neq \pm 20\%$, les temps de communication précédents croissent seulement à 5 et 10 ps avec une consommation en puissance de seulement 3 μW . Le produit puissance $\times$ retard correspondant de la porte OU est 15 aJ.

Abstract. — An advanced design of direct coupled Josephson logic (ADCL) is developed for optimum speed at the circuit level with picosecond superconducting junctions ($R_N \times C = 2\text{ps}$). Each gate consists of an input logic cell and an output buffer (OR gate) which brings efficient standardization. The design minimizes junction turn-on-delay and loading effects to reduce speed degradations in circuit conditions of operation. The methodology of speed optimization with good static and dynamic margins, small dissipation and large integration capability is presented. The new features of the ADCL gate design are, a suppression of the input resistive shunt in OR gate, a large signal line impedance, voltage and current amplification, a standardization of gate design. The maximum gate speeds at bias near threshold ($\geq 95\%$) are 2.5 ps (OR) and 5 ps (AND). At fan in/fan out ≥ 2 and 80 % of threshold bias giving $\neq \pm 20\%$ operating margins, the gat switching times rise only at 5 ps (OR) and 10 ps (AND) with as little as 3 μW /gate power dissipation. The corresponding power-delay product of the OR gate rates at 15 aJ.

1. Introduction.

The Josephson direct coupled logic is attractive for superconducting digital circuits as it is practically inductance free [1-2]. A common feature of designs with different names all referred here as DCL is a resistive shunt often in the range of 1 Ω which damps the input junction of the OR gate (Fig. 1a). It is the primary origin of sizeable turn-on-delays (tod) which do not scale down with the junction intrinsic rise time constant $t_c = R_N C$. Large tods in the simple loaded OR gate [3-5] may reach up to 90 % of the gate propagation delay time t_{pd} with junctions of $t_c \approx 1\text{-}2\text{ps}$. For example a standard DCL OR gate

with $t_c = 2\text{ps}$ junctions has a total switching time near 10 ps at a current bias $0.8 I_0$ and a fan-out ≥ 2 [3]. In these conditions there is little circuit speed improvement with the recent fast junctions [6-7]. It must be pointed out that reports in the literature on very short gate switching times refer to junction bias conditions near threshold ($\geq 95\%$) and fan-in/out = 1. In these conditions switching time reductions come mainly from an increase of junction current density and gate design has not much influence. A large reduction of the series matching resistance R_L between gates increases the available current overdrive and reduces the gate tod [6] but brings undesirable impedance mismatch. Conse-

quently DCL gate performances degrade quickly at lower bias and increased fan-in/out as illustrated in the above references. This fact and the technological dispersion of junction critical currents explain why the gate speeds in Josephson circuits (adder, multiplier, ALU...) are comparatively lower than record gate speeds obtained near junction threshold. The same trend exists in other types of Josephson logic circuits i.e. in the recent MVTL logic family [8].

Our preliminary work [3] has shown that any significant speed improvement of DCL gates in bias conditions corresponding to circuit operation requires careful speed optimization of the switching cells. We present here a full account of a new design of DCL gates with speed optimization. It has also low power dissipation and good integration capability. The basic characteristics of this advanced DCL design (ADCL) are a small turn-on-delay of the junctions inside each gate, an efficient transfer of current from gate input to gate output in the sequential switching of junctions, and good isolation between input and output of gates in the off-state. The design features specific to the speed optimization of ADCL OR and AND gates which are the basic blocks in circuits are discussed. The modeling aspects related to an accurate simulation of these picosecond gates are described. The evolution of the threshold characteristics and propagation times are determined as a function of the main parameters.

2. New features of the ADCL design.

The optimization of gate speed is searched in conditions of circuit operation, i.e. fan in/fan out ≥ 2 , nominal dc bias at 80 % of threshold, corresponding to a commonly used bias condition for margins ≥ 20 %, large integration density ($\approx 10^4$ gates for a 1 cm^2 chip and a $1600 \mu\text{m}^2$ OR gate area) to limit inter-chip signal transfers and the important signal degradations and delays at this level. There is some trade-off to perform speed optimization together with high integration and low power dissipation. We discuss the conditions which give minimum degradation of ADCL gate speed compared to junction intrinsic characteristics. The main features of the design are :

- suppression of the resistive shunt on the buffer OR gate input junction,
- large signal line impedance,
- gate voltage and current amplification,
- standardization of gate design.

A standard DCL OR gate is shown in figure 1a, where J_1 , J_3 represent single Josephson junctions while J_2 is constituted with two junctions in series. The shunt resistance R_s across J_1 is present in all previous designs and is responsible of the large tod. It has two important functions : a) it realizes a small

Fig. 1. — Structure of DCL OR gate (a) Standard DCL OR gate with input shunted junction ; (b) ADCL design without shunt for speed optimization (fan in/out ≥ 2) ; (c) same as (b) with unit fan-in/fan-out ; (d) general structure of ADCL gates with standardized OR gate output buffer.

impedance mismatch at J_1 when the latter switches (the control line of impedance $Z_L \neq 15 \Omega$ is loaded with $R_L = Z_L$ in series with J_1 shunted with $R_s \neq 1 \Omega$) ; b) it helps full switching of the isolation junction J_3 as R_s maintains a low voltage across J_1 (Fig. 1a). Then after J_2 starts to switch a large current may flow back temporarily across J_3 . The latter switches beyond the gap voltage. If R_s is removed in figure 1a, it may be shown that junction J_3 cannot switch properly without important modifications of the gate design.

In the ADCL gate design without input shunt R_s (Fig. 1b-c), particular attention is given so that junction J_3 switches fully and reaches a high resistance state, while gate junction J_2 's are minimized. This protects the previous gate against current reflections and allows derivation of the largest part of the bias current I_a towards the gate output. Simulations of several OR gates in series show that switching of $J_3(n)$ in gate n only occurs after gate $(n+1)$ has started to switch. Then part of the bias current available after switching of $J_2(n)$ is fed back temporarily in $J_3(n)$ which may switch in turn. The control current I_c coming from gate $(n-1)$ is reduced after switching of $J_1(n)$ and $J_2(n)$ and cannot inhibit the switching of $J_3(n)$. A detailed

analysis of the OR gate dynamics shows that proper operation of the ADCL design requires a strong increase of output line impedance. A large impedance reduces the current in the output line when the output junction J_2 switches. It increases the drive current sent back in the isolation junction J_3 which switches easily. Then full switching of J_3 is made easy. Then the total bias current of the gate is sent in the output line. A high line impedance also reduces impedance mismatch and accompanying reflections when J_1 is in the resistive state. A standard line impedance Z_L in Josephson circuits is in the 10-15 Ω range. We have found that $Z_L \approx 40\text{-}50\ \Omega$ which is compatible with a $\approx 1\ \mu\text{m}$ technology is a good trade-off. A series resistance $R_L = Z_L$ matches the line when J_1 is in the superconducting state.

An increase of the gate output voltage and impedance is necessary as junction J_1 is not shunted and a large line impedance Z_L is selected. It is obtained by placing two or three junctions in series in both the left and right branches of the ADCL OR gate (Fig. 1b-c) depending on loading conditions. Gates incorporating junctions in series have been already used in circuits [9]. Junction critical currents J_{c_i} are dimensioned to reduce loading effects as in the design of semiconductor logic circuits ($J_{c1} = J_{c3}$, $J_{c2} = 2.5$ to $3 J_{c1}$). This gives adequate switching conditions to the isolation junction J_3 and large current transfer to the next gate input. The small resistive elements (R_1 , R_2) give a gate cell with low sensitivity to trapped flux. Dynamic simulations show that switching performances are not sensitive to the absolute value of these resistances when they are kept small ($\approx 1\ \Omega$).

The optimization of the gate speed requires a careful choice of parameters both for the gate under study and its neighbours. The suppression of the shunt leads to more complex equivalent circuits corresponding to the successive switching of gate junctions. We introduce gate standardization which improves the design efficiency of complex circuits with speed optimization. In the ADCL family, the gate structure presents two parts (Fig. 1d): the input realizes a logic function (OR, AND, EXOR...), the output buffer which is an OR gate and is common to all gates with a given fan-out, realizes the voltage and current amplifications required by circuit fan-out. This allows a precise definition of equivalent generators with parameters (V_c , R_c) to characterize the driving conditions of each gate or junction.

3. Modeling features of the ADCL design.

The above specifications oriented towards speed optimization do not allow a number of standard simplifications found in the literature related to the design of DCL gates. We mention briefly the main parameters relevant to ADCL gate modeling.

3.1 POWER SUPPLY. — Standard DCL designs use the approximation of a constant current power supply. This assumes a large voltage supply on chip V_a and large voltage drop series resistances R_a . Such a choice leads to a large penalty in chip area and strong dissipation in the resistances. The present ADCL design uses the minimum supply voltage V_a giving optimum speed with good margins and a few $\mu\text{W/gate}$ dissipation. However the switching of several junctions in series produces variations of the voltage drop across R_a so that 20-30 % modifications in gate bias currents occur during switching. Then gate bias is modeled here with a constant voltage supply V_a and a series resistance R_a (Fig. 1b-c).

3.2 GATE EQUIVALENT CONTROL GENERATOR AND LOAD. — Control currents in standard DCL designs are assumed constant throughout OR gate switching as $R_s \ll R_L$ (Fig. 1a) so that the impedance seen from the previous gate varies very slightly. The above impedance variation becomes large in the ADCL design and the control current cannot be considered as constant. We present in section 4.2 an equivalent model (V_c , R_c) of the drive circuit of the OR gate. Since gates of the ADCL family have a common output buffer, V_c and R_c depend only on the fan out of the previous gate and not on the logic function performed. Moreover an adjustment of the buffer parameters makes V_c and R_c almost independent of the buffer fan out.

Gate loading also varies strongly during switching in the ADCL design, and figure 2a shows the equivalent circuit of the load of an OR buffer. This circuit has a tree configuration which first stage is constituted by s OR gates in parallel (fan-out= s). In this equivalent active load, the matching series resistance is R_L/s , the critical current of junction J is $s \times J_{c1}$, junction J is loaded by an impedance R_L/s^2 .

3.3 RANGE OF GATE PARAMETER VARIATIONS. — We present a design with $R_N C = 2\text{ ps}$ junctions compatible with present technological realizations based on Nb or NbN technologies [6, 7]. The loaded junctions of $t_c = 2\text{ ps}$ are described in good approximation with the RSJC model [10] where the Josephson current is calculated with the expressions of Harris [11] based on the BCS theory. A shunt resistance R_s represents the subgap excess current of real junction in the NbN technology. In our model $R_s = 10 \times R_N$. A capacitance is also incorporated in the model calculated with $C = 2\text{ ps}/R_N$. The junction critical currents are in the range 50-300 μA and the bias voltage is in the range 10-20 mV to keep power dissipation small. The range of ohmic resistances is 1-50 Ω but may be reduced to 1-5 Ω if series junctions are used in the power supply lines and in the gate-to-gate transmission lines.

Fig. 2. — Equivalent circuits related to ADCL design of OR gate. (a) Output active load of OR gate with fan-out = s . (b) Control generator (V_c , R_c). (c) Equivalent circuit corresponding to switching of junction J_1 in an OR gate with fan-in = 2. (d)-(e) Same as (c) corresponding respectively to switching of junctions J_2 and J_3 .

3.4 DEFINITION OF STATIC MARGINS. — The diagram of static margins in standard DCL design is presented in the current plane (I_a , I_c) where the assumption of constant I_a and I_c holds (Sect. 3.1). This assumption is not valid in the ADCL design and we present the static margins in the (V_a , V_c) plane. V_a and V_c are given in relative units (v_a , v_c) of the maximum gate voltage $V_{a\max}$ defining the gate switching threshold with $I_c = 0$ and $V_{c\max}$ corresponding to $V_{a\max}$.

Variations of V_a do not occur generally on a chip. On the other side, due to scattering of technological parameters, variations of the junction current density or of the metallization resistance per square may be translated in variations of V_a . We have studied the influence of such variations on the gate operation and designs are made to have margins compatible with variations of technological parameters of at least $\pm 20\%$. The margins are calculated using

nominal supply and control voltages $0.8 V_{a\max}$ and $0.8 V_{c\max}$. As V_a and V_c vary proportionally (Sect. 4.2), the gate operating line crosses the origin of the (v_a , v_c) diagram which allows to express the operating margins in analytic form.

3.5 DYNAMIC SIMULATIONS. — The signal waveforms in picosecond ADCL gates differ significantly from the ideal trapezoidal shape assumed in logic designs and also present voltage oscillations due to the a.c. Josephson current (Figs. 5.1, 8.1). Then the turn-on-delay, the propagation delay t_{pd} and the rise time of such gates are less straightforward to define accurately [3, 10]. For example t_{pd} is the delay time between the drive signal and the output gate signal across J_2 both taken, at 50% amplitude (Fig. 5.1 and Fig. 8.1). As for the static margins, precise dynamic data are obtained owing to simulations of gates constituting a tree configuration driven by a ramp input generator (V_c , R_c) with a rise time nearly equal to the OR gate one.

4. OR Gate.

The OR gate which is used as an output buffer in all gates constitutes the basic block of the logic family. Special care is given to its analysis and optimization.

4.1 STATIC OPERATION. — The figure 1b represents an OR gate with $F_{in} = F_{out} = 2$. The input junction has a relatively low critical current $J_{c1} = 75 \mu A$ and receives a strong current overdrive (50 to 150%) when it is activated. If $F_{in} = F_{out} = 1$ (Fig. 1c), $J_{c1} = 50 \mu A$. The isolation junction J_3 has the same critical current as J_1 . The output junction J_2 has a critical current 2.5 to 3 times larger than J_1 which gives a good current drive capability with a fan-out of 2-3. The junction J_2 is constituted (fan-out ≥ 2) with three junctions in series to increase the voltage in the resistive state and transfer a large current in the output transmission lines. An output voltage of 5 mV is obtained as the junctions are biased under the gap after switching. Voltage matching of the two branches of the gate is obtained using two junctions in series for J_3 . The resistances R_1 , R_2 are selected to give the proper current balance between the two branches in the zero voltage state. Simulations show that only their ratio equal to J_{c2}/J_{c1} is important. They are kept small for fast current transfer between the two branches. The feed resistance R_a of the gate is relatively small (45Ω) as the gate operates with a nominal voltage of 10 mV, which gives a very low power dissipation of $3 \mu W/\text{gate}$.

4.2 EQUIVALENT STATIC GENERATOR (V_c , R_c) OF THE OR GATE. — The derivation of simple expressions of the static margins requires to represent

switched junctions with an equivalent resistance. The determination of the generator (V_c , R_c) equivalent to the output of a switched gate driving the followings gate inputs of a tree configuration starts with full numerical simulations of cascaded OR gates and a calculation of the voltages and currents at all important points. Their analysis indicates that the switched junction may be treated approximately as a constant impedance larger than R_N . The dynamic margins obtained from systematic dynamic simulations are compared with the static margins expressed analytically using an equivalent resistance αR_N ($1 < \alpha < 4$) of the junction in the resistive state. The static margins calculated with an equivalent resistance $2 R_N$ fit precisely with the dynamic margins.

The equivalent resistance $2 R_N$ does not correspond to one of the two main static resistive states of the junction characterized by R_s and R_N . Qualitatively, as soon as a gate junction starts to switch, the drive current is derived in another branch of the gate, and while a finite voltage appears across the junction, its bias current initially equal to $0.8 I_c$ (operating bias) is observed to decrease to $\approx 0.5 I_c$ which corresponds to an equivalent resistance $\approx 2 R_N$. From the preceeding results it may be concluded that the assumption of an average resistive state $\approx 2 R_N$ does not affect the accuracy of static margin calculations and one obtains the equivalent circuit of figure 2b the following parameters :

$$V_c = \frac{2 R_{N2}}{2 R_{N2} + R' + R_2} \times V' \text{ and } R_c = R'' \times s + R_L$$

where

$$\begin{aligned} R' &= (2 R_{N1} + 2 R_{N3} + R_1) // R_a \\ R'' &= 2 R_{N2} // (R' + R_2) \\ V' &= V_a \times \frac{2 R_{N1} + 2 R_{N3} + R_1}{R_a + 2 R_{N1} + 2 R_{N3} + R_1} \end{aligned}$$

s is the gate fan-out, R_{Ni} is the normal resistance of junction J_i and $//$ means resistances in parallel.

The table I shows that V_c/V_a and R_c are quite constant with fan-out s if the junction critical currents are properly scaled. Then we may calculate the

Table I. — Variations of the parameters of the equivalent generator (V_c , R_c) of figure 2b corresponding to an OR gate (fan-out=2) versus critical current J_{c1} of junction J_1 . The parameters are $J_{c2}/J_{c1} = 2.75$, $R_L = 45 \Omega$, $R_a = 45 \Omega$.

fan-out	1	2	2	3
$J_{c1} (\mu A)$	50	75	100	150
V_c/V_a	0.48	0.48	0.48	0.48
$R_c (\Omega)$	78	89	78	78

range of variation of the control current I_c . Using $V_c = 0.48 V_a$, $I_c = V_c/R_c$, we find that in the bias voltage range

$$8 \text{ mV} < V_a < 12 \text{ mV} ,$$

I_c verifies $50 \mu A < I_c < 77 \mu A$.

Then the range of critical currents J_{c1} for 20 % static margins is

$$50 \mu A < J_{c1} < 150 \mu A .$$

In the appendix it is shown that $J_{c1} = 50 \mu A$ is also the lower limit of critical currents to maintain at a low level the probability of erroneous switching due to thermal noise.

4.3 STATIC MARGINS OF THE OR GATE. — We determine the static margins of a two input OR gate in the worst case of a single activated input. The static margins are calculated in terms of v_a and v_c (Sect. 3.4). The figures 2c-2e represent the equivalent circuits corresponding to switching of junctions J_1 , J_2 , J_3 . The voltages V_a and V_c vary proportionally (Tab. I : $V_c \approx 0.48 V_a$). The maximum relative bias voltage $v_{a \max} = 1$ occurs when the bias current of J_1 reaches J_{c1} (see Fig. 2c). Then the static margins of the OR gate are calculated.

Margin of junction J_1 :

$$v_{a \min}(J_1) = J_{c1} / [(V_{c \max}/R_c) + J_{c1}]$$

with the values of V_c and R_c in table I.

Margin of junction J_2 :

$$v_{a \min}(J_2) = J_{c2} / (V''/R'')$$

with

$$V'' = \left[\frac{V'}{R' + R_1} + \frac{V_{a \max}}{R_a} \right] \times [(R' + R_1) // R_a]$$

$$V' = \frac{R_L // R_{J_1}}{R_c + (R_L // R_{J_1})} \times V_{c \max}$$

$$R' = (R_L // R_{J_1} // R_c) \quad R'' = [(R' + R_1) // R_a] + R_2 .$$

Margin of junction J_3 : the switching condition of J_3 is less straightforward to obtain as it interacts with the next gates. We take into account all the parameters of the gate as well as the parameters of the neighbouring gates which we assume to be identical. The analytic approach results from systematic dynamic simulations which help to define the limiting switching conditions of J_3 . We consider the worst case where both gate inputs are activated, which corresponds to the maximum input control current. The equivalent circuit is represented in figure 2e. The impedance of J_1 is $\approx R_{N1}$ as J_1 receives a large part of the bias current I_a , and the input control current. The impedance of $J_2 \approx 10 R_{N2}$ as J_2 biased

at a voltage smaller than $3 \times V_g$ i.e. each junction is biased under the gap voltage.

Then $v_{a \min}(J_3) = J_{c3}/I_{J_3}$ with

$$I_{J_3} = \left[\left(\frac{V_2''}{R_2''} + \frac{V_{a \max}}{R_a} \right) \times R_3'' - V_1' \right] / (R_3'' + R_1')$$

$$V_1' = \frac{R_1}{R_{N1} + (R_c/e)} \times V_{c \max}$$

$$V_2' = \frac{R}{R + (R_a/s)} \times V_{a \max}$$

$$V'' = \frac{R_{J_2}}{R_{J_2} + R_2'} \times V_2'$$

$$R_1' = \left(R_{N1} \parallel \frac{R_c}{e} \right) + R_1$$

$$R_2' = \left(R \parallel \frac{R_a}{s} \right) + \frac{R_L}{s}$$

$$R_2'' = (R_{J_2} \parallel R_2) + R_2$$

$$R_3'' = (R_2'' \parallel R_a)$$

The figures 3a-3b illustrate the static margins in the two main cases of fan-in/fan-out equal to 1/1 and 2/2 and a bias voltage $V_{a \max} = 12.5$ mV, a control voltage $V_{c \max} = 0.48 V_{a \max}$. The point N corre-

sponds to the nominal operating gate bias. Its locus is the load line $V_c = 0.48 V_a$. The static margins are limited by the threshold line corresponding to junc-

Fig. 3. — Static margins of OR gate. Lines 1-3 correspond respectively to the threshold conditions of junctions 1-3. (a) fan in/out = 1/1, and $J_{c1} = 50 \mu A$. $R_a = 65 \Omega$, $R_1 = 2.75 \Omega$, $R_2 = 1 \Omega$. (b) fan-in/fan-out = 2/2 and $J_{c1} = 75 \mu A$. The other gate parameters are $R_L = 45 \Omega$, $J_{c2}/J_{c1} = 2.75$, $R_a = 45 \Omega$.

Fig. 4. — Optimization of OR gate static margins corresponding to figure 3 versus: (a) dc bias voltage V_a . (b) junction current ratio J_{c2}/J_{c1} (c) line inductance R_L . The curves 1, 2, 3 in figure 4a-c correspond to the switching limits of junctions J_1 , J_2 and J_3 . Figure 4d shows the power dissipation of OR gate versus transmission line impedance $Z_L = R_L$.

tion J_3 . The latter rotates slightly clockwise with increasing fan-out and a proper adjustment of the junction critical current allows to keep static margins at 20 %. This value reflects accurately the dynamic margins which may be deduced from the variation of t_{pd} versus bias in figure 5.2. It compares also favorably to dynamic margins of DCL OR gates [1].

4.4 VARIATIONS OF STATIC MARGINS WITH PARAMETERS AND POWER DISSIPATION. — The figures 4a-4c express the evolution of the static margins of the OR gate as a function of the main gate parameters and indicate the trends for gate margin optimization. Figure 4a shows that the margins of the three junctions J_1 , J_2 , J_3 improve with increasing voltage bias V_a . Figure 4b shows that the evolution of the junction margins are more contrasted when the ratio J_{c2}/J_{c1} is larger. As it could be expected the margins of junctions J_1 and J_3 increase while the margin on J_2 decreases progressively. Finally figure 4c shows that the evolution of margins is also contrasted when the line impedance $Z_c = R_L$ increases. The margins related to junctions J_1 and J_2 degrade very slowly while the margin on J_3 is strongly improved. This points out that large series impedances improve static margins. Figure 4a shows that larger values of V_a increase static margins. However power dissipation is simultaneously increased and the designer selects the minimum bias voltage compatible with the margins imposed by parameter dispersion. The figure 4b and 4c indicate that an optimum exists in the evolution of the gate margins which lies in the neighbourhood of $J_{c2}/J_{c1} = 2.75$ and $R_L = 45 \Omega$. The figure 4d shows finally the dissipation of the OR gate at constant margins (20 %) as a function of R_L using the gate parameters of table II. This figure which results from the previous ones indicates that power dissipation strongly increases when R_L decrease. For example R_L may be divided by two at a cost of three times the dissipation power. However, this also requires to double junction critical currents from 75 to 150 μA and to increase gate bias from 15 to 20 mV. The power dissipation becomes prohibitive (larger than 20 μW per elementary gate) if R_L is decreased beyond that point.

4.5 DYNAMIC PERFORMANCES. — The design of the OR gate described above has also required systematic dynamic simulations (Fig. 5.1). Switching of three stages of series OR gates forming a tree configuration has been studied. The input is driven with the control generator (V_c, R_c), outputs are terminated with the active load defined in section 3.2. The switching voltage waveforms across junctions J_1 to J_3 are presented in figure 5.1. They show that if t_{pd} is smaller than 10 picoseconds, the total switching time of junction J_2 is larger. The

Fig. 5. — (5.1) Dynamic simulation of an OR gate with $J_{c1} = 75 \mu A$ and $J_{c2} = 200 \mu A$, fan-in/fan-out = 2/2. (5.2) Propagation delay t_{pd} of OR gate ($R_N \times C = 2$ ps) as a function of reduced bias v_a . The gate parameters correspond to figure 3. In both figures the results are given for different loading conditions : (a) fan-in/fan-out = 1/1, (b) fan-in/fan-out = 2/2, (c) fan-in/fan-out = 2/3.

simulations have shown that the suppression of the input shunt to reduce the OR gate turn-on-delay is acceptable only if it is accompanied by the other important design modifications to allow proper in-/out gate isolation in the off-state and give full speed optimization of the gate. The figure 5.2 shows the variation of the propagation time per gate t_{pd} as a function of input/output loading and as a function of bias voltage. The minimum t_{pd} at threshold is near the intrinsic time constant of the junction, i.e. 2.5 ps at a relative voltage $v_a > 0.95$. At $v_a = 0.8$ and fan in/out of 2/2 or 2/3, the present design gives a t_{pd} of only 5 ps. This prediction is at least a factor of two smaller than comparable OR gate previous data. It is obtained at a cost of a very small power dissipation of 3 μW /gate. At this bias $v_a = 0.8$ and fan-in=fan-out=1 the power-delay product is 12 attojoules. This is a reduction of a factor of 6 compared with MVTL OR gate [12]. With a fan-in=fan-out=2 the power-product rises only to 15 AJ, the increase being only due to the longer gate t_{pd} .

5. AND gate.

5.1 GATE STRUCTURE AND OPERATION. — The structure of a two input AND gate is shown in figure 6. The AND gate is derived from the RCJL family [5]. The original gate has no amplification.

Fig. 6. — Structure of a two-input AND gate.

We have added an OR gate as an output buffer following the principle of figure 1d. The input junctions J_1 and J_2 have critical currents in the range of $50 \mu\text{A}$. The junction J_3 is biased at $50 \mu\text{A}$ under its critical current. We find that the critical currents of J_3 and J_5 verify the following empirical relation

$$J_{c3} = 0.8 \times J_{c5} + J_{c1}$$

to obtain coherent static margins for the different junctions. The resistances R and R' are small and of the order of 1Ω .

If a single input (e.g. input 1) is activated, junction J_1 switches at a voltage much lower than V_g and the control current is derived through the resistance network towards J_2 and J_3 . The transferred current is not large enough to switch the junctions and the gate remains in the superconducting state. On the other side if both inputs are activated, the sum of both control currents is large enough to switch the input junction J_3 of the OR gate and the whole gate switches in turn.

5.2 STATIC MARGINS. — The static margins of junctions J_1 to J_5 are calculated as in section 4.3 using appropriate equivalent generators, margin of J_1 (or J_2)

$$v_{a \min}(J_1) = J_{c1} \times R_c / V_{c \max}$$

margin of J_3 (Fig. 7a)

$$v_{a \min}(J_3) = \frac{J_{c3}}{2 V_{c \max} + \frac{R_2 \times V_{a \max}}{R_c} + \frac{R_a \times (R_1 + R_2)}{R_c}}$$

margin of J_4 (Fig. 7b)

$$v_{a \min}(J_4) = \frac{J_{c4} \times (R''' + R_2)}{\left(\frac{V_{c \max}}{R''} + \frac{V_{a \max}}{R_3} \right) \times R''}$$

with

$$V' = \frac{R_{N1}/2}{R_{N1}/2 + R_c/2} \times V_c$$

$$V'' = \frac{R_{J3}}{R_{J3} + R'} \times V'$$

$$R' = \frac{R_{N1}}{2} \parallel \left(\frac{R_c}{2} + \frac{R}{2} + R' \right)$$

$$R'' = (R_{J3} \parallel R') + R_1 \quad R''' = R'' \parallel R_3$$

margin of J_5 (Fig. 7c)

$$v_{a \min}(J_5) = J_{c5} / I_{J5}$$

with

$$I_{J5} = \left[\left(\frac{V_a}{R_3} + \frac{V_a''}{R_a''} \times (R_3 \parallel R_a'') - V_c \right) \right] \times \frac{1}{R_c'' + (R_3 \parallel R_a'')}$$

$$R'' = \frac{R_L}{s} \parallel \frac{R_{N1}}{s} \parallel \frac{R_{J2}}{s}$$

$$R_c' = \left(\frac{R_c}{2} \parallel \frac{R_{N1}}{2} \right) + R' + \frac{R}{2}$$

$$R_a' = \frac{R_3}{s} \parallel R'' \parallel \frac{R_L}{s}$$

$$R_c'' = \frac{R_{N3} \times R_c}{R_{N3} + R_c} + R_1$$

$$R_a'' = (R_a' \parallel R_{J4} + R_2)$$

$$V_c' = \frac{R_{N1}/2}{R_c/2 + R_{N1}/2} \times V_c \quad V_a' = \frac{R''}{R + R_3/s} \times V_a$$

$$V_c'' = \frac{R_{N3}}{R_{N3} + R_c'} \times V_c' \quad V_a'' = \frac{R_{J4}}{R_{J4} + R_a'} \times V_a'$$

The static margins of the gate are shown in figure 7d where lines 1 to 4 represent the switching limits of junctions J_1 (or J_2), J_3 , J_4 , and J_5 in figure 6. The are $\approx 20\%$ at the nominal bias of $0.8 V_a$. They could be increased for the input junctions by a reduction of J_{c1} to $40 \mu\text{A}$. The power dissipation of the AND gate comes mostly from the output OR buffer which gives again a minimum power dissipation of $3 \mu\text{W}$ with the selected design conditions.

5.3 DYNAMIC PERFORMANCES. — Dynamic simulations of the AND gate are made in a similar way as for the OR gate (Fig. 8.1) and the propagation time versus reduced bias v_a is presented in figure 8.2. Again the minimum t_{pd} near threshold is near the intrinsic time constant of the junctions. Figure 8.2 shows that $t_{pd} \approx 10 \text{ ps}$ at a bias equal to 80% of the junction critical currents. This is twice slower than the OR gate and is due to the input part of the AND gate constituted by junctions J_1 and J_2 which are unbiased. Moreover the gate is strongly loaded by

Fig. 7. — Static margins of AND gate with fan-in/fan-out = 2/2. (a)-(c) represent equivalent circuits to calculate switching conditions of junctions J_3 to J_5 . (d) shows the static margins where lines 1 to 4 correspond to the threshold conditions of junctions J_1 (or J_2), J_3 , J_4 and J_5 . The gate parameters are, $J_{c1} = J_{c2} = 50 \mu A$, $J_{c3} = 110 \mu A$, $J_{c4} = 200 \mu A$, $J_{c5} = 75 \mu A$, $R_a = 60 \Omega$, $R_1 = 2.75 \Omega$, $R_2 = 1 \Omega$, $R = R' = 1 \Omega$.

R and R' when gate switching starts. A faster AND gate could be obtained using an inverted structure for the gate, i.e. using input buffer OR gates in front of the junctions which realize the logic AND function. This would be at a cost of twice the power dissipation for a 2-input AND gate.

6. Conclusion.

We have described an advanced design of direct coupled Josephson logic to exploit fully the speed potentialities of small $R_N \times C$ junctions (1-2 pN). Switching times of loaded gates with fan-in/fan-out ≥ 2 in standard circuit bias conditions ($v_a = 0.8$ giving $\approx 20\%$ margins) are only 5 ps for the OR gate and 10 ps for the AND gate. The ADCL design brings a breakthrough in the speed performances of direct current logic circuits as it reduces strongly

Fig. 8. — (8.1) Dynamic simulation of an AND gate with the parameters of the figure 7. (8.2) Propagation delay t_{pd} of AND gate as a function of bias V_a . The gate parameters correspond to figure 7 except $J_{c3} = 90 \mu A$, $J_{c4} = 140 \mu A$, $J_{c5} = 50 \mu A$, $R_a = 90 \Omega$. The results are presented in different loading conditions : (a) $f_i/f_0 = 2/1$, (b) $f_i/f_0 = 2/2$.

turn-on delays which plagued previous designs and prevented to take advantage of the intrinsic performances of small area junctions. This is obtained at no sacrifice in power dissipation since the OR and AND gates rate both at $\approx 3 \mu W$ with the above speed performances. Preliminary results have shown that the ADCL design may be extended successfully to complex gates and circuits with large speed improvements of at least a factor of three in circuit conditions [13].

Appendix : noise in DCL gates.

The consequences of thermal noise on junction erroneous switching are estimated using the same approach as in [14]. The transition probability of a junction induced by thermal noise is estimated with the following expression

$$p = \left(\sqrt{\left(\frac{3.75 I_0}{2 \pi \Phi_0 C} \right)} \times \exp \left(- \frac{dU}{kT} \right) \right)$$

with

$$dU = - \frac{3.75 \Phi_0 I_0}{2 \pi} \times 2((\sqrt{1-x^2}) - x \arccos x)$$

and

$$C = \tau_c / R_N, \quad R_N = \pi V_g / 4 I_0$$

where x is the relative polarisation of the junction and I_0 is its critical current, C is the junction capacitance and F_0 is the flux quantum. The transition probability depends strongly on I_0 and slightly on C . Then it is not modified by the use of picosecond junctions, but the critical current of junctions must not be too small i.e. smaller than 50 μA . The transition probability is calculated in table II for different junction critical currents and polarizations. In a processor of 10^6 gates, a 200 ps

cycle time, and an error rate of one per year due to thermal noise, the transition probability must be smaller than 10^{-25} . This is only verified in the present design if the junction relative bias is smaller than 0.9 with junctions of 50 μA critical current. The result also emphasizes that numbers related to circuit speed performances are mostly meaningful at bias voltages far enough from threshold.

Table II. — Transition probability induced by thermal noise of OR gate with parameters of figure 3a.

$I_0 (\mu\text{A}) \backslash x$	0.88	0.9	0.92
—	—	—	—
50	10^{-25}	10^{-16}	10^{-8}
75		10^{-30}	10^{-18}

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