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High voltage RESURF LDMOS for smart power integrated circuits

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Résumé. — Une étude détaillée du comportement électrique des transistors LDMOS de type RESURF est donnée. Le claquage par avalanche est évalué à la fois par des règles analytiques simples, pour une approche de premier ordre, et par une analyse numérique bidimensionnelle pour une compréhension plus fine. Un logiciel de simulation numérique travaillant en 2 dimensions, BIDIM2, est utilisé pour évaluer l'influence de certains paramètres critiques (épaisseur et concentration d'épitaxie, distance canal-drain, profondeur de jonction de canal) sur la tension de claquage et la résistance à l'état passant. L'étude à l'état passant du transistor permet de déterminer sa résistance passante ainsi que la répartition du courant pour prévoir les améliorations qui peuvent être apportées par des techniques telles que le surdopage localisé en surface ou l'utilisation de couches semi-résistives (telle que le SIPOS). On extrait ainsi un certain nombre de règles de conception pour les transistors LDMOS RESURF qui confirment que ce composant est aisément utilisable dans les circuits intégrés haute tension. Pour valider ces règles des diodes RESURF de moyenne tension (350-550 V) sont réalisées et testées.

Abstract. — An in-depth comprehension of the electrical behaviour of a RESURF LDMOS is given. Avalanche breakdowns are evaluated leading to simple design rules based on analytical formulations for a first order analysis, and on bidimensional numerical simulations for a second order analysis. A 2D numerical simulator is used to study the influence of some critical parameters on the breakdown voltage and the on behavior. Such parameters include the epitaxy doping and thickness, the channel-drain distance, the channel junction depth. On state investigation is conducted to evaluate the on-resistance and the current flow of the device and to study the improvement which can be expected from technics such as surface doping or SIPOS deposition. With such design rules the RESURF LDMOS is a good applicant for power switches in smart power IC. To illustrate and validate these design rules medium voltage diodes (350-550 volts) are processed and tested.

1. Introduction.

Among the numerous techniques available to improve the voltage handling capability of power devices, one is very attractive due to its simplicity and its high efficiency. With the RESURF [1] technic (for Reduced SURface Field) one is able to reach the ideal bulk breakdown without changing anything to the process but only a substrate substitution: for example switching from a N−/N+ epitaxy to a N−/P− one (for a P/N− diode).

This principle can be applied to several power devices and for example to the double diffused lateral MOS transistor: LDMOS (Fig. 1).

To illustrate the appliance of RESURF LDMOS
These new kinds of chips are called Smart Power (single output) or High Voltage (multiple outputs) Integrated Circuits and will concern every sector of electronics (automotive, telecommunications, computers, ...). Some solutions, even products, are currently available, mainly single switch circuits where a vertical power transistor (often a VDMOS) is used. The isolation between this device and the low voltage circuit is done either by diffused walls, dielectric or self-shielding [13].

Among these solutions RESURF transistor appears to be a very interesting applicant for multiple switches integrated circuits.

However to properly design this kind of power device one must use sophisticated tools to take into account its highly bidimensional electrical behaviour.

The first part of this paper deals with the off-state electrical behaviour of RESURF LDMOS. The critical parameters are determined and a dedicated software tool is used to predict the breakdown voltage and location evolution versus these parameters. Some analytical rules are also given for borderline cases and are compared to the numerical results.

The second part studies the on-state electrical behaviour of this transistor. The on-resistance and some methods to improve it will be given. These methods includes using a surface implantation between the channel and the drain, as well as depositing a semi-resistive layer between the grid and the drain metallization. The third section reports some experimental results obtained on RESURF diodes in order to validate the theoretical approaches.

2. Off state.

An in-depth understanding of breakdown phenomena in RESURF LDMOS is thus possible. This understanding enables to simplify the designer's task by setting up some analytical approaches in order to roughly evaluate the values for these critical parameters. These first order formulations concern mainly the avalanche breakdown of the space charge limited junctions drain/epitaxy/substrate (vertical) and drain/epitaxy/channel (horizontal), and of the cylindrical junction well/epitaxy where the well junction depth is a critical datum for the RESURF principle.

2.1 RESURF PRINCIPLE. — Considering the figure 1 for the conventional LDMOS case (epi N - /N + ), when the drain voltage is increased, the source, P well and gate being grounded, the high voltage is essentially supported by the reverse biased junction P (channel or well)/N - (epitaxy). Thus, typically, the breakdown voltage of this device will be that of this cylindrical junction (if surface breakdown is avoided with correct oxide thicknesses and gate field plate).
But with a N−/P− epitaxy the high voltage will be also distributed on this plane reverse biased junction (the substrate must be grounded) which can attain much higher voltage than a cylindrical one. If well-designed the P (channel or well)/N− (epitaxy) junction will be completely depleted before seeing a critical voltage on its sides. The RESURF technic can be seen as a junction termination working vertically as well as for the cylindrical junction as for the surface.

2.2 ANALYTICAL BORDERLINE CASES.

— Epitaxy and substrate concentrations. — The ideal breakdown voltage of a planar junction is given by [4, 5]:

\[ V_{bp} = \frac{\varepsilon \cdot E_c^2}{2 \cdot q \cdot C_{eff}} \]  

(1)

where \( \varepsilon \) is the silicon permittivity, \( q \) the electron charge and \( E_c \) the experimental critical electric field:

\[ E_c = 9.5 \times 10^2 \cdot C_{eff}^{1/2} \]  

(2)

\( C_{eff} \) being the effective doping of the epitaxy/substrate junction [5]:

\[ C_{eff} = \frac{C_{epi} \cdot C_{sub}}{C_{epi} + C_{sub}} \]

\( C_{epi} \) and \( C_{sub} \) being respectively the epitaxy and substrate doping. Figure 4 gives the evolution of \( V_{bp} \) versus \( C_{eff} \).

---

Epitaxy thickness regarding drain/epi/substrate reach-through. — The presence of a N+(drain)/N− (epitaxy)/P− (substrate) diode can limit the breakdown voltage of the planar junction due to a possible reach-through of the epitaxial depletion layer up to the drain.

The breakdown voltage of such a diode is given by integrating a 1 dimensional Poisson equation:

\[ V_{brt} = \frac{\varepsilon \cdot E_c^2}{2 \cdot q \cdot C_{sub}} + E_c \cdot (W_{epi} - X_{jd}) - \frac{q \cdot C_{epi}}{2 \cdot \varepsilon} \cdot (W_{epi} - X_{jd})^2 \]  

(3)

where \( W_{epi} \) is the epitaxy thickness and \( X_{jd} \) the drain junction depth. \( E_c \) is still given by relation 2.

One must be careful that relation (3) is only valid when reach-through really occurs, so that one must switch to relation 1 for non reach-through condition. Figure 5 depicts the evolution of \( V_{brt} \) versus \( W_{epi} - X_{jd} \) for a 10^15/10^15 cm\(^{-3} \) doped wafer.

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P+ well junction depth. — We know that for the RESURF effect being efficient the P(channel or well)/N− (epitaxy) junction must be depleted before attaining its own cylindrical breakdown voltage. The latter is more likely to occur near the P+(well)/N− (epitaxy) junction due to its higher doping (this is confirmed by the breakdown of the conventional LDMOS in figure 2 but does not completely discard the voltage necessary to deplete the area between the bottom of the P+ well and the epitaxial junction is obtained when the two depletion layers join. Integrating Poisson equation and using the abrupt approximation for these two diodes [10], one obtain:

\[ V_{dep} = \frac{(W_{epi} - X_{jp})^2}{2 \cdot \varepsilon \cdot \left[ \frac{C_{sub}}{C_{epi} + C_{sub}} + 2 \sqrt{\frac{C_{sub}}{C_{epi} + C_{sub}}} \right]} \]  

(4)

For our 300 volts device we can choose for instance a 10^15/10^15 cm\(^{-3} \) doped wafer which gives a 410 volts planar breakdown voltage.
996

\( X_{jp} \) is the junction depth of the P + well. Obviously this value is a lower limit and the applied voltage should be greater.

The breakdown voltage of a cylindrical junction is quite well represented by the following law [6]:

\[
V_{bc} = V_{bp} \cdot \sqrt{0.871 + 0.125 \cdot \ln \left( \frac{X_{jp}}{W_p} \right)}
\]  (5)

\( V_{bp} \) being given by relation (1) and \( W_p \) being the depletion width of the equivalent planar junction at breakdown [6]:

\[
W_p = 2.67 \times 10^{10} \cdot C_{eff}^{7/8}
\]

Figure 6 gives the evolution of \( V_{dep} \) and \( V_{bc} \) versus \( X_{jp} \) for a given \( W_{epi} \) of 16 microns and the same wafer as previously. This value is chosen sufficiently high to demonstrate the depletion effect (otherwise, with thinner values, the depletion phenomenon takes place for very low voltages).

Fig. 6. — Depletion voltage of the N – area under the P well, and breakdown voltage of the cylindrical junction P well/N – epitaxy versus P well junction depth. (\( W_{epi} = 16 \) \( \mu \)m, \( C_{epi} = C_{sub} = 10^{15} \) cm\(^{-3}\).)

The intersection of the curves \( V_{dep}(X_{jp}) \) and \( V_{bc}(X_{jp}) \) gives the lower value of the P junction depth which can be considered either as the P + well one or the channel one.

— Drain-channel distance. — It is very difficult to obtain analytically, and moreover in one dimension, a minimal value of the drain-channel distance, \( L_i \).

Just to give an idea one must take care not to degrade the voltage handling capability of the device by a lateral reach-through P – (channel)/N – (epitaxy)/N + (drain).

This condition is always verified when the following relation stands:

\[
L_i \geq W_{N-} = \sqrt{\frac{2 \varepsilon \cdot V}{q \cdot C_{epi}}}
\]

\( V \) being the voltage applied to the P – (channel)/N – (epitaxy) diode.

2.3 BIDIMENSIONAL NUMERICAL ANALYSIS. — If the preceding approximations are useful to give the magnitude orders of some parameters, one still need a more precise analysis to extract reliable design rules.

We use a special purpose software, BIDIM2 [7, 11], to study the breakdown voltage and location of power devices. This software is dedicated to power and high voltage devices and is able to solve in 2 dimensions on a finite differences grid the Poisson equation and the quasi-Fermi levels equations. Off-state analysis are usually performed with the Poisson equation alone enabling to study very high biases. Results available concern the potential, the electric field (global and X and Y components), the Fermi levels, the breakdown voltage and location. On-state analysis is performed with the 3 coupled equations giving in addition of the aforementioned data, the carriers densities, the current density, the external currents and the on-resistance.

The breakdown criterion is based on the calculation of the ionization integral in several parts of the structure with Van Overstraeten coefficients [8].

The parameters of the structure being kept constant are the following:

<table>
<thead>
<tr>
<th>JUNCTIONS and SUBSTRATE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area (type)</strong></td>
</tr>
<tr>
<td>epitaxy (N –)</td>
</tr>
<tr>
<td>substrate (P –)</td>
</tr>
<tr>
<td>drain (N +)</td>
</tr>
<tr>
<td>source (N +)</td>
</tr>
<tr>
<td>channel (P)</td>
</tr>
<tr>
<td>well (P +)</td>
</tr>
</tbody>
</table>

**OTHER CHARACTERISTICS \( \text{microns} \)**

| gate oxide thickness | 0.1 |
| channel-drain area oxide thickness | 0.7 |
| channel-drain distance | variable |

— Epitaxy thickness and concentration. — The figure 7 shows the result obtained by BIDIM2 on the breakdown voltage of a RESURF LDMOS when the epitaxy thickness increases. The epi concentrations are \( 10^{15} \) and \( 2 \times 10^{15} \) cm\(^{-3}\) and the drain-channel distance 27.5 \( \mu \)m.

We observe three breakdown areas:

1) for thin epi layer (< 10 \( \mu \)m) breakdown happens at the N + (drain)/N – (epitaxy)/P – (substrate)
Fig. 7. — Breakdown voltage of a RESURF LDMOS versus epi-thickness for 2 epi-concentrations. When $C_{epi} = 10^{15}$ cm$^{-3}$ the breakdown occurs either in the plane junction (A), at the surface (B) or at the cylindrical junction P well/epitaxy N – (C).

1) in the plane junction : the drift action of the epitaxy is negligible and we are in reach-through mode ;
2) between 10 and 18 $\mu$m it occurs at the plane N – (epitaxy)/P – (substrate) junction : the RESURF effect is optimal ;
3) above 18 $\mu$m breakdown takes place at the cylindrical P (channel or well)/N – (epitaxy) : we are back to the conventional LDMOS.

For higher epi-doping ($2 \times 10^{15}$ cm$^{-3}$) the RESURF effect occurs for a very narrow range of thicknesses (less than 10 $\mu$m) and it will be more critical to process regarding the technological tolerances on epi-doping and thicknesses.

— Drain-channel distance. — The calculated breakdown voltages versus the drain-channel distance $L_i$ is plotted in figure 8. $W_{epi}$ is equal to 11 $\mu$m and $C_{epi}$ to $10^{15}$ cm$^{-3}$.

For distances greater than 27.5 $\mu$m the breakdown voltage is constant and equal to $V_{bp}$ as given by the relation (1). For $L_i$ less than 27.5 $\mu$m the proximity of the channel (grounded) and the drain induces a breakdown between them : the breakdown voltage decreases sharply.

— P + well junction depth. — It is difficult to illustrate the influence of the P well junction depth on breakdown voltage in a RESURF structure with 2D numerical analysis. If for very low values of $X_{jp}$ we effectively observe a cylindrical breakdown at the P + (well)/N – (epitaxy) junction, we have to give a quite high value for the epi-thickness and so we always notice a surface breakdown when we increase $X_{jp}$. Thus the soft increase of breakdown voltage from the cylindrical one to the planar one is delicate to show with such a tool.

However, as it is shown on figure 6, the P(well)/N – (epitaxy) area is depleted for low voltage and thus a cylindrical breakdown is not likely to occur.

The external voltage which will be seen from outside components will depend on this junction depth.

3. On state.

The on state analysis presented is based on numerical results only. BIDIM2 is used to solve the three fundamental equations of semiconductors based on potential and quasi-fermi levels. The current is calculated in the channel and near the drain contact, and the on-resistance, $R_{on}$, is calculated by Ohm's law.

The on-resistance versus the critical parameters previously stated (i.e. the drain-channel distance and the epi-thickness) is determinated.

A major drawback of lateral devices is their high on-resistance. To improve the on-resistance of such devices two technics have been proposed : using a semiresistive (such as SIPOS) layer between the channel and drain metallizations [2], or implanting a shallow lightly doped layer at the surface of the wafer [3].

are the awaited improvements.

3.1 $R_{on}$ VERSUS EPITAXY THICKNESS AND DRAIN-CHANNEL DISTANCE. — Figure 9 gives the value of $R_{on}$ versus $W_{epi}$ and $L_i$. Obviously $R_{on}$ increases with $L_i$ and decreases with $W_{epi}$. This latter effect is due to the constriction of the current lines when the epitaxy goes thinner. The on-resistance is always calculated for a 1 centimeter channel width.

The asymptotic value obtained for thick epitaxies correspond to the on-resistance of a conventional LDMOS where no current lines constriction occurs.
3.2 IMPROVEMENT OF $R_{on}$ WITH SURFACE DOPING. — In figure 10 are plotted the results obtained by BIDIM2 for $R_{on}$ versus the surface concentration of an implanted layer of fixed junction depth (3 μm). On this figure are also reported the corresponding simulated breakdown voltages. $R_{on}$ decreases from 17.5 ohms, without surface implantation, to 12.7 ohms, with a $10^{16}$ cm$^{-3}$ doped one. However, for this concentration the degradation of the breakdown voltage is significant: from 410 volts to 240 volts.

For implantation doping ranging from $2 \times 10^{15}$ to $6 \times 10^{15}$ cm$^{-3}$ the breakdown voltage is near the bulk value (400 volts) and the on-resistance can be as low as 13 ohms.

Thus, from surface doping technic, one can expect an improvement of 25% for the on-resistance of our device without degrading significantly the voltage handling capability.

Moreover surface doping technic is very simple to process and can be applied to very high voltage devices, as well lateral as vertical ones [9].

3.3 IMPROVEMENT OF $R_{on}$ WITH A SEMIRESISTIVE LAYER. — If you deposit a semiresistive layer on the top of the oxide between the channel and drain metallization you linearize the potential between these contacts, leading to a possible accumulated layer in the drift area (depending on the oxide thickness).

However, this technic is more effective for lowly doped substrate (where it is easier to accumulate electrons) but in this case the thin oxide needed on the drift area can be a major drawback for the voltage handling capability of the device (even for a RESURF one).

For instance, on a $3 \times 10^{14}$ cm$^{-3}$ doped N−epitaxy a semiresistive layer improves the on-resistance from 60 to 40 ohms (33%). The gain is only 20% on a $10^{15}$ doped epitaxy (decreasing $R_{on}$ from 17.5 to 14 ohms), and 15% for $2 \times 10^{15}$ (from 6.5 to 5.5 ohms).

Moreover SIPOS deposit is quite difficult to master technologically.

3.4 FACTOR OF MERIT. — The factor of merit is the inverse of the product of the on-resistance $R_{on}$ times the active area. For a LDMOS as depicted in figure 1 and with parallel strips the active area is defined as the product of the total cell length (including drain and P well) times the channel width.

This factor of merit can be understood as the conductance per active area unit. Figure 11 reports the evolution of this factor versus the epi-thickness and for the three drain-channel distances previously studied.

$1/R_{on} \cdot S$ increases from 10 ohm$^{-1}$ . cm$^{-2}$ without surface implantation) to 15 (with a $6 \times 10^{15}$ cm$^{-3}$ one).
4. Trade-off $R_{on} - V_{br}$

The trade-off between on-resistance and the breakdown voltage is given in figure 12 as the ratio $BV$ over $R_{on}$ versus $W_{epi}$. The epitaxial concentration is $10^{15} \text{ cm}^{-3}$ and the drain-channel distance 27.5 $\mu$m. This curve is similar to figure 7 ($BV$ versus $W_{epi}$) indicating that the evolution of the breakdown voltage dominate when $W_{epi}$ changes.

![Fig. 12. Trade-off breakdown voltage — on-resistance versus epi-thickness. ($L_i = 27.5 \mu m, C_{epi} = 10^{15} \text{ cm}^{-3}$).](image)

5. Technology.

To illustrate and check these design rules for Off state, we have processed a preliminary set of RESURF diodes [12]. Their characteristics as well as the measured and predicted by BIDIM2 breakdown voltages are reported in the following table.

<table>
<thead>
<tr>
<th>Wafer (N-/P-)</th>
<th>$L_i$ ($\mu$m)</th>
<th>$W_{on}$ ($\mu$m)</th>
<th>$V_{BR}$ (V) theoretical</th>
<th>$V_{BR}$ (V) measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 $\times 10^{15}, 1.1 \times 10^{15}$</td>
<td>27.5</td>
<td>10.0</td>
<td>340</td>
<td>370</td>
</tr>
<tr>
<td>—</td>
<td>37.5</td>
<td>—</td>
<td>400</td>
<td>370</td>
</tr>
<tr>
<td>—</td>
<td>47.5</td>
<td>—</td>
<td>400</td>
<td>370</td>
</tr>
<tr>
<td>8 $\times 10^{14}, 7 \times 10^{14}$</td>
<td>27.5</td>
<td>16.5</td>
<td>330</td>
<td>360</td>
</tr>
<tr>
<td>—</td>
<td>37.5</td>
<td>—</td>
<td>460</td>
<td>450</td>
</tr>
<tr>
<td>—</td>
<td>47.5</td>
<td>—</td>
<td>530</td>
<td>560</td>
</tr>
<tr>
<td>2 $\times 10^{15}, 8 \times 10^{14}$</td>
<td>27.5</td>
<td>29.0</td>
<td>230</td>
<td>160</td>
</tr>
<tr>
<td>—</td>
<td>37.5</td>
<td>—</td>
<td>130</td>
<td>160</td>
</tr>
<tr>
<td>—</td>
<td>47.5</td>
<td>—</td>
<td>130</td>
<td>160</td>
</tr>
</tbody>
</table>

6. Conclusion.

An in-depth comprehension of the electrical behaviour of a RESURF LDMOS for HVIC's is given. Avalanche breakdowns are evaluated leading to simple design rules based on analytical formulations and bidimensional numerical simulations.

The isolation of the device clearly depends on the P well junction depth.

On state investigation is conducted to evaluate the on-resistance and the current flow of the device and to study the improvement which can be expected from technics such as surface doping or semiresistive layer deposition. Surface doping can improve the on-resistance by 30% without degrading the breakdown voltage if carefully used. A semiresistive layer deposited between the channel and drain metallizations also improves the on-resistance but is difficult to process and is not suitable for high voltages where a thick oxide layer between channel and drain is mandatory.

We have processed a first set of RESURF diodes to check our design rules and have found a very good agreement between the calculated and the measured breakdown voltages values. RESURF LDMOS are currently under electrical test. More to come.

Although our study concerns a 300 volts device it should be noted that the RESURF technic can be applied to higher voltage handling capability devices, in fact as high as the on-resistance is acceptable for 1200 volts RESURF LDMOS for home applications.

References


