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Design and realization of a GaAs FET integrated with a heterojunction photodiode

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Résumé. — L'association d'une photodiode à hétérojonction et d'un circuit amplificateur à effet de champ produit une augmentation de la sensibilité du détecteur. Le principe de fonctionnement et les critères de conception du circuit intégré TEC-Détecteur sont décrits. La fabrication du TEC à hétérojonction est organisée à partir de la technique de l'épitaxie en phase liquide. La structure comprend deux couches épitaxiées, principales, le canal formé par une couche de GaAs de type N et la région de grille en GaAlAs de type P. Nous détaillons la technologie de fabrication du composant ainsi que les caractéristiques courant-tension. Nous avons obtenu des valeurs de la transconductance égales ou supérieures à 10 mA/V. Le transistor a montré une tension de seuil de – 4,6 V. Les résultats précédents sont appliqués à deux types de structure, d'une part des composants TEC sans détecteur et d'autre part des circuits intégrant l'amplificateur et la photodiode. Les divers dispositifs sont caractérisés et analysés.

Abstract. — Integrated receivers associating an amplifier with a photodiode are studied. The field effect transistor used for the amplifier has been designed and characterized. The FET transistor has been fabricated on a GaAs semi-insulating substrate using Liquid Phase Epitaxy. The structure consists of two epitaxial layers, i.e. one N-GaAs layer for the channel and a P-GaAlAs layer for the gate. The design, technological process and current-voltage characteristics are described. Transconductance values over 10 mA/V have been achieved and the transistor have shown a threshold voltage of – 4.6 V. Integrated receivers whose field effect transistor is associated with a photodiode, enhance the detector sensitivity. The results measured on the field effect transistor will be applied to the amplifier integrating the photodiode.

1. Introduction.

Over the last years, much work has been devoted to the integration of a photodetector and a FET on the same substrate [1]. Design of such a device shows the possibility of integrating electronic networks and optical elements (receivers here). Monolithic integration reduces parasitic capacitances and avoids interconnection problems, resulting in increased performances and reliability. The size of the PIN-FET combination is smaller than that of discrete device circuits. Several results have been obtained for the integration of the photodetector and amplifier. It is important to design a field effect transistor with a high transconductance value g_m and minimum capacitance C_T. We have studied the variation of the previous factors ratio : g_m/C_T^2 as a figure of merit for the PIN/FET device.

Wada *et al.* have measured a transconductance of 34 mS/mm and an input capacitance of 1.1 pF [2] on a MESFET circuit. For a gate width of 50 μm, the figure of merit g_m/C_T^2 equals 1.4×10^{21} V/A · rd^2/s^2. Kasahara *et al.* [3] have shown a transconductance value of 12.5 mS/mm and a capacitance reaching 1.7 pF for a PIN-MISFET photoreceiver whose ratio g_m/C_T^2 becomes 1.7×10^{21}V/A · rd^2/s^2 having a 400 μm gate width.

Leheney *et al.* [4] have integrated a junction field effect transistor with a PIN diode. The transconductance was as high as 50 mS/mm and the capacitance value was below 1.8 pF. The results have shown a figure of merit reaching 1.8×10^{21} V/A · rd^2/s^2 for a 120 μm gate width.

It is the object of this paper to present the design criteria in respect of a monolithic receiver adapted to optical communications systems. During this first work, we have intended to design and characterize the FET amplifier. We describe the fabrication of

GaAlAs-GaAs heterojunction JFET compatible with a photodiode. A heterojunction has been chosen in order to slightly improve the input impedance. The feasibility study of the circuit's active part corresponds to the drawings of the source, drain and gate electrodes. In the first part of this paper we describe the design and physical behaviour of the integrated device. The second part is devoted to the technological process. Finally in the third part we show the electrical characteristics, we detail the transconductance values, the resistance at the electrodes and the conduction mechanism in the channel.

2. Design criteria.

The electrical circuits describing the behaviour of the JFET associated with the P-N heterojunction photodetector is shown in figure 1. The device produces an output current higher than the intensity generated by the photodiode. The P-N diode responsivity is multiplied by a factor equal to the product of the transconductance of the amplifier by the resistance R_L. The current gain of the circuit in figure 1 is expressed as :

$$i_d = g_m \cdot R_L \cdot i_p$$

where :

i_d : drain current,
g_m : transconductance of the field effect transistor.
R_L : load resistance of the P-N photodiode.

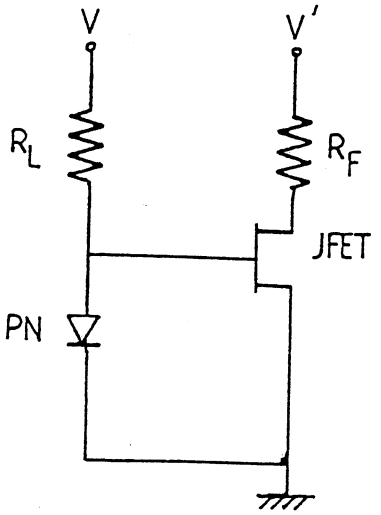

Fig. 1. — Electric circuit diagram of integrated FET and photodiode.

The feasibility study of the circuit parts corresponds to the design in the following way. The gate width is imposed by the requirements for a sufficient level of drain current and transconductance. Some transistors have a gate width Z of 350 μm, whereas other integrated receivers have a 400 μm Z value which is the sum of the two parts of the source electrode length. Thickness of the n-GaAs layer is of the order of 0.4 μm. The doping N_D is increased from 2×10^{16} cm^{-3} to 8×10^{16} cm^{-3}. The photodiode dimensions are 160×110 μm·μm within the metallic contact. The gate width is varied from 8 μm to 4 μm. Over etching of the GaAlAs layer produces lower gate widths. The GaAlAs growth greatly simplifies the technological process. The aluminium content has been fixed at 0.4 in order to permit a high doping level [5].

3. Device technological process.

Four epitaxial layers are grown on a GaAs semi-insulating substrate using Liquid Phase Epitaxy (Fig. 2) :

— a GaAs buffer undoped layer,
— an active layer, N-type GaAs and Sn doped,
— a P-GaAlAs layer for the gate electrode, Ge doped and 0.5 μm thick,
— finally, a P$^+$-GaAs, Ge doped, 1 μm thick, is produced for the contact.

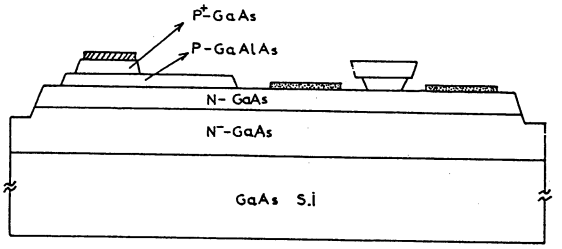

Fig. 2. — Cross section view of the integrated receiver fabricated by a LPE growth process.

The growth of the first undoped layer over the semi-insulating substrate prevents diffusion of chromium from the substrate and defines the channel limit from source to drain. Substrate preparation was carefully controlled. Cleaning is critical to achieve a successful growth [6].

The use of an additional well in the boat gives low residual doping concentration in the buffer layer : *in situ* etching is carried out in the first well and the sample is pushed under the following melt in order to grow the buffer layer. The P$^+$ GaAs contact layer is realized by photolithography. The P-GaAlAs etching is achieved with HF at 50 °C for 45 s. Definition of the ohmic contacts either over the N or P types, is through the standard lift-off technique avoiding further degradation of the surface [7].

In some samples an airbridge separates the transistor from the gate bond. The airbridge technique consists of etching the P$^+$-GaAlAs layer, using the gate metalization as a mask (Fig. 3).

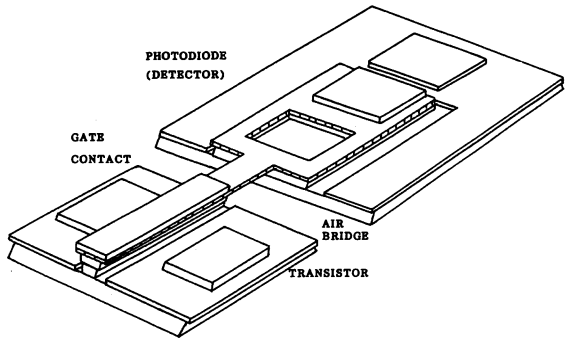

Fig. 3. — Separation of the transistor from the gate bond by airbridge.

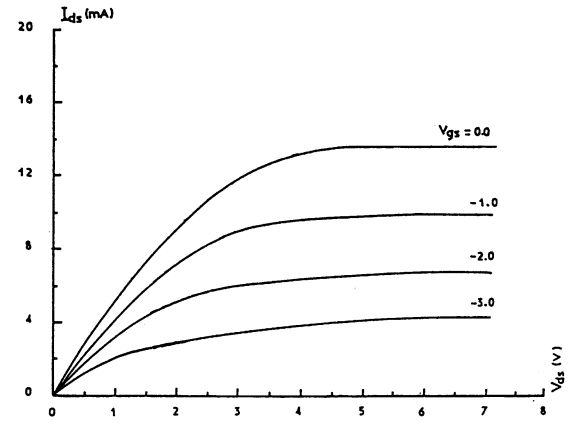

Fig. 5. — Output drain current *versus* drain voltage of the device F12 without the photodiode.

4. Electrical characterization.

CURRENT VOLTAGE-CHARACTERISTICS. — Our experimental study corresponds to the current-voltage curves of the gate-source heterojunction and the set of output characteristics. From these measurements we deduce transconductance g_m, the threshold voltage V_T and the access resistances [8].

Two kinds of devices are made, on the one hand the 3 μm gate long heterojunction field effect transistor without the detector and on the other the integrated circuit associating the detector with the transistor. Figure 4 shows the set of output characteristics for several values of gate voltage and sample F10 without the photodiode. Saturation currents of 70 mA are observed. From the curves shown in figure 4, we note a transconductance value of 12 mA/V for $V_G = -1$ V and $V_D = 5$ V. Other output characteristics are given in figure 5 for sample F12 and a 2×10^{16} cm^{-3} doping density in the N-GaAs channel layer. In this case the saturation current and transconductance results are lower than the previous values, typically 14 mA and 3.5 mA/V.

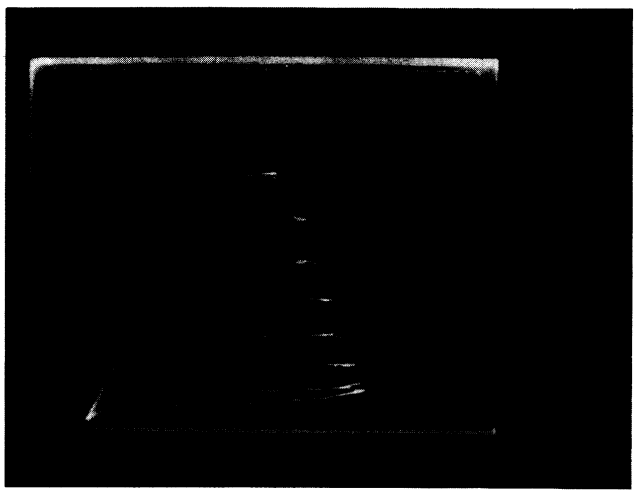

Fig. 4. — Output current voltage characteristics of the device F10 without the photodiode.

Devices integrating the field effect transistor and the detector are also characterized. The drain current-voltage curves measured on the sample PI12 are plotted in figure 6. We observe a small slope in the saturation region of the $I_D(V_D)$ characteristics giving a drain transconductance.

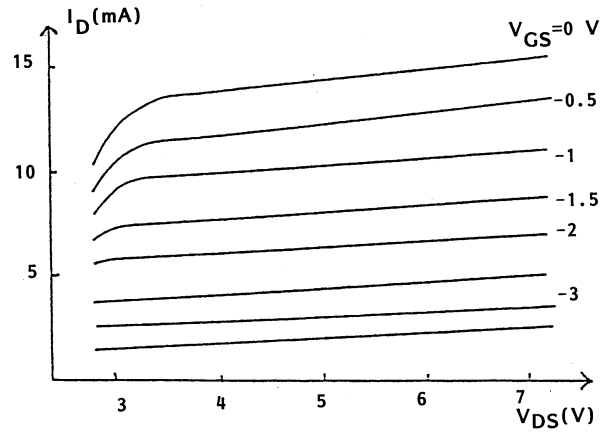

Fig. 6. — Output current voltage characteristics of the device PI12 integrating the FET and the photodiode.

As mentioned in the third section, an airbridge is formed and the transistor is separated from the gate bond. The airbridge separation overcomes the parasitic capacitance effect produced by the P^+ material between the gate electrode and the gate contact. This technique reduces the leakage current of the gate electrode. The link ensures that the layer capacitance does not affect device performance. We have measured the variation of the gate capacitance of the transistor in terms of voltage.

The results are plotted in figure 7. A small capacitance value can be observed for example the gate-source capacitance becomes 0.6 pF with a reverse voltage reaching − 6 V. The photodiode presents a capacitance of 2 pF resulting in a factor of merit g_m/C_T^2 reaching 1.5×10^{21} V/A (rd/s)^2.

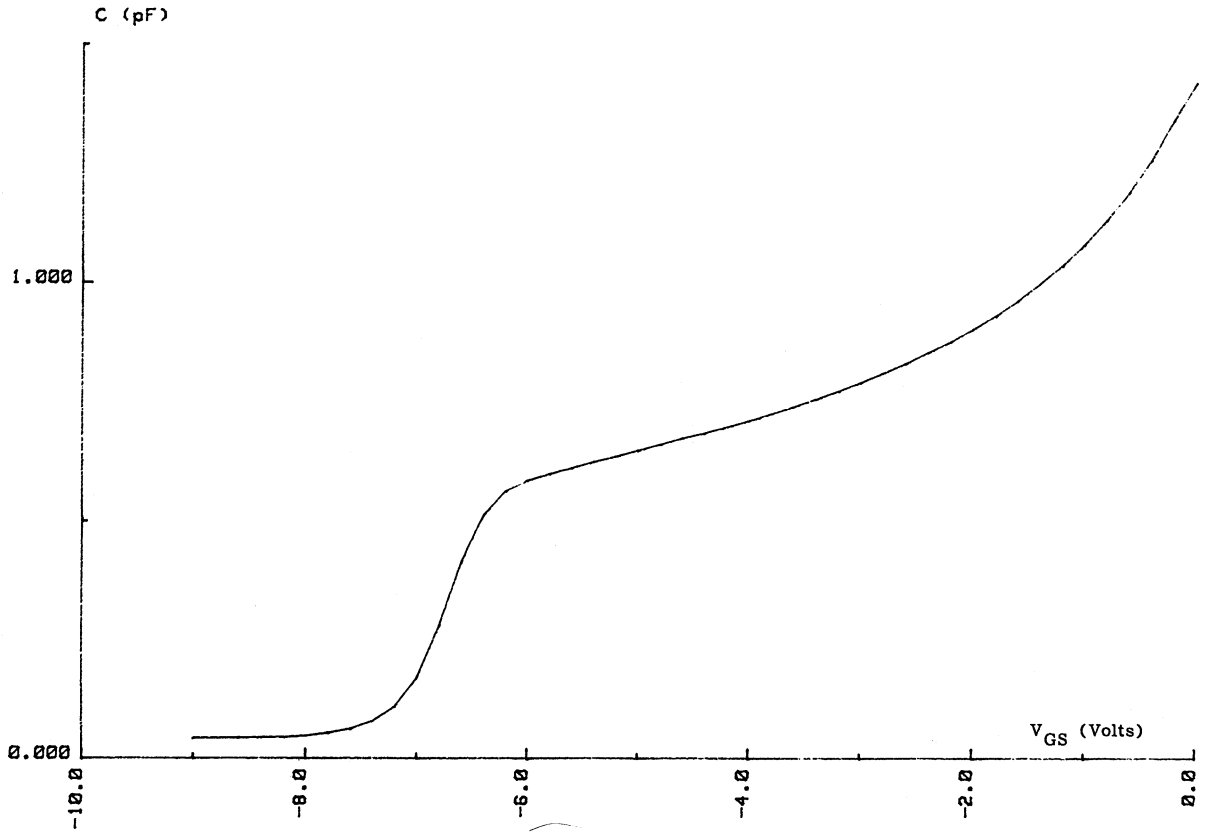

Fig. 7. — Capacitance-Voltage characteristics between the gate and the source of the device F12.

5. Conclusion.

We have designed and characterized a field effect transistor with a heterojunction gate. The technological process of the circuit active part corresponds to the design of the source, drain and gate electrodes. The set of output characteristics I_{DS} (V_{DS}) have been measured. We have deduced a saturation current reaching 70 mA, transconductance values of 12 mA/V and access resistance of about 70 Ω.

We have formed an airbridge by photolithography of the p-GaAlAs layer between the gate contact and the transistor. This technique produces a small value of the gate-source capacitance and additional capacitance does not affect device performance.

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