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Submitted on 1 Jan 1985

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Electronic properties of Al-SiO$_2$-(n or p) Si MIS tunnel diodes (+)

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(Reçu le 16 mai 1984, révisé le 18 septembre 1984, accepté le 1er octobre 1984)

Abstract. — Automatic measurements I-V, C/G(V, $\omega$) are used to study the electrical properties of a great number of aluminum-SiO$_2$-n or p type silicon MIS tunnel diodes with an oxide thickness of 30 Å prepared by two technologies of oxidation, low pressure chemical vapour deposition (LPCVD) and low oxygen pressure (LPO$_2$). A comparison between the I-V and C-V characteristics on n and p substrate is presented as well as a dispersion study of I-V characteristics. The modelling of I-V characteristics has been carried out with a simulation model with two single level interface states. The variation of the main parameters of the modelling is connected with the variation of I-V curves provoked by the dispersion. The interface state densities deduced of the modelling are in agreement with those obtained from the C/G(V, $\omega$) measurements.

Notation.

$C_m$ measured parallel capacitance

$C_p$ (parallel) sum of space charge capacitance and interface state capacitance

$C'_p$ parallel interface state capacitance

$C_{ox}$ oxide capacitance

$C_{sc}$ silicon space charge capacitance

$E_T$ energy of interface states in silicon band-gap

$f$ signal frequency

$G_m$ measured parallel conductance

$G'_p$ parallel interface state conductance

$G_T$ tunnelling conductance

$I$ total current density

$n$ ideality factor

$N_{A}$, $N_D$ acceptor, donor densities in silicon

$N_{so}$ interface state densities of acceptor level located at $E_T$ below the conduction band

$N_{si}$ interface state densities of donor level located at $E_T$ below the conduction band

$N_{ss}$ interface state density

$R_s$ series-resistance

$V_a$ applied d.c. bias

$V_s$ surface potential in silicon

$V_{so}$ surface potential in silicon at zero bias

$\delta$ oxide thickness

$\Phi_B$ barrier height of metal-semiconductor barrier

$\chi$, $\chi_p$ effective electron, hole affinities

$\omega$ angular frequency

1. Introduction.

There is a practical interest in the study of conducting Metal-(Ultra-thin SiO$_2$) Insulating-(Si) Semiconductor structures generally called MIS tunnel diodes because of their uses in microelectronics (VLSI, memory devices, photodiodes arrays) and in photo-cells applications.

There is also a fundamental interest in these studies because these very thin silicon oxide layers (30 Å here) on silicon represent the initial stage of silicon oxidation.

In this paper current-voltage characteristics on n and p type silicon substrate are presented as well as capacitance and conductance characteristics.


Classification

Physics Abstracts

73.40Q

Article published online by EDP Sciences and available at http://dx.doi.org/10.1051/rphysap:0198500200103700
Using a self consistent numerical model of the working of MIS tunnel diodes developed by the authors [1, 2] the dispersion of the current-voltage characteristics of diodes on the same wafer are studied and analysed.

This work based on fully automatic experimental apparatus controlled by microcomputers, allows us to deduce extreme dispersion values of the most important physical parameters at the Si-SiO₂ interface: electronic affinity, oxide thickness, density and energy location of interface states.

Besides comparison between current-voltage and capacitance, conductance-voltage characteristics permits to complete and confirm the previous results.

2. Technological characteristics of the samples.

The devices have been fabricated in EFCIS/Thomson laboratories on <100> oriented n type and p type silicon substrate ($N_D$ or $N_A = 10^{15}$ cm$^{-3}$) by two technological processes described elsewhere [1] to obtain oxide films of 30 Å thickness, measured by ellipsometry:

- Thermal oxidation under low oxygen pressure at 950 °C called LPO₂.
- Low pressure chemical vapour deposition of SiO₂ at 880 °C called LPCVD.

Eight kinds of structures have been studied: LPCVD and LPO₂ oxides on n and p type substrate without and with thermal annealing at 400 °C during 30 min under N₂ atmosphere. A great number of tunnel diodes have been tested (the total number of devices tested is about 50) by using evaporated aluminum electrodes typically of 400 µm x 400 µm on the top surface, wires are attached by ultrasonic bonding on these metallizations. Back contacts are gold or silver. No one measurement has been carried out by pressure and point contact. A special mask is used to permit the realization of the connections, which are made on thick oxide layer parts (Fig. 1).

3. Apparatus of measurement.

In this work automatic data acquisition is always performed. It permits the study of a great number of devices quickly, the storage of data on floppy disks for further treatments and calculations. The following measurement apparatus have been used:

- $I(V)$ measurement unit (automatic HP4140B pA meter-DC voltage source) connected through the IEEE bus-line cable to a HP9826 computer and a HP2673A graphics printer.
- $C(V)$, $G(V)$ measurement unit described elsewhere [3] including principally:
  - an automatic Brookdeal lock-in amplifier with an IEEE interface connected to an Apple II computer, a preamplifier, a Boonton precision decade capacitor and a HP plotter.
  - Automatic semiconductor component test system (HP4061A) consisting of a 4275A multifrequency LCR meter for AC impedance measurements from 10 kHz to 10 MHz, a 4140A pA meter-DC voltage source, a switching subsystem, a 9826A controller and a 7470A plotter. This system permits among others: $I-V$, $C-V$ quasi-static, doping profile measurement and gives bias and/or frequency characteristics of devices.

4. Current voltage characteristics.

Typical current-voltage $I-V_s$ and current density voltage $J-V_s$ characteristics in linear and semilogarithmic plots are shown respectively in figure 2 for the eight kinds of MIS tunnel diodes mentioned in section 2. All measurements are made in the dark.

4.1 Characteristics on n type substrate. — Typical characteristics are represented in linear (range of $10^{-8}$ or $10^{-9}$ A) and semilogarithmic plots in figures 2a and b respectively. The reverse curves present a saturation current, the density is of the order of $10^{-8}$ to $10^{-2}$ mA/cm² (Fig. 2b).

The reverse characteristics show sometimes a « threshold effect » particularly for devices without annealing (curve 2 in Fig. 2a) : the current is first very low and then remains constant for bias lower than $-0.3$ V. The authors have explained this effect in a previous paper by introducing electrostatically acting donor-like interface states in the vicinity or below of the semiconductor midgap [1]. For the forward characteristics it may be observed that an exponential law is not generally obtained, the characteristics in semilog plot are curved towards the voltage axis. Sometimes other shapes may be observed (curve 1 in Fig. 2b), first the characteristics are slightly curved towards the voltage axis and then above $0.3$ V the current increase more rapidly.

It may be noted also that there is a tendency to obtain larger ideality factors for non annealed samples (curves 2 and 2' in Fig. 2b).

The figure 3 shows the dispersion of $J-V_s$ characteristics of devices obtained on the same wafer in the
Fig. 2. — Experimental current-voltage characteristics for LPCVD (solid lines) and LPO₂ (dashed lines) Al-SiO₂-Si diodes on n (a and b) and p type wafer (c and d) annealed (curves 1) or not (curves 2). For n type devices $V_n = V_{m} - V_{sc}$ whereas for p type devices $V_p = V_{sc} - V_{m}$, so that the curves have familiar shapes for both n and p type wafer ($V_{m}$, $V_{sc}$ bias to metal and to semiconductor respectively).

Fig. 3. — Experimentally observed dispersion of $J-V_n$ characteristics for LPCVD (solid lines) and LPO₂ (dashed lines) annealed or not devices on n (a and b) and p (c and d) type wafer ([A]SiO₂ : annealed SiO₂, [NA]SiO₂ : not annealed SiO₂).
case of annealed or not samples. The shapes of the
curves are preserved (saturation effect for reverse bias,
characteristics generally curved toward the voltage
axis for forward bias). There are approximately two
orders of magnitude of dispersion in the reverse charac-
teristics at $-0.7$ V. The experimental dispersion of the
$J(V)$ characteristics depends on the parameters
mentioned in section 4.3.2 and mainly of $\delta, \chi$ (the
tunneling current is proportional to $\exp(-\chi \delta)$)
and the density of the states.

Hysteresis on current-voltage characteristics has
been studied. The 4140B pA-meter mentioned in
section 3 has a voltage source with a double staircase
wave: output voltage changes step by step from start
voltage to stop voltage. Successively, output voltage
is returned to start voltage by same step voltage.
The hold time at beginning and end of voltage ramp is
fixed to 1 s. The annealed LPCVD oxides on n type
substrate do not show hysteresis. Generally for a step
delay time of 10 s and 1 s there is no observable hyste-
resis. Slight displacements between the curve corre-
sponding to an increasing voltage (from start to stop
voltage) and the curve corresponding to a decreasing
voltage are observed for short delay times 0.1 s and
particularly 0.01 s. This is due to time response of the
circuit.

4.2 Characteristics on p type substrate. — Typi-
cal characteristics are represented in linear (range of
$10^{-10}$ A) and semilogarithmic plots in figures 2c and d
respectively. The reverse characteristics have a ten-
dency to present a saturation effect around a voltage
of $-1$ V (Fig. 2d), the density of current is in the range
of $10^{-5}$ mA/cm$^2$.

Some forward characteristics exhibit a kind of
plateau similar to that presented by Shewchun et al. [4]
the current increases approximately exponentially
with voltage for low voltage values then increases less
rapidly, and at last starts to increase rapidly with
voltage above 0.6 V (curve 1 in Fig. 2d). These
authors [4, 5] explained this kind of plateau by consi-
dering the distribution of the external applied voltage
between the oxide layer and the semiconductor,
when the semiconductor surface goes from depletion
to accumulation regime. This plateau effect is attenu-
ated by the action of interface states.

The dispersion curves are shown in figures 3c and d.
The reverse characteristics show a saturation effect,
we have approximately a dispersion of two orders of
magnitude, the forward characteristics show often
the kind of plateau mentioned above (curves 1 in
Figs. 3c and d).

Hysteresis on current-voltage characteristics has
been studied. As in n type device slight displacements
between the curve corresponding to an increasing
voltage and the curve corresponding to a decreasing
voltage are observed for short delay times of 0.1 s or
0.01 s (see section 4.1). No hysteresis is observable for
delay times above 1 s.

4.3 Discussion.

4.3.1 Comparison of MIS tunnel diodes on n and p
type substrate. — As a general rule, there is at least
an order of magnitude between the currents (forward
or reverse) for the same bias range in MIS tunnel diodes
on n and p type wafers (see Fig. 1). There are also some
differences in the shape of the forward curves, the effect
of « plateau » mentioned in section 4.2 appears only
in devices on p type substrate significantly. We can
note also that there is no important difference between
the I-V characteristics for the devices prepared by
LPO$_2$ and LPCVD technologies (see section 4.1).

It is known in the literature [4-7] that majority
carriers dominate the tunnel current in tunnel diodes
on n type substrate and that minority carriers domi-
nate in Al-SiO$_2$-pSi structures. Indeed the Al-SiO$_2$-pSi
structure has naturally a large metal-semiconductor
barrier height $\Phi_b$ as a result of the difference in work
function between Al and p type Si. This can explain
the difference in the magnitude of currents in n and p
type structure. The results on capacitance-voltage
measurements presented further corroborate this anal-
ysis, we see indeed that the silicon surface is inverted
for zero bias for p type structure and near accumu-
lation for n type.

We have quoted above, papers giving a detailed
numerical and experimental analysis of MIS tunnel
diodes on p wafer [4, 5]. In the present work we use a
simulation model [1, 8] developed for n type semi-
conductor, particularly to study the dispersion of I-V
characteristics on n type silicon. The results obtained
using this model are presented in the next sec-
tion (4.3.2).

4.3.2 Modelling study connected to the dispersion of
I-V curves. — In MIS tunnel structures with a very
thin oxide layer the mechanisms for current conduc-
tion are : tunneling between the metal and the major-
ity carrier energy band in the semiconductor, tunnel-
ling between the minority carrier energy band, tunnel-
ling between the metal and surface state levels (surface
states act as recombination generation centres and
provide additional tunnelling paths between the metal
and the semiconductor). From these considerations, a
simulation model for the working of MIS tunnel
structures has been developed by the authors [1, 8].
In this model the usual differential equations describ-
ing the potential distribution and the transport of
free carriers are replaced by a nonlinear algebraic
equation system : the numerical solution becomes
much shorter and a Multics CII-HB67 com-
puter. The actual continuous distribution obtained by
$C/G(V, \omega)$ studies is replaced by discrete levels (here
two), in order to simplify the simulation program and
decrease the calculation time.

a) An acceptor-like level located near conduction
band ($E_c - E_F$, typical value 0.3 eV) having a density
$N_{so}$ and an electrostatic and kinetic action [2], acting
essentially on the forward characteristics and less on the reverse characteristics.

b) A donor-like level $E_{T1}$ located typically at the vicinity of the midgap having a density $N_{s1}$ and an electrostatic action [2], acting on the reverse characteristics and allowing us to simulate the threshold effect observed on the reverse characteristics.

The other important parameters of the modelling which enable to fit the experimental and theoretical curves are: the oxide thickness $\delta$ and the effective electron/hole affinities $\chi_{n}$, $\chi_{p}$.

It is not necessary to introduce a fixed charge in the numerical simulation. Indeed the interface state densities used, allow us to fit the experimental results and are consistent with the values obtained by experimental measurements ($C/G(V, \omega)$).

Typical modelling curves are shown in figures 4a and 4b for LPCVD and LPO$_2$ devices respectively. We note that a satisfactory modelling can be found with only two single levels of interface states by simply varying the values of $\delta$, $\chi_{n}$, $E_{To}$, $E_{T1}$, $N_{So}$, $N_{S1}$. We can remark (Figs. 4a and b) that the observed discrepancies between experimental and theoretical curves are due to the fact that our calculations are based on single level interface states which actually replace the continuous distribution.

We can discuss now the variation of modelling parameters. For example between the curves (1') and (3') of figure 4a we have a variation of $J$ of two orders of magnitude (for $V_{a} = -1$ V). By supposing that there is no dispersion of the typical oxide thickness value ($\delta = 30 \text{ Å}$), we find using our model a $\chi_{n}$ variation of 0.15 eV, a $N_{So}, N_{S1}$ variation of $9 \times 10^{11} \text{ cm}^{-2}$ and $2.4 \times 10^{11} \text{ cm}^{-2}$ respectively.

Between the curves (1') and (3') of figure 4b we find in the conditions mentioned above a variation for $\chi_{n}$ of 0.18 eV, for $N_{So}$ of $1.8 \times 10^{11} \text{ cm}^{-2}$ and no variation of $N_{So}$. In conclusion with the assumption of constant oxide thickness, we can modelize experimental extreme curves of figure 4 with a variation of $\chi_{n}$ lower than 0.2 eV and a variation of interface state density ($N_{So}$ or $N_{S1}$) lower than $9 \times 10^{11} \text{ cm}^{-2}$. It may be noted that the variation of the current obtained by the simulation model are very sensitive particularly to the variations of $\chi$ and also to the variations of the state density of donor type ($N_{s1}$) acting on the forward characteristics (see above). The acceptor states ($N_{so}$) acting on the forward characteristics play a less important role due to their energetical position with regard to the Fermi level. The accuracy is then not as good for the acceptor states ($N_{so}$) than for the donor states ($N_{s1}$). The $\chi$ values determined by the modelization are consistent with those reported in the literature [9]. To our knowledge the physical reasons of the observed dispersion of $\chi$ values has not been studied in the literature.

On the contrary if we assume a possible thickness dispersion in the order of 2 Å we can determine the values of the other parameters. Such thickness variation could corresponds to the insulating layer inhomogeneities on the wafer. These calculations were carried out using as an example the curve 1 of the figure 4a.
We find so:

- For $\delta = 30\,\text{Å}$
  
  \[ N_{so} = 10^{12}\,\text{cm}^{-2},\quad N_{s1} = 3 \times 10^{11}\,\text{cm}^{-2}\quad V_{so} = 113\,\text{mV} \]

- For $\delta = 28\,\text{Å}$
  
  \[ N_{so} = 10^{12}\,\text{cm}^{-2},\quad N_{s1} = 5 \times 10^{11}\,\text{cm}^{-2}\quad V_{so} = 32\,\text{mV}. \]

Among these above two possibilities we can choose the first one which gives the $V_{so}$ value in accordance with the capacitance measurement for this sample (section 5). So with this reasoning the fluctuations of the thickness are not involved.

5. Capacitance and conductance-voltage characteristics.

5.1 EXPERIMENTAL RESULTS ON $C$ AND $G-V$ VS. BIAS AT DIFFERENT FREQUENCIES. — The curves of figure 5 (solid lines) present the variations of capacitance vs. bias for devices on n and p type wafers at several frequencies of measurement ($C_m$ in linear scale).

For devices on n type substrate (curves 5a) we observe, in accumulation, plateau values $C_{ma}$, which correspond to the $C_{ox}$ value (in the order of 1 900 pF) only at low frequencies (here 30 Hz). For higher frequencies the contact resistance $R_g$ of the samples provokes a decrease of the $C_{ma}$ values [10] (see equivalent circuits of Figs. 7a and b):

\[
C_{ma} = \frac{C_{ox}}{1 + R^2_s C^2_{ox} \omega^2} \quad \text{(valid if } \frac{1}{R_s} \gg G_f \text{)}.
\]

This relation permits to evaluate $R_s$. We found $R_s$ around 250 Ω.

For devices on p type substrate the accumulation is obtained for larger voltage value than in the case of n type device (Fig. 5b). It is obtained in accumulation region plateau values of $C_{ma}$ lightly increasing with bias $V_a$. The series-resistance is found to be around 400 Ω in this case.

Fig. 5. — Measured capacitance (solid lines) and conductance (dashed lines) versus applied voltage characteristics for devices on n(a) and p(b) wafer (linear plot for $C_m$ and $G_m$).

Fig. 6. — Measured capacitance (solid lines) and conductance (dashed lines) versus applied voltage characteristics for devices on n(a) and p(b) wafer (logarithmic plot for $C_m$ and $G_m$).

Fig. 5.

\begin{center}
(a)
\end{center}

\begin{center}
(b)
\end{center}
Accumulation begins at around \(-1\) V in p type devices and 0.1 V in n type. These results are in agreement with the semiconductor surface regime at 0 voltage bias: inversion for p type devices and depletion-accumulation for n type devices (see section 4.3.1).

The curves of figure 5 (dashed lines) present the variations of the conductance vs. bias voltage with $G_m$ in linear scale for the same devices as previously. The losses increase with the frequency [11] according to:

$$G_m = \frac{G_T + R_s C_{ox} \omega^2}{1 + R_s^2 C_{ox}^2 \omega^2} \left( \text{valid if } \frac{1}{R_s} \ll G_T \right).$$

The peaks in $G_m V_a$ curves in the depletion region are only observed with $G_m$ in logarithmic plot. Typical example is shown in figures 6a and b.

5.2 EVALUATION OF $N_{ss}$ AND $V_s$. — The conductance method of Nicollian and Goetzberger [1, 11-13] is suitable for the determination of interface state density $N_{ss}$ in MIS structure with very thin oxide layer. The necessary equivalent circuits of the MIS diode for this evaluation are shown in figures 7c and d. The n devices are in depletion in low reverse bias (Fig. 5a), so the evaluation of $N_{ss}$ is possible. The p devices are in inversion in reverse bias (Fig. 5b), and so we have not determined the interface state density in that case.

We found $N_{ss}$ values typically $5 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$ near the midgap for annealed LPCVD n devices and slightly higher for other n devices (around $10^{12}$ cm$^{-2}$ eV$^{-1}$ near the midgap). These values are consistent with those used in modelling section (4.3.2).

The determination of surface potential has been carried out with Berglund integral [11] on low frequency C-V characteristics (30 Hz).

The $V_{so}$ value (surface potential at 0 V) have been evaluated by HF measurement [1]. We have found generally a positive value, depending on the samples between 50 mV and 150 mV for n devices and about 600 mV and 800 mV for p type devices.

Finally we have reported on figure 8 the experimental (solid lines) curves $V_s$ vs. $V_a$ for two samples (on n and p type substrate). The dashed line represents, for example, a theoretical $V_s$ vs. $V_a$ curve obtained by the simulation program of section 4.3.2. The agreement between experimental and theoretical results is generally satisfactory except for some not annealed LPCVD n devices which are in accumulation for zero volt bias.

6. Conclusion.

In this paper Al-SiO$_2$-Si tunnel structures with thin oxide layers (30 Å) on n and p type wafers have been studied using measurements based on a microcomputer controlled system.

Interesting results may be deduced from the modelling of experimental I-V curves. The dispersion of these characteristics on the same wafer allow us to deduce dispersion of the most important physical parameters.
Thus, we have shown with the assumption of constant oxide thickness (typical value 30 Å) that the extreme experimental $I-V$ curves can be fitted with an electronic affinity variation lower than 0.2 eV and an interface states density variation lower than $9 \times 10^{11} \text{ cm}^{-2}$.

This study is able to provide very useful information about the dispersion of the most important physical parameters of the Si-SiO$_2$ interface for very thin insulator layers. It would so be possible to improve the technological process in order to obtain good quality thin oxide layers.

References