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Defects left after regrowth of amorphous silicon on crystalline Si : $C(V)$ and DLTS studies

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Résumé. — Du silicium p et n a été auto-implanté à 77 K avec des faisceaux multi-énergétiques dans le but d'amorphiser une couche de 0,3 à 0,4 μm sans introduire trop de défauts dans le cristal sous-jacent. Après recristallisation par recuit à 550 °C, on a caractérisé les défauts restant par les méthodes de capacité-tension ($C(V)$) et de spectroscopie transitoire des niveaux profonds (DLTS). Dans n-Si, on a trouvé une sous-couche de donneurs profonds en forte concentration tandis que dans p-Si, ils étaient présents en faible concentration. Ces pièges sont sans doute associés à l'auto-interstitiel qui se comporte différemment dans n-Si et p-Si.

Abstract. — n and p-type silicon have been self-ion implanted at 77 K with multi-energetic beams. This process was used to amorphize a 0.4 μm layer with a minimum amount of damage in the underlying crystal. After regrowth by a 550 °C anneal, the remaining defects were assessed by capacitance-voltage ($C(V)$) measurements and deep level transient spectroscopy (DLTS). In n-type Si, a buried layer of deep donors in large concentration was found, whereas in p-type Si, their concentration was small. These traps are believed to be associated with self-interstitials injected beyond the amorphous layer by the implantation process, their electrical activity depending on the nature of the majority carrier.

1. Introduction.

Solid phase epitaxial (SPE) regrowth of silicon amorphized by ion implantation has been studied by a number of techniques with a view towards characterization of the crystal perfection after complete regrowth. In particular, transmission electron microscopy (TEM) has shown a high density of twins and dislocations after regrowth of (111) wafers, and essentially no defects in (001) wafers [1-4]. Other studies using cross-sectional TEM specimens have shown that, in (001) regrown wafers, there is a layer of unresolvable defects at the amorphous-crystal interface [3, 4]. The expected profile of defects is shown schematically in figure 1a. Although we devised an implantation procedure to avoid these defect clusters, they were always present [4]. In (110) wafers, in addition to the layer of defect clusters already mentioned for the (100) case [4], microdefects were observed within the regrown layer. Thus, there seem to be two distinct regions (Fig. 1b); the amorphized-regrown layer contains a relatively low density of defects and is bounded by a dark band in which isolated defects cannot be resolved, except after high temperature, i.e., 800 °C, annealing [4]. This

paper presents the electrical properties of Schottky diodes made on n and p-type Si wafers of (001) and (110) orientation containing these defect structures. In the main, we have used capacitance-voltage, $C(V)$, and deep level transient spectroscopy, DLTS, to characterize the defects.

2. Experimental techniques.

2.1 SPECIMEN PREPARATION. — Specimens were prepared from commercially available Si wafers. Their characteristics are summarized in table I. The wafers were processed to produce the square diodes (0.88 mm edge) used throughout this study. After opening squares through 1 μm thick SiO_2 , multienergetic $^{28}\text{Si}^+$ ion implantation was performed at 77 K to produce an amorphous layer of about 0.4 μm thickness. This procedure was intended to minimize the creation of defects below the amorphous-crystal interface [4]. The amorphization was performed only in the central part of the wafers, leaving an annular control region which otherwise had the same processing history. This scheme allowed the detection and monitoring of contamination-induced deep levels,

Table I. — Characteristics of the silicon wafers deduced from measurements on U diodes for shallow impurities and on AR diodes for deep level energies. The symbol (A) refers to specimens annealed 2h at 650 °C (1 eV = 1.6×10^{-19} J).

Type	Orientation	Shallow impurity conc. cm^{-3}	Energy of deep levels $E_C - E_T$
n	(110)	1 to 4×10^{14}	0.7 0.6 (A)
n	(001)	10^{15}	0.5 0.6 (A)
p	(110)	3.5×10^{15}	0.65 (A)
p	(001)	6 to 9×10^{15}	0.6 (A)

Fig. 1. — Variation of defect concentration in SPE regrown (001) (a) and (110) (b) wafers as deduced from TEM observations [4].

see section 2.3. After cleaning, the wafers were annealed in nitrogen for 5 hours at 550 °C to allow complete recrystallization of the amorphous layer. Selected wafers were given an additional anneal of 2 hours at 650 °C; data from these wafers are designated by an A in the text and figures.

Schottky barriers were formed after the regrowth anneal by contact between platinum silicide (silicide formed at 500 °C) and n-type Si, and sputtered titanium and p-type Si. We then have four types of diodes; those made on the *unamorphized* annular regions of n and p-type Si, which we shall call U, and those made on *amorphized-regrown* n and p-type Si, which we shall call AR.

Current-voltage (I - V) characteristics were measured to assess diode quality. The n-type U diodes showed the expected behaviour : ideality factor $n = 1.05$, reverse current at low voltage $I_R \sim 10^{-9}$ A, breakdown voltage > 20 V. The AR diodes were noticeably degraded; in particular, I_R was about 10 times larger than for the U diodes. For p-type Si, the Ti sputtering did not produce good barriers, resulting in control diodes with poor I - V characteristics, the AR diodes being closer to ideality than the U ones. Nevertheless,

they were of sufficient quality to allow $C(V)$ and DLTS studies on the p-type Si. More details on the experimental procedures can be found in [5].

2.2 CAPACITANCE-VOLTAGE. — An automated profiler was used. It is based on the standard technique that deduces the free carrier concentration *versus* depth curves [6] by measuring the capacitance, C , as the reverse bias, V , is stepped. The values of concentration reported in table I have been measured by this technique; they are in agreement with the resistivities provided by the wafer vendors. The depth profile resolution is limited by the Debye length, which is between 500 nm and 50 nm in our wafers. We therefore expect the measured profiles to be a distorted representation of the true profile, and, thus, not directly comparable to the dimensions from TEM observations (Fig. 1).

2.3 DLTS. — Following a reverse bias pulse which fills traps, their emptying by thermal emission of carriers induces a variation in capacitance, $C(t) = C_0 + \Delta C(t)$; here, C_0 corresponds to the equilibrium capacitance i.e. t large. If $N(t)$ is the concentration of ionized impurities at time t , we have then :

$$\Delta N(t) = N(t) - N_0$$

and :

$$\Delta C(t) = C_0 \left[\left(\frac{\Delta N(t)}{N_0} + 1 \right)^{1/2} - 1 \right] \quad (1)$$

where N_0 is the ionized impurity concentration at equilibrium DLTS is simply a study of this $\Delta C(t)$ as a function of temperature.

The DLTS experiments were performed with the apparatus described in detail in [7]. Basically, it consists of a fast capacitance meter which performs

16 measurements of the capacitance decay, $\Delta C(t)$, at time intervals between 100 μ s and 1 s after the filling pulse. The data are stored and later used to plot $\Delta C(t_1) - \Delta C(t_2)$ versus temperature, T , in a range between 77 K and 373 K. Following Tomokage *et al.* [8] and others, there is an extremum in this curve when t_1 and t_2 satisfy the following relation with the emission rate $1/\tau$ being equal to $1/\tau_m$:

$$\frac{t_1}{t_2} \exp - \frac{t_1 - t_2}{\tau_m} = \left[\frac{1 + (\Delta N(0)/N_0) \exp - t_1/\tau_m}{1 + (\Delta N(0)/N_0) \exp - t_2/\tau_m} \right]^{1/2} \quad (2)$$

where the concentration of filled traps is described by :

$$\Delta N(t) = \Delta N(0) \exp - t/\tau, \quad (3)$$

and N_0 corresponds to the concentration of ionized impurities at equilibrium, (t large). If $\Delta N(0)/N_0 \ll 1$, equation (2) can be simplified to give the usual value for τ :

$$\tau_0 = \frac{t_1 - t_2}{\ln(t_1/t_2)} \quad (4)$$

which we have used in all our analyses. If the condition $\Delta N(0)/N_0 \ll 1$ is not fulfilled, the capacitance decay is not exponential with time, and equation (2) has to be used to calculate τ_m . It can be written, setting $r = t_2/t_1$, as :

$$\frac{\tau_0}{\tau_m} = 1 + \frac{1}{2 \ln r} \ln \frac{1 + (\Delta N(0)/N_0) \exp \left(\frac{\tau_0}{\tau_m} \frac{\ln r}{1 - r} \right)}{1 + (\Delta N(0)/N_0) \exp \left(r \frac{\tau_0}{\tau_m} \frac{\ln r}{1 - r} \right)} \quad (5)$$

The use of τ_0 instead of τ_m for the Arrhenius plot generally gives incorrect results. However, if the analysis is performed at constant r , as it usually is, the ratio τ_0/τ_m is a constant (Eq. (5)), and the activation energy for emission determined from the τ_0 approximation is correct.

We have used DLTS to verify that the diode fabrication process itself did not induce any contamination, i.e., spurious trap levels [5]. DLTS spectra of U diodes for (110) n-type Si did not show any features which could be related to traps in concentration larger than $5 \times 10^{11} \text{ cm}^{-3}$. For (001) n-type diodes, a broad vague line was observed, corresponding to electron traps in concentration of $7 \times 10^{12} \text{ cm}^{-3}$ ($E_C - 0.35 \text{ eV}$), which was much less than the shallow donor concentration, N_D . It was clearly a consequence of the annealing treatment since it was not observed in a wafer which was not annealed. The efficacy of DLTS monitoring was confirmed when a Pt deep level was observed on diodes from a wafer that inadvertently had been coated with 30 nm of the metal, and then had the Pt layer removed chemically, *prior* to the regrowth anneal. A Pt concentration of 10^{13} cm^{-3} ($E_C - 0.25 \text{ eV}$) was

measured in this case [5]. Diodes from this contaminated wafer were not used in our study.

For p-type Si, the DLTS spectra of U diodes showed some faint structure which vanished for long relaxation time readings ; this effect was probably related to the non-ideality of the diodes. The preparation of these diodes introduced no major contamination i.e., no deep levels in the Si, since there was no anneal following the barrier metal deposition.

3. Results.

3.1 $C(V)$ PROFILING. — Free carrier concentration versus depth curves are shown in figures 2 and 3 for several diodes prepared from different n-type wafers. The reproducibility for diodes from the same wafer was excellent. Both (001) and (110) processed wafers show a large carrier concentration increase at some distance from the Schottky contact (Fig. 2). Annealing at 650 °C did not induce any qualitative change in the profile.

The carrier profiles were strongly influenced by the temperature of measurement ; the peak observed on AR diodes disappeared entirely by 77 K, at which temperature their profile became identical with those of U diodes. This result shows that the peak in carrier concentration (Figs. 2 and 3) is due to the ionization of deep levels, which become « frozen out » at 77 K. We did not analyse the effect of deep ionization on carrier concentration profiles at intermediate temperatures, 77 K < T < 298 K.

For p-type Si, there is almost no difference between U diodes and AR diodes, indicating the absence of a large concentration of deep level centres.

Fig. 2. — Carrier density versus distance obtained by $C(V)$ profiling at room temperature on amorphized-regrown (AR) n-Si for (001) and (110) orientations. The curve marked « A » corresponds to a wafer which received an additional anneal at 650 °C.

Fig. 3. — Carrier density *versus* distance obtained by $C(V)$ profiling at various temperatures between liquid nitrogen and $+75\text{ }^{\circ}\text{C}$.

3.2 DLTS.

3.2.1 *n*-type AR diodes. — The DLTS behaviour of AR diodes showed several unusual features for *n* as well as *p*-type Si. For *n*-type Si, very strong DLTS peaks were observed (Fig. 4), corresponding to the emission of electrons from the deep donors revealed by $C(V)$ profiling. Their concentration was so high that $\Delta C(t_1) - \Delta C(t_2)$, at the DLTS peak, was a large fraction of the equilibrium capacitance (Fig. 4), and the capacitance transient was non-exponential [5].

This non-exponential behaviour may have several origins :

- (i) A trap emptying rate that varies with depth, that is, when the traps are located at the depletion region edge, where the carrier concentration falls off in a distance the order of the Debye length [13-15].
- (ii) A spatially varying emission rate [13, 16].
- (iii) A large trap concentration [9, 16].
- (iv) A distribution of trap level energies, which cause broadening of the DLTS peaks [11, 12].

All these origins of non-exponential transients are plausible in our experiments. We have a non-uniform trap distribution whose peak concentration is much larger than that of the shallow donors. A reasonable fit of the $\Delta C(t)$ curves could not be obtained using both equations (1) and (3). This finding indicates that the origin of the observed non-exponential transients is not simply that the condition $\Delta N(0)/N_0$ (or $\Delta C(t)/C_0$) $\ll 1$ is not realized. The complex nature of the defects giving rise to the traps may yield a distribution of energy levels and capture cross-sections which could induce broadening of the resultant DLTS peaks. Actually, we have always observed very narrow peaks (Fig. 4), about one half as wide as those calculated for a single level using the results of Goto *et al.* [10]. This peak narrowing is an unusual feature for which we have no explanation.

Fig. 4. — DLTS signal for AR diodes. The same rate window is used for both curves *viz.* $t_1 = 4.31\text{ ms}$ and $t_2 = 8.08\text{ ms}$. Both wafers were annealed at $650\text{ }^{\circ}\text{C}$ « A ». DLTS experimental conditions were : *n*-type : Reverse bias $V_R = -2\text{ V}$; pulse $V_P = -0.5\text{ V}$; room temperature capacitance = 107 pF ; capacitance variation at minimum = 26 pF . *p*-type : $V_R = -3\text{ V}$, $V_P = -0.5\text{ V}$; RT-capacitance = 67 pF ; capacitance variation at maximum = 0.6 pF .

We have looked for a mean to achieve exponential capacitance transients from our non-uniform, high density trap distributions. If the filling pulse brings the traps below the Fermi level for a time too short to reach saturation, the emission after setting back the reverse bias does not involve large capacitance changes. The transient is then exponential in time. Unfortunately, the DLTS set-up we used [7] could not produce pulses shorter than $1\text{ }\mu\text{s}$, a time which still filled the traps to saturation. We tried an alternate way to fill a small fraction of the traps ; voltage pulses with amplitudes of 0.1 V were applied. This procedure, in principle, does not give exponential transients [9], because the emission rate is spatially non-uniform [13]. The traps filled are limited to the decay of the Fermi distribution, of width kT , giving spatial variations in the emission rate at the crossing of the trap level and Fermi energy (edge region limit). These non-exponential transients obviously occur for uniform trap concentrations. This is not the case in our experiments, where exponential transients can therefore be expected to exist. They have been predicted for a step-wise distribution of traps where no emission takes place at the edge region limit when using small amplitude pulses [9]. In this case, the filled traps are in low uniform concentration because they correspond to the asymptotic portion of the Fermi distribution, far above the Fermi energy which hardly moves during the pulse ; there is no spatial variation of the emission rate related to small trap concentration, giving exponential transients.

We have indeed always found exponential transients after small amplitude pulses [5], and trap level energies

derived from these data probably constitute our most reliable results (Table I). The DLTS experiments that we have performed on n-type silicon do not provide information on the trap concentration since, either they have non-exponential transients, or they correspond to unsaturated traps. They do, however, allow the determination of the energy levels associated with these traps. For that purpose we have utilized a computer program which makes use of equation (4) to make an Arrhenius plot of the emission rates. They are linear over four decades even for non-exponential transients, provided we keep $r = t_2/t_1 = \text{constant}$. The agreement for the various bias and pulse conditions is fair (Fig. 5). The scatter of the slopes is not too large except for experiments under large reverse bias [5], where the emitting traps are close to the junction ; here, large electric fields preclude satisfactory results. The activation energies determined from our analysis are reported in table I.

3.2.2 p-type AR diodes. — The DLTS signals on p-type Si showed some unstable behaviour which was likely due to the non-ideality of the Schottky barrier [5]. Peaks were systematically observed for the specimens annealed at 650 °C (Fig. 4), but no typical feature was observed after 800 °C anneals. The peaks correspond to the emission of minority carriers, i.e., electrons (Fig. 4), although no injection pulse was applied to the diodes ; this result may be due to the quality of the Ti barriers. The transients are exponential in time and correspond to a small variation of capacitance (Fig. 4). The electrons are emitted by traps which are very similar to those observed in n-type Si (Fig. 5), but in much smaller concentrations. The concentration, however, cannot be determined since the traps are not saturated by electrons. Nevertheless, $C(V)$ profiling has shown that they are in much lower concentration in p-type Si than in n-type Si. The values for their energy levels are shown in table I.

4. Discussion.

4.1 CONCENTRATION PROFILES. — Capacitance-voltage characteristics often have been used for impurity profiling, including when they have been influenced by a distribution of deep level centres [17, 18]. Our profiles (Figs. 2 and 3) are similar to those cited in these references. The Debye length, L_D , is the limit of spatial resolution for this technique. It is clear that the profiling on our (110) n-type wafers is strongly distorted, since, in this case, L_D is about 500 nm, which is large with respect to the width of the defect distribution. The experimental situation for the (100) n-type wafers was somewhat more favourable ; here, L_D was about 100 nm. In spite of the distortion, we can estimate the position of the deep level centres and compare it with the TEM observations. The distances in figures 2 and 3 correspond to the edge of the depletion region. The actual positions of the deep level centres are at the intersection of their electronic energy levels with the Fermi level. Since the donor concentration is constant

Fig. 5. — Arrhenius plot for thermal emission rates deduced from DLTS spectra using equation (4) with $r = t_2/t_1 \approx 1.9$. The light lines correspond to n-type diodes for various conditions of reverse bias V_R and pulse V_P [5]. Thick lines are the more representative results for n and p-type Si corresponding to the following conditions :

a) (001) orientation. AR 4 and AR 6 (A) : $V_R = -3$ V, $V_P = -2.9$ V. AR 24 (A) : $V_R = -3$ V, $V_P = -0.5$ V.
b) (110) orientation. AR 1 : $V_R = -1$ V, $V_P = -0.8$ V. AR 3 (A) : $V_R = -3$ V, $V_P = -2.9$ V. AR 11 (A) : $V_R = -3$ V, $V_P = +1$ V.

to the right of the peaks (Figs. 2 and 3), we can calculate the true position of the roll off in free carrier concentration. To first order, the true trap distribution can be derived from its measured $C(V)$ « image » by a translation, λ , given by an integration of Poisson's equation [5] :

$$\lambda = \left[\frac{2 \epsilon_S (E_F - E_T)}{q^2 N_D} \right]^{1/2} \quad (6)$$

where, E_T = trap energy level,

E_F = Fermi energy level,

ϵ_s = dielectric constant of Si, $= 10^{-10}$ F/m,

q = 1.6×10^{-19} Coulomb,

and N_D = donor density.

For (110), we have $N_D = 10^{20} \text{ m}^{-3}$, $E_C - E_T \sim 0.65 \text{ eV}$ (Table I), and $E_C - E_F = 0.4 \text{ eV}$. Thus, we find $\lambda \cong 2 \text{ } \mu\text{m}$.

For (001), we have $N_D = 10^{21} \text{ m}^{-3}$, $E_C - E_T \sim 0.55 \text{ eV}$ (Table I), and $E_C - E_F = 0.3 \text{ eV}$. In this case, $\lambda \cong 0.6 \text{ } \mu\text{m}$.

If we shift the apparent free carrier concentrations by $2 \text{ } \mu\text{m}$ for (110) and by $0.6 \text{ } \mu\text{m}$ for (001), taking half-maximum positions, they fall at $0.5 - 0.7 \text{ } \mu\text{m}$, and $0.4 - 0.5 \text{ } \mu\text{m}$, respectively. These values correspond closely to the depth of the dark bands observed by TEM at the amorphization limit. A more sophisticated analysis of the profiles, as in [18], was not attempted, even though it might reproduce more of the details of the curves in figures 2 and 3. Our methods were probably not sensitive enough to separate the electrical activity of the small defects in the regrown (110) layers [4], since they were overwhelmed by the large signal associated with the buried layer of cluster defects at the amorphization limit. For p-type Si, deep level centres were not detected by $C(V)$ profiling.

4.2 NATURE OF DEFECTS. — The amount of damage left in the regrown layer has been qualitatively explained on the basis of the mechanism of solid phase epitaxy (SPE) on the various crystallographic planes of Si [1, 3]. According to these models, regrowth of (001) crystal leads to less defective layers and regrowth of (111) yields the most defective ones, the (110) case being intermediate. This picture is in agreement with our observations [4]. Electrical measurements are not expected to give any signal from the regrown layer on (001), contrary to (110) Si where crystal defects [4] should give an observable DLTS signal [19]. The residual defect density within the regrown layers is difficult to assess; however, it is likely that the number of dislocation levels is not larger than occur as a result of plastic deformation [19], and is therefore much too small to explain the peaks in the carrier profiles (Fig. 2).

The observation of these small concentrations of traps *within* the regrown layer have been made difficult in AR diodes of both orientations by the residual layer of defect clusters at the amorphous-crystal interface. Our TEM study shows that their nature and concentration are similar in n and p-type Si for both orientations (001) and (110) [4]. However, $C(V)$ profiling and DLTS measurements suggest that the electrically active defects are orders of magnitude higher in concentration in n-type than in p-type Si. This conclusion is based on the comparison of (110) p-Si and (001) n-Si which have the same background free carrier concentration (Table I). This discrepancy may be explained by one of three possibilities. *First*, the number of defects created in

p-type Si is smaller than in n-type material. This hypothesis is inconsistent with the amorphization procedures, which are identical for both types, and with TEM observations. *Second*, the defects anneal out more rapidly in p-type than in n-type Si [20]. Actually, the annealing rate is not substantially changed between 550°C and 650°C for n-type Si, since TEM, $C(V)$ profiling and DLTS indicate the same trap concentration [4, 5] (Fig. 2). TEM observations show the same defect configurations at the amorphization limit for n and p-type, with significant annihilation and growth of dislocation dipoles and loops being achieved only after 800°C annealing [4]. That is, we did not observe any qualitative difference in the annealing of defects in n and p-type Si. *Third*, the density of lattice defects present in n and p-type Si may appear to be similar in the TEM, since that technique is sensitive only to lattice strains. The electrically active defects may differ from those observed by TEM; however, they should be in equal concentrations in both types of Si, since they are produced by the same physical process.

We now discuss this last possibility in relation to the formation mechanism of the defects that lie at the amorphous-crystal interface. The implanted Si ions lose their energy in the amorphized region; the projected range for the highest energy used is $0.28 \text{ } \mu\text{m}$ (standard deviation $0.12 \text{ } \mu\text{m}$) [21], which corresponds to the thickness of the amorphized layer. Beyond the amorphized layer, Si ions are injected into the lattice, and are likely to diffuse. The energy deposited by the ion beam can raise the lattice temperature and enhance interstitial Si diffusion. In our experiments, care has been taken in cooling down the specimen to minimize diffusion. However, the results show that a substantial density of defects is still present. It is likely that they have an interstitial nature, although annealing at 550°C and 650°C has certainly decreased the strain energy by allowing clustering. A continuous distribution of cluster sizes probably is still present, only the biggest giving rise to a strain contrast visible by TEM.

The electrical properties of these interstitial clusters in n and p-type Si have been observed in our experiments. The exact nature of the electronic levels associated with self-interstitials in silicon is a problem currently being studied theoretically [22-24]. Initial results suggest that the self-interstitial should be stable on a tetrahedral site in p-type Si, giving no level in the gap, and that the presence of deep levels for the hexagonal position should make it the stable one in n-type Si [23, 24]. This model is consistent with our observations that the density of deep level centres in p-type AR diodes is small relative to their density in n-type diodes.

5. Conclusions.

Electrical characterization of Schottky barrier diodes made on amorphized and SPE regrown silicon was

dominated by the buried layer of deep level centres at the limit of the amorphized layer. These centres are stable up to at least 650 °C, and have been observed on cross-sectional TEM specimens. DLTS experiments were performed, and only the use of small amplitude pulses in reverse bias produced exponential transients. The high density of defects in the buried layers is likely to be associated with interstitial clusters, which yield deep levels only in the n-type case.

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