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SILICON PROCESSING III.

AN ADVANCED PROCESSING TECHNOLOGY FOR HIGH VOLTAGE BIPOLAR IC'S

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Résumé. — Le développement de circuits intégrés vers les tensions élevées introduit des compromis technologiques difficilement tenus au niveau de la réalisation des trois types de transistors : npn, pnp latéral et pnp substrat. Une investigation de ces limitations, conduite à l'aide d'un modèle bidimensionnel, a montré que, pour obtenir des tenues en tension de l'ordre de 150 V, les paramètres de l'épithaxie doivent être optimisés pour le transistor npn et les limitations inhérentes aux pnp sont alors repoussées au moyen de nouvelles solutions.

Deux possibilités ont été étudiées. Dans le premier cas une implantation d'ions non localisée avant épithaxie assure une augmentation de tenue en tension de 30 V. Dans le deuxième cas le dopage de l'épithaxie est augmenté près de la jonction émetteur-base en effectuant une implantation avant la diffusion émetteur et avec le même masque.

Un processus technologique haute tension a été mis au point. Des tenues en tension de 160 V ont été obtenues pour les trois types de transistors.

Abstract. — The development of integrated circuits toward high voltages introduce difficult compromises in regard to the technological process of three types of integrated transistors : npn, vertical pnp and lateral pnp.

An investigation of these limitations has been done using a bidimensional model. The main results issued from this work show that, for voltages of 150 V, the parameters of the epitaxial layer have to be optimized for npn transistors and the limitations inherent to pnp transistors will be overcome by means of new solutions. Two possibilities have been studied. In the first case an ion implantation is performed without masking before epitaxial growth. This improves vertical pnp transistor breakdown voltage in excess of 30 V. In the second case the doping of the epitaxial layer is increased near the emitter base junction by an ion implantation before the emitter diffusion while using the same mask.

A high voltage technological process has been carried out. 160 V collector emitter breakdown voltage has been achieved for the three types of above mentioned transistors.

1. Introduction. — For many applications like telephone, control, automation, integrated circuits must be able to support high voltage. This is also necessary in cases like automotive applications where severe parasitic overvoltages are superimposed on supply voltages.

The improvement of breakdown voltage (BV_{CEO}) of npn transistors needs an increase of geometric parameters (junction depth, guards, epitaxy thickness) and also an increase of epitaxial layer resistivity. However this layer (Fig. 1) acts as the base of lateral and vertical pnp transistors. Therefore the p substrate/n epitaxy junction depletion layer shifts rapidly toward the p emitter and punch-through occurs. A new increase of epitaxial layer thickness cannot be allowed because the performances of npn transistors would be decreased. The problem looks the same for the lateral pnp transistor. To obtain a specified BV_{CEO} the required emitter collector distance is such that other performances remain poor.

The work shown here consists in its first part to an evaluation of the limits of supply voltages which can be applied to the three types of integrated transistors isolated by junction. Then a theoretical profiles

FIG. 1. — Cross sectional view showing the classical integration of the three transistor types.

approach has been performed in order to overcome those limitations. Using these results a high voltage technological process has been carried out.

2. Computations of BV_{CEO} for npn and pnp integrated transistors. — An investigation of the BV_{CEO} limi-

tations has been done using a bidimensional model based on regional analysis [1]. This model is interesting in order to take into account the real profiles in two dimensions for the case of composite junction like epitaxy-isolation walls.

For npn transistor the base profile is for the two directions x and y :

$$N_B = 4.5 \times 10^{18} x \exp - \left(\frac{x}{L_A} \right)^2 \text{ at/cm}^3 \quad (1)$$

with $L_A = 1.5 \times 10^{-4}$ cm.

A junction depth of 4.2μ avoiding curvature effect up to 200 V was the first result obtained.

Taking into account the redistribution of buried layer the collector profile becomes :

$$N_C = N_D + 8 \times 10^{18} x \operatorname{erfc} \left(\frac{W - x}{L_{BL}} \right) \text{ at/cm}^3 \quad (2)$$

with : N_D and W : doping concentration and thickness of epitaxial layer ; L_{BL} : diffusion length of buried layer impurity depending on the epitaxial thickness.

At each increment of collector voltage the electric field is calculated and the ionization integrals are solved according to Lee *et al.* [2]

$$\frac{\exp \left[- \int_{x_p}^{x_n} (\alpha_n - \alpha_p) dx \right] + \frac{J_p}{J_n}}{\left(1 + \frac{J_p}{J_n} \right) \left(1 - \int_{x_n}^{x_p} \alpha_n \exp \left[- \int_{x_n}^{x_p} (\alpha_n - \alpha_p) dx' \right] dx \right)} = 1 + \frac{1}{H_{FE}} \quad (3)$$

J_p and J_n are the minority carrier densities, holes and electrons. For ionization rates α_n and α_p we have taken Grant's values [3].

x_p and x_n are the width depletion in the base and collector regions. The results obtained with $H_{FE} = 80$ are plotted in the figure 2.

To carry out the breakdown voltage of the vertical pnp transistor we calculate the electric field distribution corresponding to the composite junction epitaxy/substrate and epitaxy/isolation walls. For this last one an experimental profile obtained from secondary ionic emission is taken. The first calculation was done with a substrate resistivity of $10 \Omega\text{-cm}$. According to a previous theoretical and experimental work this value is a good compromise in regard to parasitic lateral npn, collector pnp resistance and parasitic capacitances. We have taken into account the displacement of substrate/epitaxy junction during the isolation-walls diffusion. The calculated values versus the epitaxial parameters are shown in figure 3 in solid line. From figures 2 and 3 one can see that npn and pnp BV_{CEO} of about 150 V lead to an excess of npn epitaxy thickness, increasing high injection effects and decreasing performances.

FIG. 2. — Collector emitter breakdown voltage of npn transistor versus epitaxial parameters. The buried layer redistribution is taken into account. $XJ_{BC} = 4.2 \mu$, $H_{FE} = 80$.

FIG. 3. — Collector emitter breakdown voltages of pnp transistors versus epitaxial parameters. The solid lines are for a substrate resistivity of $10 \Omega\text{ cm}$. The dotted lines are for a substrate resistivity of $20 \Omega\text{ cm}$.

3. The breakdown voltage improvement of the vertical pnp transistor. Theoretical approach. — To improve BV_{CEO} of vertical pnp the first idea might consist of pushing down the space charge in the substrate by means of high resistivity. In regard to parasitic lateral npn, this can be achieved if implanted foundations $p+$ are used. Indeed in this case buried layers are surrounded by a guard ring and the gain of parasitic transistors are reduced. The BV_{CEO} calculations for a

substrate resistivity of 20 Ω -cm are plotted in figure 3 in dotted lines. This solution is not suitable because the collector pnp resistance is increased and the problem of lateral pnp is not solved. Therefore the best solution for voltages of about 150 V consists of optimizing parameters of the epitaxial layer for npn transistors. Then the limitations inherent to pnp transistors are overcome by means of new solutions. These are based on the location of an n doped layer between collector and emitter with an optimized concentration profile to confine the base-collector space charge. To act properly this layer must be continuous, either completely surrounding the emitters or overlaying the isolation walls.

In the first solution an ion implantation is performed without masking before epitaxial deposition (layer A in figure 4). During the thermal operations this implant diffuses in the epitaxial layer like the n+ buried layer. So we have taken for the base profile :

$$N_B = N_D + \frac{Q_B}{\sqrt{\pi} L_A} x \exp - \left(\frac{x - w}{L_A} \right)^2 \quad (4)$$

FIG. 4. — First solution improving the BV_{CEO} of the vertical pnp. An arsenic implantation is performed without masking before epitaxial growth.

Q_B is the arsenic implanted dose and L_A is the corresponding diffusion length. The BV_{CEO} of the npn transistor is not disturbed as long as the multiplication avalanche is avoided near the isolation walls. The results of computations are plotted in the figure 5 giving BV_{CEO} and H_{FE} versus the arsenic implanted dose. This method whose main advantage is simplicity improves vertical pnp BV_{CEO} in excess of 30 V without disturbing the performances of the npn transistor.

The second solution improves the characteristics of both lateral and vertical pnp transistors. But the calculations have been performed only for the vertical pnp. The surface effects are not important for this one compared to the lateral pnp. The doping of the epitaxial layer is increased near the emitter-base junction by an ion implantation performed before the

FIG. 5. — Breakdown voltage and forward gain of vertical pnp transistor versus arsenic implanted dose. The parameters of epitaxial layer are : $\rho = 12 \Omega$ cm and $W = 24 \mu$.

emitter diffusion of the pnp transistors using the same mask (layer B in figure 6). Now the base profile is :

$$N_B = N_D + \frac{2 Q_{B'}}{\sqrt{\pi} L_{A'}} x \exp - \left(\frac{x}{L_{A'}} \right)^2 \quad (5)$$

FIG. 6. — Second solution improving the BV_{CEO} of both vertical and lateral pnp. A phosphorus implantation is performed in the emitter area with composite masking.

$Q_{B'}$ and $L_{A'}$ are the phosphorus implanted dose and the corresponding diffusion length respectively. Again here the gaussian distribution is correct because the diffusion length is much higher than the range project. The results of these computations are shown in the figure 7. Three diffusion times have been considered. The BV_{CEO} improvement is greater than in the first case. Therefore as a drift field is built in the base, dynamic characteristics are improved.

FIG. 7. — Breakdown voltage and forward gain of vertical pnp transistor versus phosphorus implanted dose. The substrate resistivity is $10 \Omega \text{ cm}$. The parameters of epitaxial layer are: $\rho = 12 \Omega \text{ cm}$ and $W = 24 \mu$.

4. **Processing and experimental results.** — Figure 8 shows the cross-section of each transistor at the end of the fabrication sequence. In order to make full use of the described high voltage solutions it needs to introduce some improvements in the process. The p-type CZ pulled substrate, $\langle 111 \rangle$ oriented and $10 \Omega\text{-cm}$ resistive, was initially annihilated in a nitrogen atmosphere. To minimize surface problems, all the oxidations were performed with HCl.

After the buried layer diffusion the foundations have been implanted. A 180 keV boron implant for the isolation and a 380 keV phosphorus implant for the collector sink have been used. Then to test the first high voltage solution several arsenic doses without masking have been implanted. In consideration of all these implantations the silicon had to be regenerated

FIG. 8. — Cross section of three types of integrated transistors built with the high voltage process. The two high voltage solutions are shown here. The first one uses the layer A and the other is based on the layer B. Normally only one of them is chosen.

carefully before epitaxial growth. For this last one we took the calculated values, 24μ for the thickness and $12 \Omega\text{-cm}$ for the resistivity. The operating conditions have been optimized to avoid unwanted doping coming from the previous implantations.

After predeposition collector sink, isolation walls and p diffusions were self-aligned by means of composite masking. Before base diffusion the wafers, processed with the second high voltage solution, were phosphorus implanted in the p emitter areas using a selected photoresist mask. A diffusion length $L_A = 5 \mu$ has been chosen. To avoid parasitic MOS a sandwich of pyrolytic oxide and doped polycrystal was deposited after emitter diffusion under aluminium. The polycrystal, which is positive with respect to the epitaxy acts as a shield and prevents the upper silicon surface from inversion.

The measured results of BV_{CEO} and H_{FE} are listed in the table I. In consideration of npn the results agree well with the theory on an average as we can see in the

TABLE I

Measured results

Wafers number	Implant	nnp		Vertical pnp		Lateral pnp	
		H_{FE}	BV_{CEO}	H_{FE}	BV_{CEO}	H_{FE}	BV_{CEO}
1	none	60	158 V	420	79 V	235	105 V
2	1 st 2×10^{11}	75	155 V	450	78 V	255	108 V
3	solut. 5×10^{11}	80	150 V	470	76 V	230	110 V
4	As 10^{12}	78	152 V	360	91 V	225	102 V
5	400 keV 2×10^{12}	83	128 V	230	115 V	280	95 V
6	2nd 10^{12}	68	164 V	320	90 V	220	115 V
7	solut. 2×10^{12}	88	145 V	250	115 V	205	125 V
8	P 5×10^{12}	80	170 V	120	155 V	130	160 V
9	150 keV 10^{13}	65	168 V	110	165 V	110	182 V

figure 9. However some deviations occur sometimes. This is generally a consequence of an apparent shift and deformation of the buried layer. These phenomena, which are more important with higher epitaxial thickness, make the first alignment after epitaxial growth difficult, and the guards we took in our masks were somewhat shorter.

FIG. 9. — Experimental results for the npn transistor. The circles are used for the wafers processed with the first high voltage solution and crosses for the wafers processed with the second high voltage solution. The solid and dotted lines show the calculation for the first and the second solution respectively.

The BV_{CEO} reducing for arsenic doses higher than 10^{12} at/cm² is smaller than the calculated values. Perhaps this arises from the difficulty having a p+ foundations profile approximation which fits well. There is the same for the vertical pnp as we can see in the figure 10. Moreover the theoretical curve seems shifted toward lower doses. Likely this arises from the arsenic out diffusion which occurs at the beginning of the epitaxy growth. With the second high voltage solution the agreement between measures and theory are quite good for the vertical pnp. A diffusion length of $5\ \mu$ and a phosphorus dose of 8×10^{12} at/cm² fit well with the objective. These values are not critical at all.

For the lateral pnp the BV_{CEO} are shown in the figure 11. A relatively high BV_{CEO} is obtained because measured transistors have a drawn channel width of $25\ \mu$ m. This is a bit too high. However the static gain remains correct. This confirms that surface effects have been greatly reduced in this process.

Wafers 1 and 9 were cut. The pnp transistors were encapsulated and the maximum of transition frequency was measured at 50 MHz with $V_{CE} = 150$ V. In the case of vertical pnp, 12 MHz and 65 MHz have been measured for wafers number 1 and 9 respectively.

FIG. 10. — Experimental results for the vertical pnp transistor. The circles and crosses have the same meaning as in the figure 9. The solid and dotted lines show also the calculation for the first and the second solution respectively.

FIG. 11. — Experimental results for the lateral pnp transistor. Again here the circles and crosses have the same meaning as in the figure 9.

For the lateral pnp 8 MHz and 60 MHz have been obtained respectively. Moreover current gain conservation has been greatly improved.

5. Conclusion. — The development of integrated circuits toward high voltages pointed out the limitations inherent to pnp transistors. Voltages greater than 100 V are generally limited by punch-through. A study of these limitations has been done using a bidimensional model and in order to avoid them new

solutions have been carried out. Using these latter and some other improvements a processing sequence was worked out. BV_{CEO} of 160 V has been achieved for the three types of transistors issued from this process. The limitation comes from the buried layer redistribution into the epitaxy during the isolation diffusion although p+ foundations are used. However using enhanced diffusion [4, 5] by means of vacancies

supersaturation arising by implantation damage expansion [6]. BV_{CEO} up to 200 V are possible with junction isolation.

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