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HOT ELECTRONS INJECTION INTO THE OXIDE OF A SILICON-ON-SAPPHIRE IGFET AT LOW OPERATING VOLTAGE

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Résumé. — On décrit une méthode expérimentale qui permet de mesurer, pour une tension de fonctionnement faible, l'injection dans l'isolant de grille (SiO_2) d'électrons du substrat d'un transistor à effet de champ réalisé en technologie *Silicium sur Corindon.* Notre but est d'identifier les paramètres essentiels qui régissent les phénomènes d'instabilité des transistors à effet de champ dus aux électrons chauds. On observe qu'une probabilité d'injection non négligeable ($P \simeq 10^{-10}$) existe pour une tension de substrat réduite à 2,2 V et une tension de grille égale à 2,5 V, pour des dopages similaires à ceux qui seront utilisés pour les dispositifs *submicroniques.* Un modèle basé sur le concept de l'*électron chanceux* décrit très bien les résultats expérimentaux, sauf pour des champs électriques dans l'oxyde inférieurs à 1×10^6 V.cm^{-1}. Suivant ce modèle, on trouve un libre parcours moyen équivalent entre collisions de l'ordre de 100 Å, c'est-à-dire pratiquement le même que celui observé pour du silicium massif. Ce modèle doit servir à définir la plage des tensions de fonctionnement qui évite ou limite la dérive du seuil de conduction des dispositifs subminiatures très dopés réalisés en technologie S.S.C.

Abstract. — An experimental method is described for measuring electrons injection from the electrical substrate of a silicon-on-sapphire IGFET into the gate insulator at low operating voltage. The aim of these experiments is to identify the relevant parameters which govern hot-electron related instability problems in IGFET. We notice that a significant injection probability ($P \simeq 10^{-10}$) exists for $V_{\text{substrate}}$ as low as 2.2 V and $V_{\text{gate}} = 2.5$ V and for doping levels which are consistent with V.L.S.I. trends. Except for oxide field lower than 1×10^6 V cm^{-1}, we found that a *lucky-electron* model describes the experimental data very well. Using this model, it is concluded that the equivalent collision mean free path is about 100 Å for electrons in S.O.S., and so, practically the same as the value observed for bulk silicon. This model may be useful for predicting the safe operating voltages of highly-doped submicron S.O.S. devices in order to avoid threshold instabilities.

1. **Introduction.** — The present trend in I.G.F.E.T. technology is towards very large scale integration (V.L.S.I.) devices which will need shorter channel lengths, shallower junctions, thinner gate insulators and higher substrate doping.

One can expect that one of the serious problems encountered will be the effect of high fields, associated with high doping levels, on device stability and reliability if the operating voltages are not reduced by some scaling factor.

If the electric field in the semiconductor increases, the carriers drifting in this field have some opportunity to fall through an important potential drop without having lattice collisions, and some of them will get sufficient energy to overcome the silicon-insulator barrier and be injected into the gate insulator. Most of these carriers cross the insulator layer and reach the gate electrode where they create some gate current but a weak part of them is trapped in the insulator and cause a shift in the characteristics of the devices — in particular, in the threshold voltage —; this phenomenon affects the stability of the devices and also their reliability if the trapping is irreversible.

The microelectronics designers will have to take these constraints into account and evaluate the optimum parameters (geometry, insulator thickness, doping levels, ...) and then, the maximum applied voltages to keep this instability low. It explains the need of an accurate model of the emission of hot carriers from the silicon substrate into SiO_2 — which can be C.A.D. oriented. Although there have been many experimental and theoretical studies [1-4] devoted to understanding the hot carriers injection process, very little work has been published on the particular case of thin film devices using the silicon on sapphire (S.O.S.) technology. This technology has proved to be very efficient for making fast C-M.O.S. devices, however while stepping on towards V.L.S.I. devices — where the channel lengths will be of the order of the μm and the doping levels higher than 10^{16} at/cm^3 — it is important to know better the carriers emission process in this structure where this phenomenon could be slightly different from the one in the bulk substrate devices because of lattice defects.

In this paper, we describe an experimental method for measuring the dependence on doping profile, substrate (1) voltage and oxide field of the emission probability of hot carriers in S.O.S. devices. The measured emission probability gives a good index of the emission process and consequently should be very useful to evaluate threshold instability problems in S.O.S.-M.O.S. transistors and also to forecast the reliability (in other words the *life-time*) of such devices.

In section 2, we describe in detail the experimental method; in section 3, we give experimental results showing the influence of gate and substrate voltages on emission process. In section 4, the results are analysed and discussed using the *lucky electron* concept including Schottky lowering of the interface barrier.

2. **Experimental method.** — The experimental method is derived from an optically induced hot electrons injection experiment as proposed by Ning [1]. A particular bias arrangement allows us to measure easily the charge amount injected into SiO_2 which is the sum of the charge of the carriers collected by the gate and the charge trapped in the insulator layer.

The device is N channel, Al-SiO_2-Si, T shaped I.G.F.E.T. on a sapphire substrate. The channel is 16 μm long and 50 μm wide. The substrate which is about 0.8 μm thick, is boron implanted; the doping profile has been measured by a method based on that one described by Buehler [5] and is shown in figure 1. We shall return to this point in section 4.

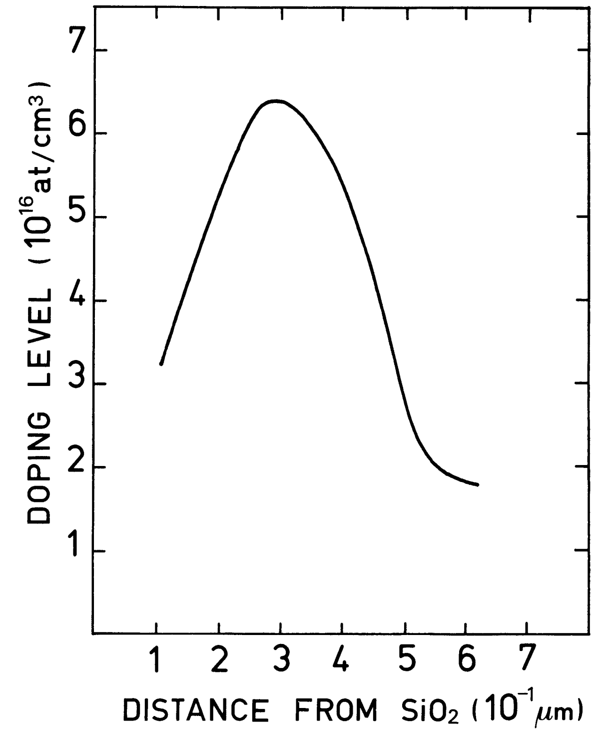

FIG. 1. — Doping profile of the silicon on sapphire layer of the device.

2.1 MEASUREMENT SET UP. — Referring to figure 2 :

— the gate can be positively biased or left floating by lifting the probe P ;

— a negative voltage V_{sub} is applied to the substrate and the substrate current I_{sub} is measured ;

— the source and the drain are grounded except for a small alternative signal (E_0, f_0) which is used to record the channel conductance by means of a lock-in amplifier and a $Y(t)$ recorder.

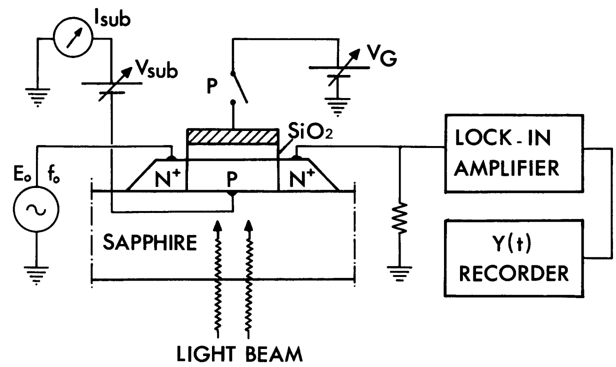

FIG. 2. — Schematic of the experimental set up for studying optically induced hot electron injection into SiO_2.

The silicon substrate underneath the gate is illuminated through the sapphire using a focusing arrangement not shown here.

2.2 BIASING CONDITIONS. — The substrate is reverse biased with respect to source and drain while a positive bias V_G is applied to the gate so that an inversion channel exists; with these biasing conditions the energy bands diagram is that given in figure 3.

Note that the grounding of source and drain :

1) keeps the channel equipotential and forms an electric screen which allows to independently vary the electric field in the insulator and the substrate potential, V_{sub} ;

2) makes the fields in the insulator and the silicon perpendicular to the interface Si-SiO_2 and therefore allows to consider the problem as unidimensional, at least in first approximation, provided that the source or drain depletion layer width is small compared with the channel length.

2.3 OPTICALLY INDUCTION OF A PRIMARY CURRENT. — Electron hole pairs are created in the substrate by a very thin light beam produced by a halogen light bulb and focused through the sapphire in the very middle of the gate area. The beam section has been reduced (about 10 μm in diameter) so that all the pairs are generated in the substrate at a distance greater than the diffusion length from the source and the drain. With these conditions, the created electrons cannot be

(1) In the following, *substrate* always shall mean *electrical substrate* which has to be distinguished from the insulating substrate (sapphire).

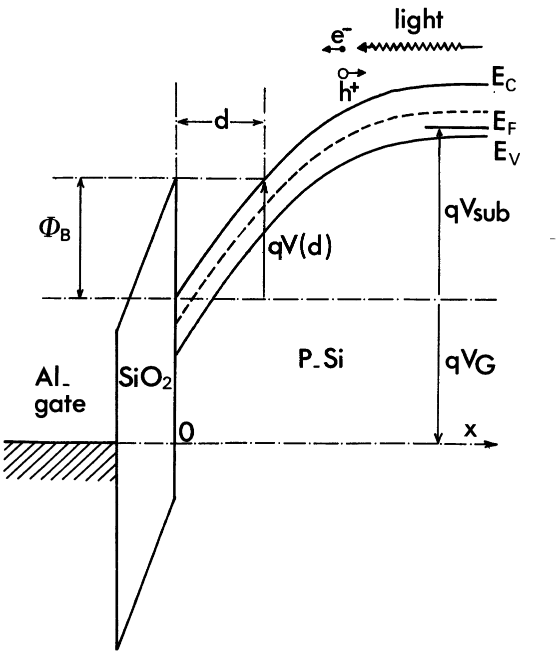

FIG. 3. — Schematic of the energy band diagram of an n-channel MOS transistor during hot electron injection.

collected directly by source or drain and thus, the photocurrent is composed only with electrons which have drifted perpendicularly to the interface Si-SiO_2 in the electric field of the depletion layer underneath the channel. This photocurrent, measured as I_{sub}, represents exactly the primary current of the emission process, i.e. the hot electrons source flux : this point is very important to measure the absolute emission probability rather than some relative value. Note the particular fitting between our experimental arrangement and S.O.S. technology since this last condition can be verified only if the diffusion length is short.

2.4 EMISSION PROBABILITY MEASUREMENT. — The electrons gain energy from the electric field in the depletion region as they drift towards the interface. Those electrons reaching that interface with energy greater than the Schottky lowered Si-SiO_2 interface barrier are emitted into the insulator, those not emitted are collected by the source or the drain.

The emission probability of an electron can obviously be expressed as the ratio of the total emitted current, I_E, to the primary photocurrent, I_{sub}, assuming that all the electrons which constitute this primary current have had the same physical history. This last condition is quite perfectly fulfilled in accordance with the statements given in the last paragraph. So :

$$P = I_E/I_{sub} .$$

Due to device size and light focusing, the resulting gate current is very small (down to 10^{-16} A) and cannot be directly measured, so an indirect method, with the FET under study acting as an electrometer, is used.

After a preliminary bias, the gate is left floating so that, in the absence of charge injection, the channel conductance, g, will keep constant. The charge equilibrium implies :

$$Q_n + Q_{sub} + Q_G + Q_T = 0 \tag{1}$$

where Q_n is the channel charge, Q_{sub} is the charge in the depletion layer, Q_G is the gate charge, Q_T is the trapped charge.

When the device is illuminated, with suitable biasing conditions, electrons are emitted into SiO_2 : they are either trapped in the insulator or collected by the gate. The floating gate condition implies :

$$I_E = \frac{d}{dt}(Q_G + Q_T) \tag{2}$$

I_E being the emitted current.

Equations (1) and (2) imply :

$$I_E = -\frac{d}{dt}(Q_n + Q_{sub}) . \tag{3}$$

But Q_{sub} is constant for a given V_{sub} and then :

$$I_E = -\frac{dQ_n}{dt} . \tag{4}$$

So the emitted current is equal to the opposite of the channel charge variation. Now, Q_n is connected to the channel conductance, g, by the relation :

$$g = -\frac{Z}{L}\mu_n Q_n \tag{5}$$

where Z and L are the width and the length of the channel, μ_n is the electron mobility. Finally :

$$\frac{dg}{dt} = -\frac{Z}{L}\mu_n \frac{dQ_n}{dt} \tag{6}$$

$$\frac{dg}{dt} = \frac{Z}{L}\mu_n I_E \tag{7}$$

or :

$$I_E = \frac{L}{Z} \times \frac{1}{\mu_n} \times \frac{dg}{dt} . \tag{8}$$

Thus, the total injected current can be readily deduced from channel conductance *versus* time measurements. We want to underline that this method takes into account all the injected charges, even those trapped in the insulator whereas those charges are omitted by classical gate current measurements.

3. **Experimental results.** — The experimental procedure is as follows :

The substrate voltage is set to the selected value and the gate is biased to its maximum voltage in the range of interest (corresponding approximately to $E_{ox} = 1.5 \times 10^6$ V/cm).

Then, the light beam being kept off by a mechanical shutter, the gate probe is lifted and the $Y(t)$ recorded turned on (a typical starting point was $g = 2 \times 10^{-4}\ \Omega^{-1}$); next, the light beam is switched on and the channel conductance decrease *versus* time is recorded down to $g < 1 \times 10^{-5}\ \Omega^{-1}$ (Fig. 4).

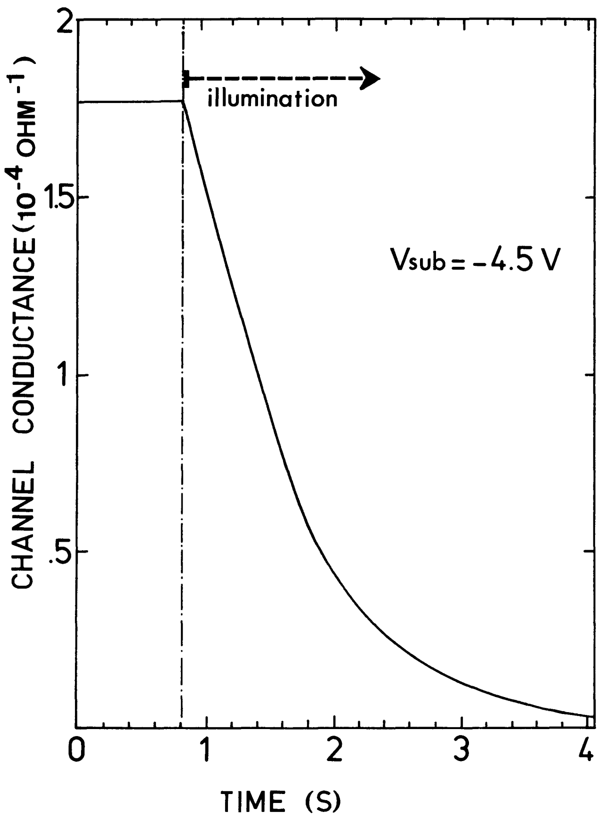

FIG. 4. — Typical channel conductance shift as a function of time during optically induced hot electron injection.

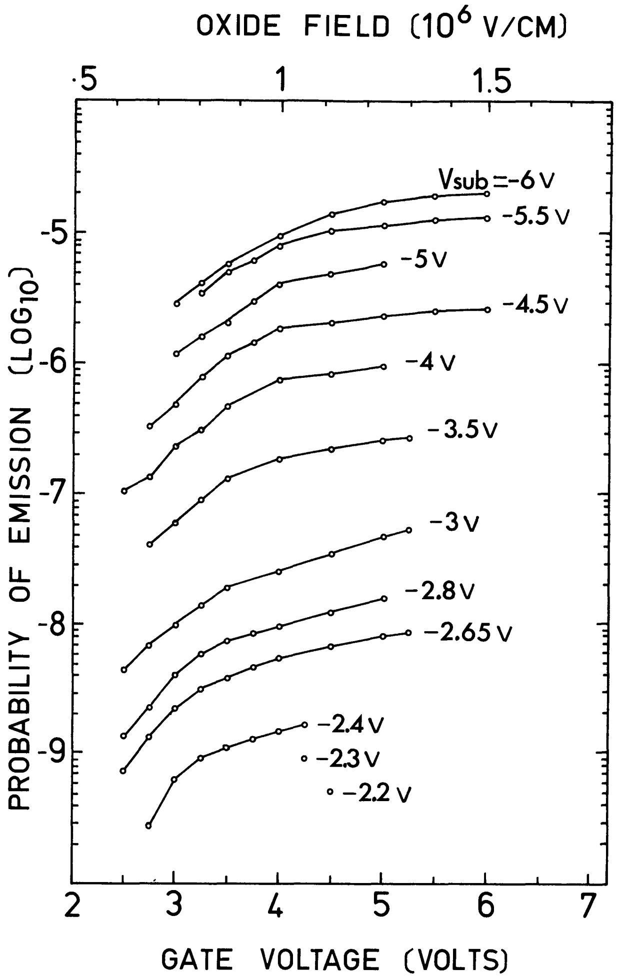

FIG. 5. — Measured emission probabilities as a function of gate voltage with substrate voltage as a parameter.

All the experiments were made at room temperature (300 K) for substrate voltages ranging from 1.8 V to 6 V, corresponding to usual operating voltages of highly-doped M.O.S. devices. The primary photocurrent was about 1×10^{-6} A.

The channel conductance is related to the oxide field E_{ox} so that, from a single record, we can calculate the emitted current as a function of E_{ox}, for a given V_{sub}. This is made by reference to a preliminary plot of conductance *versus* oxide field with V_{sub} as a parameter which is used also to correct equation (8) for eventual mobility variations.

Figure 5 is the resulting plot of the emission probability P as a function of the oxide field E_{ox} (or gate voltage V_G), with V_{sub} as a parameter. We define a probability threshold $P_T = 5 \times 10^{-10}$, under which we may not assert that the calculated currents were indeed due to hot-electron emission. More accurate measurements would need larger devices for which the ratio of the emitted current to the surface leakage current would be increased.

Above this threshold, we begin to find significant emission probabilities when the total potential drop across the depletion layer becomes greater than the estimated barrier energy, i.e. for $V_{sub} > 2$ V. We notice also that, for a given V_{sub}, the probability increases by nearly an order of magnitude when E_{ox} varies between 0.6×10^6 V/cm and 1.5×10^6 V/cm.

4. **Analysis of experimental results and discussion.** — The works of Ning *et al.* [1, 2] have shown that the original Shockley's *lucky electron* model could be adapted to the hot electron emission phenomenon and fitted the experimental data very well. Let us sum up the main assumptions from which this model is derived :

(i) Assuming a suitable electric field at the Si-SiO_2 interface, an electron can be emitted if it reaches this interface with an energy higher than the Schottky lowered Si-SiO_2 interface barrier, i.e. :

$$\Phi_B = 3.1 \text{ eV} - \beta E_{ox}^{1/2}$$

where 3.1 eV is the Si-SiO_2 interface barrier for electrons when the electric field is very small and

$$\beta = 2.6 \times 10^{-4}\ \mathrm{e}\ (\mathrm{Vcm})^{1/2}$$

for SiO_2 [6].

(ii) To gain this energy, the electron may be lucky enough to fall through a potential drop equal to Φ_B without any collision with the lattice. This condition defines a distance d from the interface where the potential energy is equal to Φ_B :

$$qV(d) = \Phi_B \qquad \text{(Fig. 3)}.$$

(iii) The emission probability of an electron which has a collision within the distance d is negligible.

With these assumptions, the emission probability is written in the form :

$$P = P_0 \exp(-d/\lambda)$$

where P_0 is a fitting parameter and λ is some equivalent mean free path for optical phonon electron collision. *Equivalent* means that λ is not the actual mean free path (denominated classically as L_R) but some phenomenological one resulting from assumptions (ii) and (iii).

In fact, the difficulty for explaining the dependence of P on V_{sub} and E_{ox} arises from the uncertainty when determining the distance d. Let us show it with a simple example :

— Assuming a constant doping level N_A, it can be easily derived from the depletion approximation :

$$\frac{\Delta d}{d} = -\frac{\Delta\lambda}{\lambda} = -\frac{1}{2}\frac{\Delta N_A}{N_A} \quad \text{(for a given } P/P_0)$$

or

$$\frac{\Delta[\mathrm{Ln}\,(P/P_0)]}{\mathrm{Ln}\,(P/P_0)} = -\frac{\Delta d}{d} = \frac{1}{2}\frac{\Delta N_A}{N_A} \quad \text{(for a given } \lambda).$$

Therefore, the relative accuracy of doping level measurements is reflected linearly on the mean free path value but exponentially on the probability value.

This was the actual problem to describe our experimental results because of the difficulty to measure doping profiles of S.O.S. devices. We used Buehler's method that we find suitable to thin film devices because it is static.

Using these data, the distance d is calculated as a function of V_{sub} and E_{ox} by integration of Poisson's equation. (The value of E_{ox} is used to correct the barrier energy for Schottky-effect lowering.)

In figure 6, the emission probabilities are plotted as a function of the distance d for several values of E_{ox}. It shows that the model describes the data very well for $E_{ox} > 0.8 \times 10^6$ V/cm, taking $P_0 = 0.5$ and $\lambda = 100$ Å.

For smaller values of E_{ox}, the discrepancies between the model and experimental data are important. Such departures have been already observed and can be explained by the scattering in the oxide [3]. For small field strengths, the distance to the potential maximum of the Schottky-lowered barrier is largest and therefore the scattering probability is increased.

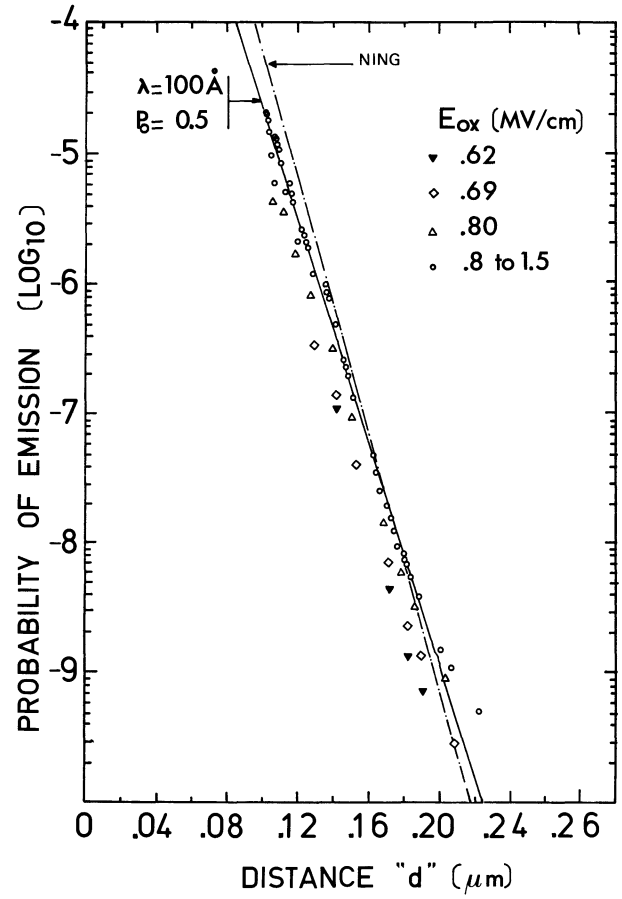

FIG. 6. — Measured emission probabilities as a function of d. The solid line corresponds to $P_0 = 0.5$ and $\lambda = 100$ Å, the broken line is Ning's results.

It is interesting to compare the value of λ we found to the value of L_R deduced from ionization rate measurements which is close to 70 Å [4]. The larger value of λ is probably due to the underestimation of P introduced by assumption (iii) : if (iii) vanishes (a more accurate modelling would show it), the emission probability will be greater than $\exp(-d/\lambda)$ and so, the resulting value of λ will be smaller. It explains our reservations when we call λ the *equivalent* mean free path for phonons interactions.

5. **Conclusion.** — In figure 6, we have reported the Ning's results on bulk silicon (at 300 K, he found $P_0 = 2.9$ and $\lambda = 91$ Å). The two results are nearly identical and it proves that :

(i) The high field properties of S.O.S. appear to be the same as those of bulk silicon in spite of lattice defects.

(ii) The emission probability can now be predicted accurately using the *lucky-electron* model, when the electric field is perpendicular to the Si-SiO_2 interface.

The modelling of emission should be useful :

(i) For evaluating the dependence of threshold instabilities on stress conditions (currents, operating voltages) when scaling down the S.O.S.-M.O.S. devices ;

(ii) For reducing writing energy of S.O.S. non-volatile memory devices which use hot-electron injection [7].

In a quantitative manner, our results show that N.V.M. writing can be achieved with small voltage level. For example, with $P = 1 \times 10^{-5}$ corresponding to $V_{\mathrm{sub}} = 5$ V, we can estimate the writing energy to be about 1 μJ/bit (see [4] for calculation details). On the other hand, these same results emphasize the sensitivity of threshold instabilities to the operating voltage since the emission probability can vary of several orders of magnitude for a 2 or 3 V variation of V_{sub}.

It can be pointed out that accurate doping profile measurements are the key to describe the dependence of the emission process on technological and electrical parameters. Reciprocally, a perfect technological mastery over doping profiles will be essential to achieve optimum performances of N.V.M. devices and to insure the reliability of VLSI devices.

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