A model of the leakage current in n-channel silicon-on-sapphire most's

P. Gentil

A MODEL OF THE LEAKAGE CURRENT IN n-CHANNEL SILICON-ON-SAPPHIRE MOST'S

P. GENTIL

Equipe Physique des composants à semiconducteurs (*),
E.N.S.E.R. Grenoble, 23, avenue des Martyrs, 38031 Grenoble Cedex, France

Résumé. — On montre expérimentalement qu'il existe, sur les transistors MOS à canal n sur silicium sur isolant, un courant de fuite direct entre drain et source. On montre que le courant drain varie avec la polarisation du drain et de la couche de silicium comme le courant d'un canal à l'interface silicium saphir travaillant en régime d'inversion faible. Les mesures statiques $I(V)$ permettent de déterminer une densité d'états à l'interface silicium-saphir de 10^{12} cm^{-2} eV^{-1}.

Abstract. — The existence of a direct drain to source leakage current is experimentally demonstrated on n-channel SOS MOS transistors. The measured currents are shown to vary according to a model of an inversion channel at the sapphire interface working in the weak inversion regime. A value of interface state density at the silicon sapphire interface of 10^{12} cm^{-2} eV^{-1} is determined by static $I(V)$ measurement.

1. **Introduction.** — Anomalous high value of the leakage current has been reported by several authors [1-5] in n-channel Silicon-On-Sapphire (S.O.S.) M.O.S. transistors. This leakage current was described in terms of currents in the reverse-biased junctions of the MOST. Higher value of leakage current in n-channel SOS MOST was explained by the fact that the drain depletion layer would speed laterally toward the source region due to the presence of a high density of donorlike states in the silicon at the Al_2O_3-Si interface. In P-channel SOSMOST, the presence of the same donors would reduce the depletion layer near the sapphire interface resulting in a smaller leakage current. Also, it was mentionned [2, 4] that an inversion layer may exist at the Al_2O_3-Si interface but without experimental evidence and without model for the corresponding leakage current.

In this paper, the existence of such a leakage current is demonstrated and we show that it is predominant in an important fraction of the tested wafers. Experimental results of the variations of the drain leakage current as a function of the drain bias V_{DS} and as a function of the silicon layer bias V_{BS} (with respect to the source) are presented on n-channel S.O.S. M.O.S.T. when the top silicon surface is turned off. For devices built on a silicon layer doped with a uniform boron doping of about 10^{16} cm^{-3} and exhibiting normal value of the leakage current (about 10^{-9} A), the drain to source leakage current is shown to vary according to the weak inversion theory of a MOST. From static measurement of the leakage current and the weak inversion channel theory, a value of the density of the surface states at the sapphire interface is easily determined.

2. **Model.** — In this section, we present a model of a parasitic conduction of the n-channel SOSMOS transistor based on a n-type inversion channel at the sapphire interface (Fig. 1). We suppose that the inversion channel is only induced by an intrinsic Al_2O_3-Si interfacial charge, Q_{sap}. The sapphire is very thick so that the inversion channel is not controlled by any insulated gate as in a normal MOST (consequently, the effect of the difference in work functions between silicon and a metal gate is neglected). Furthermore, we suppose that a neutral silicon region exists above the depleted layer of the Al_2O_3-Si interface. Thus, it can be written :

$$Q_{sap} + Q_{ss} + Q_n + Q_B = 0 \qquad (1)$$

where Q_n is the charge per unit area of the parasitic inversion channel, Q_B the charge of the depleted

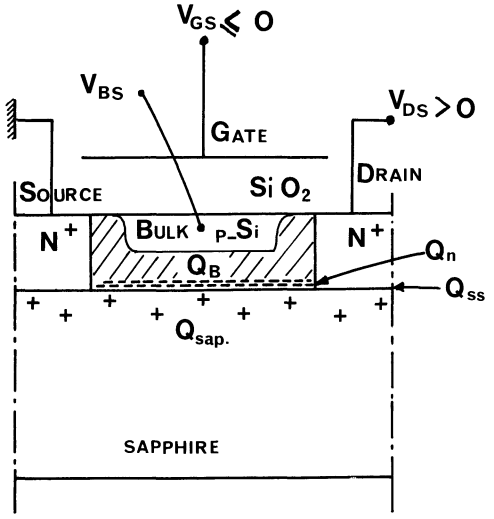


FIG. 1. — Cross-section of a n-channel SOSMOS transistor.

(*) E.R.A. C.N.R.S. nº 659.

layer and Q_{ss} is the varying charge in the surface states at the Al_2O_3-Si interface.

Establishment of the formulation giving the drain to source current at the sapphire interface follows the calculation procedure used in references [6, 7]. In this paper, we consider a bias V_{BS} of the electrical substrate (that is to say the neutral silicon layer bias) with respect to the source. The control of the substrate bias must allow to vary Q_B, Q_n, Q_{ss}.

The charge Q_n, available for the leakage current, is obtained by integrating Poisson's equation in the silicon (near the sapphire surface). Using a first order series expansion, Q_n is found :

$$Q_n = -\frac{1}{2}\left(\frac{2\,N_A\,\varepsilon_{si}\,kT}{\beta\varphi_s - 1}\right)^{1/2} \times \times \exp[\beta(\varphi_s - \varphi_c - 2\,\varphi_F)]\,, \quad (2)$$

where : N_A is the doping of the silicon layer, ε_{si} the permittivity of the semiconductor, k the Boltzman's constant, T the absolute temperature, $\beta = q/kT$ with q the electronic charge, φ_s the surface potential, φ_F the potential difference between the midgap and the bulk Fermi level, and φ_c the difference between the electron quasi-Fermi level and the bulk Fermi level. φ_s, φ_F, φ_c are positive in the normal operation of the n-channel. The charge in the depletion region Q_B is given by :

$$Q_B = -(2\,N_A\,\varepsilon_{si}\,kT)^{1/2}\,(\beta\varphi_s - 1)^{1/2}\,. \quad (3)$$

A good approximation for the φ_s value is obtained by using (1), and by expanding Q_B in a first order series around $\varphi_s = \frac{3}{2}\,\varphi_F - V_{BS}$:

$$\varphi_s = \frac{3}{2}\,\varphi_F - V_{BS} + V + \frac{Q_{B_0} + Q_{sap} - C_{D_0}\,V}{C_{D_0} + qN_{ss}}\,; \quad (4)$$

where : V is the part of φ_c originating from the drain to source V_{DS} bias, N_{ss} the surface state density per-unit area and unit energy, Q_{B_0} the value of Q_B for $\varphi_s = \frac{3}{2}\,\varphi_F - V_{BS}$ and C_D the depletion capacitance per unit area ;

$$C_{D0} = C_{D(\varphi_s = \frac{3}{2}\varphi_F - V_{BS})} = \left[\frac{qN_A\,\varepsilon_{si}}{2\left(\frac{3}{2}\,\varphi_F - V_{BS} - \frac{kT}{q}\right)}\right]^{1/2}. \quad (5)$$

The leakage current is given by :

$$I_L = \frac{W}{L}\,\mu_n \int_{source}^{Drain} Q_n(\varphi_c)\,d\varphi_c \quad (6)$$

where : W and L are the width and the length of the channel respectively, and μ_n the mean mobility of the channel electrons.

Inserting (2) in (6), using (4) and considering small values of V_{BS} (compared to $\frac{3}{2}\,\varphi_F$), we obtain

$$I_L = \frac{W}{L}\,\mu_n\,C_D^*\left(\frac{kT}{q}\right)^2 \frac{C_D^* + qN_{ss}}{C_D^*} \times \times \exp\left[\beta\left(-\frac{\varphi_F}{2} + \frac{Q_{sap} + Q_B^*}{C_D^* + qN_{ss}}\right)\right] \times \exp\left[\beta\,\frac{C_D^*\,V_{BS}}{C_D^* + qN_{ss}}\right]\left[1 - \exp\left(-\beta\,\frac{C_D^*\,V_{DS}}{C_D^* + qN_{ss}}\right)\right] \quad (7)$$

where, as in [6]. Q_B^* and C_D^* are the values of Q_B and C_D respectively, for $\varphi_s = \frac{3}{2}\,\varphi_F$.

It can be noted :

1) Device geometry only affects I_L by the W/L ratio.

2) I_L increases exponentially with the sapphire charge Q_{sap}.

3) I_L is influenced in a complicated way by the silicon doping N_A : Q_B^* and C_D^* vary with N_A.

4) An exponential relation exists between I_L and V_{DS} as in a MOS transistor working in the weak inversion regime.

5) I_L decreases exponentially when the reverse bias $|\,V_{BS}\,|$ applied to the silicon layer increases (V_{BS} is negative). This behaviour is opposed to the one of the leakage current of a reverse-biased junction.

6) The same constant exists in the exponential factors containing V_{BS} and V_{DS}. Both variations of I_L *versus* V_{BS} and of I_L *versus* V_{DS} allow to calculate the sapphire interface state density N_{ss}.

3. **Experimental results. Discussion.** — 3.1 General observations. — n-channel enhancement mode MOS transistors were fabricated by LETI (Grenoble) on a silicon film doped by boron implantation. Sapphire substrates originate from Union Carbide. Devices were processed with wet gate oxide (1 000 °C) and annealed in nitrogen.

Measurement of the leakage current was carried out on many wafers. As was reported in earlier publications, I_L varies from wafer to wafer by several orders of magnitude but variation in I_L from device to device on a given wafer is typically less than a factor of 2. Also, comparison of the leakage current for circular and rectangular devices shows that the edge leakage current is a negligible fraction of the total leakage current.

Devices with silicon layer doping ranges from 5×10^{14} cm^{-3} to 2×10^{17} cm^{-3} were measured but no conclusion can be made on the influence of the layer doping without the use of different doping on the same wafer. However, as mentioned in [2], we have obtained the lowest values of the leakage current on a wafer which was implanted with an additional concentration of boron atoms

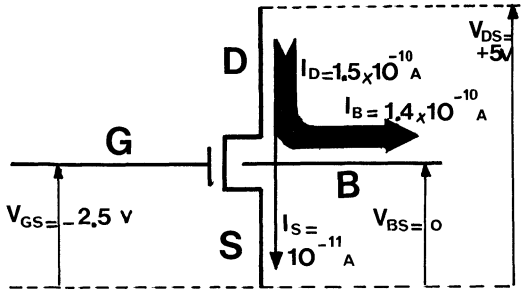
$$(2 \times 10^{17}\ \text{cm}^{-3})$$

near the Al_2O_3-Silicon interface. In that case, leakage currents have the same order of magnitude as those of the p-channel SOS transistors.

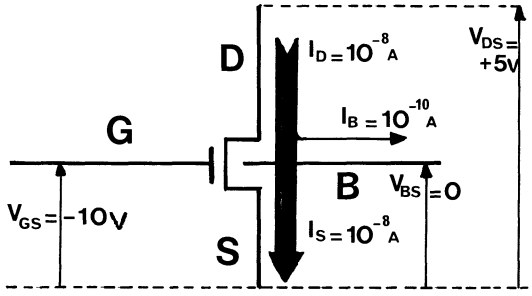
3.2 NATURE OF THE CURRENT. — Owing to the P-silicon layer contact (also called bulk), we can compare the magnitude of the drain current, source current and bulk current in the SOS MOS transistors.

Figure 2A gives the different currents for a wafer exhibiting small values of the leakage current. In that case, most of the leakage current is due to the reverse-biased drain bulk junction current.

Figure 2B gives the same current components for a wafer exhibiting higher values of the drain leakage current. It is evident here that most of the leakage current is due to a direct drain to source leakage current.



2.A



2.B

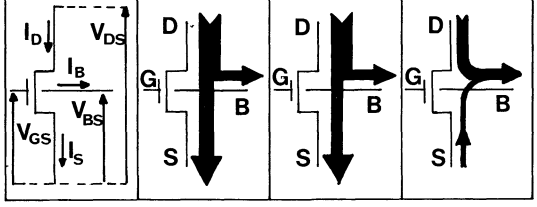
FIG. 2. — Leakage currents in a n-channel SOSMOS transistor. 2A – $N_A \sim 10^{17}$ cm^{-3} implanted at 2×10^{17} cm^{-3} near the Al_2O_3 surface; $X_{si} = 0.8$ µm; $W = 100$ µm; $L = 100$ µm. 2B – $N_A \sim 10^{15}$ cm^{-3}; $X_{si} = 0.7$ µm; $W = 100$ µm; $L = 50$ µm.

Results obtained on a wafer giving intermediate values of the drain leakage current are reported on table I. The two first cases of biasing conditions ($V_{BS} = 0$) show that the drain leakage current is the sum of an important drain to source component and a reverse-biased drain-bulk junction leakage component. The last case of biasing condition ($V_{BS} = -0.2$ V) shows that by applying a small V_{BS}, the direct drain to source current is considerable decreased as predicted by equation (7) while the bulk current, including drain-bulk and source-bulk leakage current, is slightly increased.

In the following, emphasis is given to devices built on a silicon layer doped with a uniform doping of boron of about 10^{16} cm^{-3} which is a normal value for

TABLE I

Leakage currents in a n-*channel* SOSMOST *with the top silicon surface cut-off.* $N_A = 10^{16}$ cm^{-3}; $X_{si} = 0.8$ µm; $W = 100$ µm; $L = 100$ µm.

V_{DS} (V)	+0.5	+5	+5
V_{BS} (V)	0	0	-0.2
I_D (nA)	+2.1	+2.3	+1
I_S (nA)	+1.3	+1.3	-0.2
I_B (nA)	+0.8	+1	+1.2
			

integrated circuit necessity. Also, measurements reported are those of wafers giving a mean value of the leakage current (about 10^{-9} A with

$$W = L = 100\ \mu).$$

3.3 EFFECTS OF THE WIDTH AND LENGTH OF THE CHANNEL. — Table II gives the leakage currents for various width and length of the channel. 2A and 2B are measured on two different wafers. On these wafers, the leakage current is mainly due to a direct

TABLE II

Drain leakage current in a n-*channel* SOSMOST *as a function of the transistor geometry.* $V_{DS} = +5$ V; $V_{BS} = 0$. 2A – $N_A = 2 \times 10^{16}$ cm^{-3}; $X_{si} = 0.8$ µm; W/L is constant. 2B – $N_A = 10^{16}$ cm^{-3}; $X_{si} = 0.8$ µm; W is constant.

W (µm)	100	40	20	16
L (µm)	50	20	10	8
I_L (nA)	15	17	15	18

2.A

W (µm)	100	100	100
L (µm)	100	10	5
I_L (nA)	2.4	28	60

2.B

drain-to-source current. From figure 2A, this leakage current is seen to be constant when the width W and the length L vary so that the W/L ratio is keeped constant. From figure 2B, on devices having a constant width, it is seen that the leakage current varies approximately like the W/L ratio. Device geometry acts as predicted by equation (7) on SOS MOST exhibiting direct drain to source leakage.

It can be noted that the usual parameter giving the leakage current per 10 μm (or per mil) of width of channel is not adequate to characterize devices exhibiting direct drain-to-source leakage current.

3.4 DRAIN CURRENT CHARACTERISTIC. — Figure 3 gives the drain current vs the drain voltage with the bulk to source bias voltage as parameter. Such a

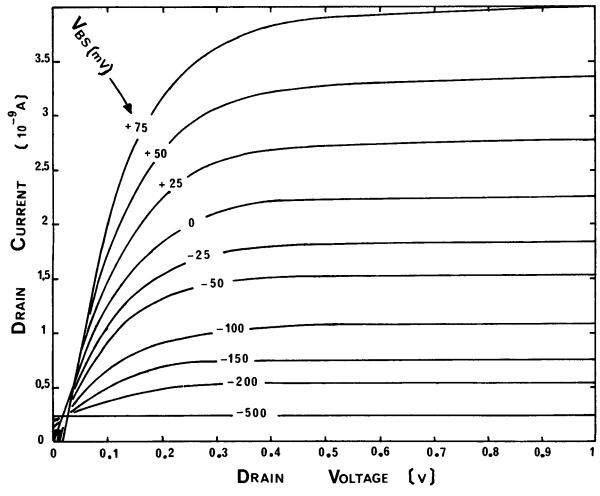


FIG. 3. — Drain current *vs* drain voltage with the bulk-to-source bias voltage as parameter. $N_A = 6 \times 10^{16}$ cm^{-3}; $X_{si} = 0.8$ μm; $W = 100$ μm; $L = 120$ μm.

variation as a function of V_{DS} can be described by equation (7). It can be noted that the $I_{DS}(V_{DS})$ curves do not pass by the point $I_{DS} = 0$, $V_{DS} = 0$ when the bulk is not connected to the source. This is due to the leakage current of the drain-bulk junction which is not completely negligible. As was mentionned previously the direct drain to source leakage current strongly depends on the bulk bias V_{BS}. This dependance is better seen from figure 4 which gives the drain leakage current vs the bulk voltage with the drain voltage as parameter for small values of biasing. At the right of figure 4, for positive biases of the bulk, the drain current decreases because of the direct bias of the drain bulk junction.

At the left part of figure 4, for negative biases of the bulk, all the curves tend toward the same limit which corresponds to the leakage of the reverse biased drain to bulk junction as it is shown by the curve $I_{DS}(V_{BS})$ with $V_{DS} = 0$. The direct drain to source leakage current (obtained by substracting the drain current under $V_{DS} = 0$ from the drain current under $V_{DS} \neq 0$)

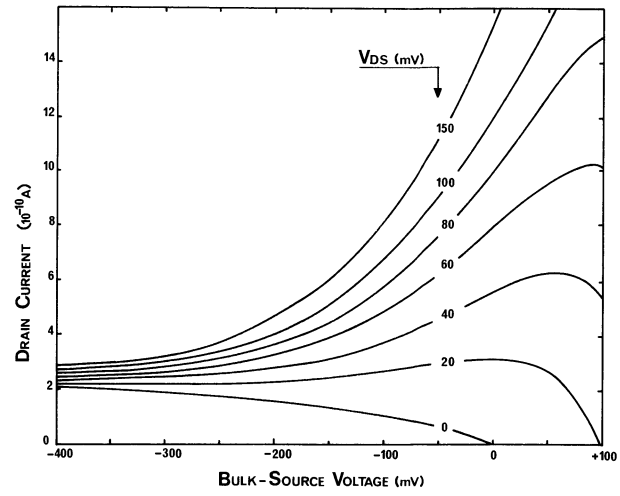


FIG. 4. — Drain current *vs* bulk to source bias voltage with the drain voltage as parameter. Same device as in figure 3.

is plotted in semilogarithmic scales on figure 5. The straight lines thus obtained are in good agreement with equation (7). From the slope of these curves and equation 7, we obtain a N_{ss} of 1.1×10^{12} cm^{-2} V^{-1}. A value of $N_{ss} = 9.1 \times 10^{11}$ cm^{-2} V^{-1} can be obtained from $I_{DS}(V_{DS})$ with $V_{BS} = 0$ (as described in [6]).

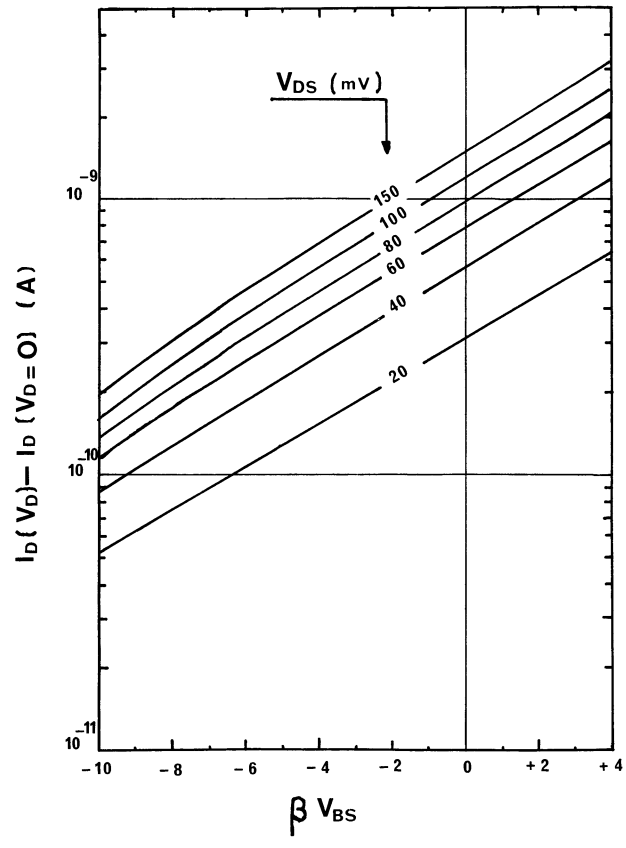


FIG. 5. — Drain to source current *vs* bulk to source bias voltage with the drain voltage as parameter. Curves are calculated from figure 4.

Measurements carried out on various wafers have given surface state densities at the silicon sapphire interface ranges from $5 \times 10^{11}\ cm^{-2}\ V^{-1}$ to $2 \times 10^{12}\ cm^{-2}\ V^{-1}$. These values are consistent with the ones obtained by the $C(V)$ characteristic of the back Metal-Sapphire-Silicon capacitance [8] and other methods [9]. The high value of N_{ss} agrees with recombination properties of the silicon film at the sapphire interface [10].

4. **Conclusion.** — We have shown that an important fraction of the n-channel (enhancement type) MOS transistors built on a SOS substrate exhibits an anomalous high value of drain leakage current which corresponds to a direct conduction between source and drain. Experimental results agrees with a model of a parasitic inversion channel at the sapphire interface working in the weak inversion regime. The values of N_{ss}, determined from the $I(V)$ characteristics agree with the ones obtained by the back $C(V)$ characteristics. However, the method proposed here is more easy to carry out.

It may be argued that the direct drain to source leakage current may originate from a high concentration of donor impurities at the sapphire interface which would give a n-type silicon resistive channel. However such a channel would behave as a JFET when biasing the P type silicon layer. We tried to make the comparison but we did not meet a profile of the donor impurities which fits with $I_D(V_{DS})$.

From equation (7), it is theoretically possible to calculate the electron mobility at the sapphire interface if the value of Q_{si} is known. Q_{si} could be obtained from a back $C(V)$; however, because of the strong dependance of the Q_{si} on the leakage current, the leakage current and Q_{si} must be measured precisely on the same wafer which was not carried out here.

Acknowledgment. — The author wishes to thank searchers of the LETI Grenoble for supplying devices and for numerous helpful discussions.

References

[1] HAM, W. E., IEDM (1973), abstract 8.7.
[2] MCGREIVY, D. J., *IEEE Trans. Electron Devices* **ED 24** (1977) 730.
[3] PREUSS, E. and SCHLOTTERER, H., *Solid State Devices*, Conf. series 40 (The Institute of Physics, Bristol and London) 1977, p. 7.
[4] HARARI, E. and MCGREIVY, D. J., *IEEE Trans. Electron Devices* **ED 24** (1977) 1277.
[5] CHOUJAA, A., Thèse de Docteur Ingénieur, Grenoble (1977).
[6] VAN OVERSTRAETEN, R. J., DECLERCK, G. J., MULS, P. A., *IEEE Trans. Electron Devices* **ED 22** (1975) 282.
[7] LORA TAMAYO, E., MERCKEL, G., GAUTIER, J., Note Technique LETI/MEA Grenoble, n° 1160 (1976).
[8] GOODMAM, A. M. and WEITZEL, C., *IEEE Trans. Electron Devices* **ED 24** (1977) 215.
[9] GENTIL, P. and CHAUSSE, S., *Solid-State Electron.* **20** (1977) 935.
[10] CRISTOLOVEANU, S., CHOVET, A. and KAMARINOS, G., *Solid-State Electron.* **21** (1978) under press.