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DYNAMIC SELF-BIASING OF THE FLOATING SUBSTRATE
OF THE SOS TRANSISTOR

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Abstract. — Under dynamic operation the grounded source diode of the SOS transistor creates a reverse bias on the floating substrate. Numerical simulations agree well with the directly measured increase of this bias as a function of doping and frequency. The reverse self-bias increases the threshold voltage on heavily doped samples. This leads to a reduction of the weak inversion leakage current and gives rise to the minimum of the current-vs-frequency curve observed on SOS circuits. An anomalously strong temperature dependence of the frequency of a ring oscillator operated at low voltage is attributed to the effect of dynamic self-biasing.

1. Introduction. — The SOS IGFET is characterized by the absence of a direct contact to the silicon region below the channel. This configuration, named floating substrate, gives rise to differences in the electrical behaviour as compared to that of a conventional IGFET:

1) In saturation the substrate current, caused by carrier multiplication in the pinch-off region, creates a forward bias on the source junction. The corresponding decrease of the threshold voltage gives rise to the first kink [1, 2].

2) A reduced source-to-drain break-down voltage is observed [3].

3) The subthreshold transconductance is found to be smaller on SOS MOSTs than on corresponding bulk devices due to a clamping of the electrical potential at the Si/sapphire interface [4]. For the ideal SOS MOST, however, the contrary is theoretically found [5].

4) A frequency-dependent transient of the drain current has been reported [6].

In this paper we present a study of another floating-substrate effect, namely the appearance of a reverse substrate bias under dynamic operation.

2. Substrate bias under dynamic operation. —

2.1 Basic Considerations. — In order to determine the potential of the floating substrate under dynamic operation, we consider the equivalent network of the SOS MOST, shown in figure 1 for the source region.

The MOST is assumed to be in the blocked state or in weak inversion, i.e. there is no capacitive shielding by the channel. The drain electrode is connected to ground in our initial considerations. The capacitances of the fast interface states (near the gate oxide and near the sapphire) may be included in C_{BS}. The resistor parallel to the diode represents the diode leakage current.

We consider in a first approximation the gate capacitance with the source diode in series only, assuming a periodic signal \( V = V_0 (\sin \omega t + 1) \) applied to the gate. Dynamic self-biasing will occur if the diode leakage current \( I_0 \) (of source and drain) is too small to discharge the gate capacitance within a risetime \( \tau = 1/2 \pi f \) such that:

\[
I_0 < V_0 C_{GB}/\tau = 2 \pi f V_0 C_{GB} \quad (1)
\]

which transforms to

\[
f > f_c = I_0/2 \pi V_0 C_{GB} \quad (2)
\]
For a typical SOS MOST

\( W = L = 6 \mu m \), \( t_{ox} = 0.1 \mu m \),

\( I_0 = 1 nA \), \( V_0 = 5 V \), \( C_{GB} \approx C_{ox} \)

\( f_c \approx 3 kHz \). As SOS circuits normally operate in the MHz range, they quite naturally will be subjected to dynamic self-biasing since \( f \gg f_c \).

2.2 Measurements. — Direct measurements of the substrate bias were performed by using a small p-ch MOST \( W = L = 4 \mu m \) as a voltage follower whose gate was connected to the substrate contact of the large n-ch MOST \( W = L = 80 \mu m \) used as test vehicle and shown in figure 2. On-chip bonding was used to connect the two transistors in order to reduce parasitic capacitances. The d.c. level of the output was adjusted on the oscilloscope before each measurement by applying the input signal directly to the gate of the follower. The frequency response was about 100 kHz. For the large n-ch MOST, \( f_c \approx 200 Hz \).

Fig. 2. — Experimental set up. A small p-ch MOST \( T_2 \) is used as a voltage follower for the substrate bias of a large n-ch MOST \( T_1 \).

2.3 Results. — A typical set of curves is shown in figure 3 for a heavily doped MOST. The horizontal time scale has been adjusted for the same length of a period on the picture. The upper trace shows the input signal in order to determine the phase of the substrate bias. It is seen that the negative substrate bias is very pronounced in the blocked state of the MOST, but disappears in the conducting state.

Figure 4 shows the influence of a voltage applied to the drain. The amplitude of the negative substrate bias is slightly reduced and the positive bias related to the multiplication-induced substrate current [1, 2] appears in the on-state of the transistor. At higher frequencies this reduction of the negative substrate bias is found to be more pronounced.

Fig. 4. — Substrate bias \( V_B \) (lower trace 0.5 V/div) induced by a 1 kHz gate signal (upper trace 1 V/div.) \( V_B \) (peak to peak) increases with \( V_D = 0, 5, 10 V \), \( N \approx 1.4 \times 10^{16} \text{ cm}^{-3} \), \( V_T = 1.8 V \).

2.4 Analysis. — We have obtained numerical solutions for the dynamic self-biasing voltage by simulating the equivalent network of figure 1 and taking into account the grounded drain diode. Voltage-dependent gate-to-substrate and substrate-to-source capacitances, obtained from high-frequency \( C(V) \) measurements on the same device and experimentally determined diode characteristics, were used for the calculations. The theoretical curves are compared with experimental points taken from measurements of the type in figure 3. Figure 5a shows a case of low doping in the frequency range 1-20 kHz and figure 5b a case of high doping in the range of 100 Hz-10 kHz. The agreement is good as regards the general shape and amplitude of the induced substrate bias. The difference between the results of figure 5a and 5b is due to the different threshold voltages, since \( C_{GB} \) drops to zero at the onset of inversion (shielding by the channel for \( V > V_T \)).

2.5 Reverse bias in the on-state of the transistor. — At high frequencies, the reverse substrate bias is observed on some samples to persist into the on-state of the transistor, as shown in figure 6. This behaviour cannot be explained with our model. It can probably be attributed to charging of the fast interface states near the sapphire or to second order effects that are not described by our model.
3. Influence of the substrate bias on the threshold voltage of the SOS transistor. — The existence of the substrate bias by itself does not necessarily change the performance of an SOS circuit unless a MOST parameter is changed.

3.1 Maximum threshold voltage of the SOS MOST. — The threshold voltage of a MOS transistor on bulk silicon is increased by a reverse substrate bias according to [7]

\[
V_T = V_{FB} + 2 \varphi_B + [2N_B |q| \varepsilon_0 \varepsilon_s (2 \varphi_B - V_B)]^{1/2} / C_{ox} .
\]

where \(V_{FB}\) is the flatband voltage, \(\varphi_B\) the Fermi level in the silicon, \(N_B\) the doping of the silicon, \(q\) the elementary charge, \(\varepsilon_0 \varepsilon_s\) the dielectric constant of silicon, \(V_B\) the substrate bias voltage, \(C_{ox}\) the gate-oxide capacitance.

This increase is caused by the fact that the maximum depletion-layer width \(x_{dmax}\) is growing under the influence of the reverse bias:

\[
x_{dmax} = [2 \varepsilon_0 \varepsilon_s (2 \varphi_B - V_B) / qN_B]^{1/2} .
\]

In the case of SOS, the depletion-layer width cannot exceed the silicon film thickness \(t_{Si}\), leading to an upper limit of the threshold voltage:

\[
V_T \leq V_{FB} + 2 \varphi_B + N_B q t_{Si} / C_{ox} .
\]

3.2 Measurements of \(V_T(V_B)\). — Measurements of the threshold voltage as a function of the substrate bias were performed on SOS transistors with different doping levels and film thicknesses by imposing a constant potential to the lateral substrate contact of a SOS MOST. The threshold voltage was determined from the linear region \(V_D = 50 \text{ mV}\) by extrapolating the \(I_D(V_G)\) curve. The results are shown in figure 7 for transistors with different doping levels, gate-oxide thicknesses and epi layer thicknesses. It is seen that no change of \(V_T\) takes place at the lowest doping levels and that saturation occurs even for the highest doping. The increase of the threshold voltage with reverse substrate bias is most pronounced in the case of a very thick gate oxide (sample \(d\)). Much smaller
changes of $V_T$ as a function of $V_B$ are observed if the threshold voltage is determined from the saturation current of the MOST. This is due to the fact that the multiplication-induced substrate current partially offsets the externally applied substrate bias.

3.3 Influence of fast interface states at the Si/Sapphire interface. --- Upon onset of total depletion of the silicon film, the substrate contact becomes ineffective because of the extremely high resistivity of the depleted region. Thus the substrate bias cannot be further increased, inhibiting a determination of the charges that might build up in the fast interface states at the Si/sapphire interface under the influence of the substrate bias. Under dynamic operation, charges of this kind could lead to an even further increase of the threshold voltage.

4. Implications of dynamic self-biasing on SOS circuit performance. --- 4.1 Minimum of the current-versus-frequency curve. --- At very low frequencies, the current consumption of a SOS circuit is determined only by the static leakage current $I_{stat}$. There are two components to this current: the reverse current of the drain junction $I_r$ and the weak-inversion (subthreshold) channel current $I_{th}$ [4, 8]. The latter is given by:

$$I_{th} = I_0 \exp(-qV_T/nkT)$$  \hspace{1cm} (6)

where $I_0$ depends on the MOST parameters, the temperature and the drain voltage; $V_T$ is the threshold voltage, $k$ Boltzmann's constant, $T$ the absolute temperature and $n$ the parameter of the subthreshold slope of the MOST.

At high frequencies, the current consumption of a circuit is dominated by the dynamic current which is given by:

$$I_{dyn} = f.C_{eq}.V$$  \hspace{1cm} (7)

where $C_{eq}$ is the equivalent capacitance of the circuit. The total power consumption $I = I_{stat} + I_{dyn}$ should thus be a monotonic function of the frequency.

However the experimental curves of figure 8 for a static inverter and a dynamic binary counter, both fabricated on highly doped silicon films, exhibit pronounced minima. This can be understood by the fact, that the threshold voltage in the blocked state increases as a function of frequency due to dynamic self-biasing of the floating substrate (Fig. 7). The static subthreshold current given by (6), thus will decrease with increasing frequency, giving rise to the current minimum. Dynamic circuits, due to their floating nodes and since the subthreshold current depends exponentially on $V_T$, exhibit the current minimum even in the case of low doping.

4.2 Influence on the upper frequency limit of a SOS circuit. --- It is important to know whether the speed of a SOS circuit is reduced by the dynamic self-biasing. In a circuit, not only the gate signal, but also the drain signal — via the capacitance of the drain junction — will induce a reverse bias of the floating substrate. Being in opposite phase with the drain current, it will directly affect the conducting state of the MOST. Such a mechanism has been briefly discussed in references [1] and [10]. For this reason we have performed a study of a 9-stage ring oscillator integrated on our samples.

Burns [9] has shown that for $|V_{th}| + |V_{th}| < V_{DD}$ and $\beta_p/\beta_n > 0.2$ the stage delay of a CMOS inverter is equal to

$$t_{ds} = 0.9 \cdot \frac{C_L \cdot V_{DD}}{-T}$$  \hspace{1cm} (8)

where $T$ is defined by

$$T = (T_n^{-1} + T_p^{-1})$$  \hspace{1cm} (9)

$I_n$ and $I_p$ are the drain currents obtained for $V_G = V_D$. $C_L$ is the load capacitance. It can be determined from the current consumption:

$$I_{osc} = 9 \cdot C_L \cdot f \cdot V_{DD}$$  \hspace{1cm} (10)

The theoretical oscillation frequency of the 9-stage ring oscillator is given by:

$$f_{th} = \frac{1}{9 t_{ds}} = \frac{1}{8.1 \cdot \frac{7}{V_{DD} \cdot C_L}}$$  \hspace{1cm} (11)

By using measured currents, of identical MOSTs as those of the oscillator, as values of $I_n$ and $I_p$, static floating-substrate effects are taken into account in a first approximation.

The ratio of the experimental frequency $f$ to the theoretical frequency $f_{th}$ is a measure of how much the speed is influenced by dynamic effects. At low temperatures and low operating voltages, the junction leakage currents are very small and dynamic self-biasing should thus be most pronounced, whereas at high temperatures and high drain voltages the increased leakage current is expected to counterbalance the negative substrate bias. Samples with

![Figure 8](https://example.com/f8.png)
low doping \((x_{\text{dmax}} > t_0)\) should have a ratio \(f/f_{\text{th}}\) which is independent of temperature and close to unity. Highly doped samples \((x_{\text{dmax}} < t_0)\) should exhibit a reduction of \(f/f_{\text{th}}\) towards low temperatures at low voltages.

In order to test this prediction we have measured the frequency of the ring oscillator between \(-60^\circ\text{C}\) and \(120^\circ\text{C}\) on samples with different doping levels. At the same time the temperature-dependent drain currents of the test transistors, identical to those of the oscillator \((L_n=L_p=6\ \mu\text{m}, W_n=22\ \mu\text{m}, W_p=22\ \mu\text{m})\) and located on the same chip, were measured with \(V_G=V_D\). In order to eliminate on-chip fluctuations, several samples were measured and those corresponding best to the average results were selected for the final analysis.

Each sample was measured at two voltages over the whole temperature range. These voltages were chosen such that the same two frequencies were obtained at \(120^\circ\text{C}\), namely 5.5 MHz (lower voltage) and 25 MHz (higher voltage). This procedure was chosen to insure that both oscillators were operated at about the same ratios of \(V/V_{Tn}\), since \(V_{Tn} > V_{Tp}\) on our samples.

The results presented in figure 9 show that for the undoped sample the ratio \(f/f_{\text{th}}\) is indeed independent of temperature and close to unity for both values of the drain voltage (2.0 V and 0.6 V respectively). On the strongly doped sample (n-ch only) no influence of temperature on \(f/f_{\text{th}}\) is observed at the higher drain voltage (6 V), but at low \(V_{DD}\) (3.5 V) a strong decrease of \(f/f_{\text{th}}\) occurs with decreasing temperature. We attribute this behaviour to the increasing effect of dynamic self-biasing towards lower temperatures. It is surprising to note that in this last case the average value of \(f/f_{\text{th}}\) still remains at about unity instead of being lower. This is probably due to the large difference between the drain currents of the n-ch and p-ch MOSTs at low voltage \((V_{Tp} \approx 1.2\ V, V_{Tn} \approx 2.2\ V)\).

For such an extreme case the numerical factor in Burns' equation (8) may have to be slightly modified.

5. Conclusions. — The existence of a dynamic reverse self-biasing of the SOS floating substrate has been demonstrated theoretically and experimentally. This bias is increasing with doping and frequency. For high doping levels \((x_{\text{dmax}} < t_0)\) the corresponding increase of the threshold voltage leads to a decrease of the static leakage current and to a reduction of the maximum operating frequency, if a circuit is operated at low voltages and low temperatures.

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