MODELLING OF H_{FE} AVALANCHE DEGRADATION IN GATE CONTROLLED BIPOLAR TRANSISTORS

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Résumé. — Modélisation de la dégradation par avalanche du gain H_{FE} d'un transistor bipolaire à grille de contrôle.

Le modèle du phénomène de dégradation par avalanche présenté ici prend en compte à la fois l'augmentation de la vitesse de recombinaison en surface localisée près du point intrinsèque dans la zone de transition surfacique de la jonction et le déplacement du point intrinsèque dû à la charge injectée dans l'oxyde.

On présente une méthode de détermination des paramètres du modèle. On donne les résultats de la modélisation pour une augmentation uniforme de la densité des états de surface et pour une distribution gaussienne. Ce modèle est utilisé pour améliorer la conception de points mémoires basés sur ce phénomène.

Abstract. — The avalanche degradation phenomenon model presented here takes into account both : an increase of surface recombination rate localized near the initial intrinsic point in the junction transition region surface and a displacement of the intrinsic point due to the oxide injected charge.

A method for the determination of parameters of the model is presented.

The modelling results are given for uniform surface state density increase and for an other distribution. This model is used to improve the design of memory cells devices using this phenomenon.

1. Introduction. — The reversible modification of bipolar gate controlled transistor current gain [1] can be used for the realization of an electrically reprogrammable memory. The project of such a memory using these devices was already presented at the 1976 ESSCIRC conference [2], [3].

The transposition of the obtained results upon discrete devices to the realization of an integrated memory has shown the complexity of the physical phenomenon which involves a modification of the surface recombination rate as well as hot carriers injection. These phenomena are complex, still poorly controlled and depend on the geometrical and technological parameters of the used devices.

The functional model of the emitter base junction avalanche degradation in bipolar gate controlled transistors permits to explain the phenomenon of H_{FE} degradation and restauration by controlling the gate bias during the avalanche. It also allows to draw conclusions for the application of this phenomenon to the realization of a REPRM, particularly upon the efficiency of the degradation-restauration and upon the aging problem on great numbers of programming cycles.

This study has been done in the frame work of the A.T.P.-C.N.R.S. M.I.S. *Nouvelles structures* with experimental devices realized by the Sescosem-Saint-Egrève.

Three kinds of devices have been studied (Fig. 1) :
— Discrete devices.

— Integrated devices with aluminium gate and polysilicon gate.

FIG. 1. — Geometries of studied devices.

2. Device characteristics and phenomena involved.

— The avalanche degradation phenomenon is mainly characterized by an increase of the I_B base current in the measured characteristic $I_B = f(V_{GM})$ with collector current I_C unchanging (Fig. 2) after a base emitter avalanche (V_{GA} gate bias applied, I_A avalanche current, t_A duration). Let us note that apart from ΔI_B peak, the base current keeps its initial value and that ΔI_B varies according to the injection level like $\exp \frac{qV_{BE}}{2kT}$, showing that the degradation is noticeable only for weak and average injection and that a recombination current increase occurs in the surface transition region.

FIG. 2. — Effect of an avalanche breakdown stress on the static curve $I_B(V_{GM})$ in forward bias conditions.

This current peak keeps the same amplitude and shape (Fig. 3), moves on the V_{GM} axis as a function of the V_{GA} gate bias applied during the avalanche stress. This displacement remains linear as long as I_B peak is not situated in the region where other surface phenomena occur. However, the I_B peak amplitude depends on stress parameters and varies like $(I_A \cdot t_A)^{1/n}$ with $2 < n < 10$, depending on the devices.

The experimental study of the base current localized increase permits to precise two points of the involved physical phenomenon (Fig. 4) that is :

— A recombination rate increase in the surface transition region of the emitter base junction due to the created surface states during avalanche.

FIG. 3. — Variation of I_B with V_{GM} in forward bias conditions for different values of V_{GA} during avalanche breakdown stresses.

FIG. 4. — During Avalanche : Creation of surface states by the sweeping of the maximum electric field point. Reading : Effect on forward condition bias of V_{GM} upon I_B after avalanche breakdown stress.

— A hot carriers injection and a trapping in the oxide which alters the silicon surface potential.

The amount of charges induced in the silicon in the neighbourhood of the surface can be written in the form :

$$-\Sigma_{Si} = C_0 \left(V_G - V_s - \frac{\Sigma_0}{C_0} + \frac{\Sigma_{SS}}{C_0} - \varphi_{MS} \right)$$

where :

V_s is the surface potential,

C_0 is the gate capacitance (per unit area).

Σ_0 is the density of charges induced by the oxide charges.

Σ_{SS} is the density of interface charges.

φ_{MS} is the work function difference between metal and silicon.

Depending on the type of the considered region they appear as an accumulation or a depletion of carriers in the silicon near the surface. So the emitter base transition region bends. In the forward condition, one can obtain a displacement of the point where the electric field is maximum, where the effect of recombination is there fore maximum too (intrinsic point). The base current peak appears for a gate bias V_{GM} which makes this maximum field point coincide with the created recombination centers.

3. Experimental support of the model. — To confirm and precise this model, complementary experimental studies have been done, relating to the degradation nature, localization and to carriers injection.

3.1 BV_{BE} BREAK DOWN VOLTAGE AND I_G GATE CURRENT EVOLUTIONS (Fig. 5). — It is known that an important variation of the BV_{BE} voltage (walk-out phenomenon) can be obtained only if the oxide thickness is inferior to the surface transition region width.

FIG. 5. — BV_{BE} and I_G evolution during the avalanche breakdown stress.

That condition is not fulfilled for our samples; however the weak recorded variations show that carriers injection and trapping create a space charge region in the silicon, tending to annul the gate bias action and to bring the avalanche point back into the metallurgical junction neighbourhood, reducing at the same time BV_{BE} value to the value taker for $V_{GA} = 0$ V.

Another interesting evolution to be followed during the stress is the avalanche gate current I_G .

During a stress under $V_{GA} = 150$ V, an important gate current can be observed, I_G decreases corresponding to the trapping of electrons progressively annulling the gate bias effect. The gate current evolution time factors are the same as those of BV_{BE} voltage evolution. It has been possible to notice as well that if I_G peak amplitude obviously depends on the device geometrical and technological parameters it also heavily depends on the device realization conditions.

If the sample is submitted to a stress under

$$V_{GA} = -150 \text{ V}$$

one can observe a perfectly measurable gate current which corresponds to the previously injected electrons trapping. Let us note however that the hypothesis of a simultaneous holes injection and trapping cannot be ruled out.

The experiences about BV_{BE} and I_G evolutions have permitted to confirm that hot carriers injection brings the created modification back into the intrinsic point neighbourhood, and that the injected and trapped charge must be balanced by a V_{GM} gate bias, depending on V_{GA} , to retrieve the maximum modification in forward condition.

3.2 I_R EMITTER BASE REVERSE CURRENT (Fig. 6). — Other kind of experiences have permitted to specify the modification nature : study of the emitter base junction reverse current I_R as a function of the gate bias V_{GM} after avalanche [4].

The I_R current evolution can be divided into three regions, according to the surface current which are predominant.

Region 1 corresponds to the generation current in the space charge region induced by the field and varies like $\exp \frac{qV_{GM}^2}{2kT\varphi_B}$ (φ_B : potential barrier).

Region 2 corresponds to the generation current due to surfaces states and varies like $\exp \frac{qV_{GM}^2}{kT\varphi_B}$.

Region 3 corresponds to the generation current in the emitter base transition region, in the bulk or at the surface.

The evolution of this characteristic after avalanche shows that region 3 alone is disturbed : one can therefore confirm that the surface recombination rate modification exists only in the metallurgical junction neighbourhood.

FIG. 6. — V_{GM} dependence of junction reverse current I_R shows the displacement of I_R minimum with V_{GA} ($V_{BE\text{inverse}} = 1.5\text{ V}$).

4. **Functionnal model.** — These experimental studies have permitted to work out a functionnal model of tetrode bipolar transistors avalanche degradation. A schematic representation of the parameters occurring in this model is given in figure 7, which shows

FIG. 7. — Schematic representation of the space charge region at the surface of the structure in forward bias conditions.

the surface transition region in case of a direct bias. One can distinguish a disturbed region around the metallurgical junction : the surface states avalanche creation increases the surface recombination rate on a $\pm x_A$ distance of S_{oA} quantity. The X_i displacement of the point where the electric field is maximum depends on the Q_i trapped charge and on the applied V_G gate bias. When V_G is such as to annul Q_i effect, the degradation effect is maximum because the maximum field point coincides with the center of the disturbed region. When this condition is fulfilled, a numerical exploitation of the model is possible insofar as the phenomenon is no longer strongly bidimensionnal and subject to certain hypothesis.

- Gradual junction hypothesis justified by the characteristics symmetry around this point in relation to V_G .
- A gaussian or uniform repartition of the created surface states.
- A linear relation between V_G gate bias and X_i maximum field point displacement.

FIG. 8. — Modelling results : normalized ΔI_B variations dependence of model parameters x_i and x_A for a uniform and a Gaussian surface states increase.

The functional model gives normalized ΔI_B variations depending of the model parameters :

$$F = \frac{2 \Delta I_B}{q \eta_i X_0 S_{0A} P_E \exp \frac{V_{BE}}{2 U_T}}$$

where :

- κ_0 is the half width of the transition region,
- S_{0A} is the surface recombination rate,
- P_E is the perimeter of the base emitter junction,
- n_i intrinsic concentration.

The obtained numerical results are presented in figure 8 in case of a uniform and gaussian repartition of the traps for integrated device.

This model does not allow to foresee the transistors characteristics evolution after an avalanche stress; it permits however to characterize this evolution and a comparison of these experimental and numerical results gives a simple determination of the model parameters :

- I_B peak amplitude permits to determine S_{0A} .
- The calculated $(\Delta I_B / \Delta X_i)$ slope and the $(\Delta I_B / \Delta V_{GM})$ slope permit to give the linearity factor between V_{GM} and X_i .
- Finally, the peak width characterizes the disturbed region.

For devices having undergone a stress number superior to 10^3 , one has found a recombination rate increase of 2×10^4 cm/s on a ± 350 Å width around the metallurgical junction.

5. Conclusions. — The phenomenon of avalanche reversible modification of the gate controlled transistors H_{FE} gain can be used for the realization of an electrically REPRON memory. In that case, this model is going to allow to specify the origin of the aging problem observed on a great number of programming cycles. In fact the study of the model parameters evolution during programmations must permit to specify whether the aging is due to :

- a surface recombination rate continual increase,
- the disturbed region widening,
- less and less efficient trapping and untrapping.

The first obtained results on integrated devices are interesting and must permit to correlate the degradation efficiency with the resistance to aging. It has been possible to show, for example that the devices involving only an electrons trapping then untrapping in the programming gives a quicker programming and a lesser aging than devices making use of electrons and holes trapping.

References

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