Classification

Physics Abstracts

73.40Q — 73.60H

Dipolar relaxation effects in Al/SiO₂/Si structures investigated by Transient Capacitance Spectroscopy

E. Rosencher, R. Coppard, D. Bois and J. C. Pfister

CNET-CNS (RPT/PMD), B.P. 98, 38243 Meylan, France

(Reçu le 19 janvier 1984, accepté le 19 mars 1984)

Résumé. — La Spectroscopie de Transitoires Capacitifs (DLTS) dans les structures Métal-Oxyde-Semiconducteur (MOS) est généralement interprétée en supposant que le signal n'est dû qu'à l'émission thermique des porteurs piégés à l'interface Si/SiO₂, dans le film de SiO₂ ou dans le silicium. En utilisant un cycle original d'impulsions électriques, nous avons observé dans tous nos échantillons des transitoires capacitifs qui ne correspondent pas à ce mécanisme d'émission, mais sont en accord avec un mécanisme de relaxation de type dipolaire. Après chaque impulsion, la relaxation s'effectue dans la direction du champ électrique avec une constante de temps répartie, presque indépendamment de la température et de la tension appliquée (de 35 K à 200 K). Nous expliquons pourquoi ces relaxations dipolaires n'étaient pas observables par les techniques usuelles de caractérisation de MOS (capacité-tension, conductance). Enfin, l'origine physique de ces relaxations dipolaires est brièvement discutée.

Abstract. — Transient Capacitance Spectroscopy (DLTS) in Metal-Oxide-Semiconductor structures is usually analysed assuming that the only contribution to the variations in the semiconductor surface capacitance originates in detrapping of carriers from defects at the Si/SiO₂ interface or in the Si or SiO₂ bulks. Using original pulse configurations, we have detected, in all samples investigated, capacitance transients which cannot be accounted for by such classical emission mechanisms but are in accordance with a dipolar relaxation mechanism. After each pulse, the relaxation follows the electric field direction with a distributed time constant, almost independently of temperature and applied electric field (from 35 K up to 200 K). We further explain why these dipolar relaxation effects could not be observed easily *via* the usual capacitance or conductance measurements. The physical origin of these dipolar relaxations is briefly discussed.

Transient Capacitance Spectroscopy consists of detecting the capacitance transients of a semiconductor junction as a function of temperature in a selected time interval [1-2]. In a Metal-Oxide-Semiconductor (MOS) structure, the junction is at first biased in accumulation (excitation bias V_{ex}) for a time interval τ_{ex} generally very short (100 ns-100 μ s) in order to fill the impurity states with majority carriers. The junction is then biased in depletion (relaxation bias V_r) for a time interval τ_r , much longer than τ_{ex} . The charge state variation of the electronic traps is detected through the capacitance variation of the junction during the second phase by means of either a boxcar integrator [1-2] or a lock-in amplifier [3]. In a MOS device, these traps are located either

Fig. 1. — Band diagram and transient behaviour of a MOS structure due to : a) the emission of trapped majority carriers; b) dipolar-like relaxation.

in the silicon or silica bulks (③ and ① respectively in figure 1a), or at the Si/SiO₂ interface (② in figure 1a). In all cases, this emission of majority carriers leads to a shrinkage of the depletion layer, i.e., to an increase in the junction capacitance during the transient (see Fig. 1a). We have evidenced in MOS structure the opposite behaviour, i.e., a decrease in the capacitance during the transient. From a phenomenological point of view, we are in the presence of dipolar relaxation, the origin of which is still undetermined [4].

Several Al/SiO₂/Si structures having different technological origins were investigated and all exhibited the same behaviour. In this Letter, we report results for a MOS device described in the following. A four inch, n-type, < 100 > oriented silicon wafer is used, having a resistivity of 1-3 Ω.cm. Its backface is overdoped by ion implantation in order to yield a good backside ohmic contact. A 100 nm oxide is thermally grown in wet ambient at 950 °C for 1 h. The structure undergoes several annealing steps in order to lower the defect concentration in the structure. An aluminum layer is then evaporated onto the top surface and annealed at 450 °C in forming gas. Gates 1 mm in diameter are defined using standard photolithographic techniques. The device is then mounted in a circulating helium cryostat. The voltage cycles are provided by a pulse generator : the pulse durations (τ_{ex} and τ_r) and biases (V_{ex} and V_r) are controlled by a computer. The capacitance transients are detected *via* a home made impedance bridge : a gating circuit protects the detection set-up during high capacitance variations, e.g., while driving the MOS device in accumulation. This is particularly important in the experiments we present, in which drastic changes in capacitance are to be applied over relatively long periods of time (several milliseconds)

without saturating the detection system, which is not possible with usual commercial set-ups. The resulting time constant of the apparatus is then in the 20 μ s range. The time constant window is defined by a double gate boxcar integrator providing the capacitance transient amplitude $C(t_2) - C(t_1)$ at each temperature. The data are collected by a computer which controls the whole experiment.

In a first step, DLTS spectra of the MOS device are recorded for different filling pulse durations τ_{ex} . Curve 1 in figure 2 shows a typical DLTS spectrum of interface traps [3, 5]. No variations in the DLTS spectrum are observed when τ_{ex} is increased from 1 μ s to 100 μ s. This result is in accordance with an interface state filling time τ_s given by :

$$\tau_s = (\sigma_n \cdot v_{th} \cdot N_s)^{-1} \quad (1)$$

where v_{th} is the thermal velocity and N_s the volumic density of free carriers in the accumulation layer. For a typical capture cross-section of 10^{-15} cm^2 [6] and a concentration N_s of 10^{17} cm^{-3} the filling time τ_s is indeed in the 1 ns range.

However, as the filling pulse duration τ_{ex} is increased up to values comparable to τ_r , the DLTS signal drastically decreases, becoming negative when $\tau_{ex} \sim 5$ ms (curves 2 and 3 in figure 2). Such an effect cannot possibly be accounted for by any majority carrier emission mechanism. Moreover, in the temperature range investigated, the minority carrier density is very low [7], as is proved by the absence of any inversion layer formation. Nor can this effect arise from the backside series resistance [8]. This resistance is measured *via* the impedance bridge at each temperature and checked to be small, even decreasing with temperature down to 40 K. We are therefore led to

Fig. 2. — Influence of filling time duration τ_{ex} on the DLTS spectra in a MOS structure.

conclude that *these Transient Capacitance Spectra are the contribution of two distinct signals resulting from i) the emission of trapped majority carriers (classical DLTS) and ii) variations in the semiconductor surface potential opposite in sign to those due to majority carrier emission.* In phenomenological terms, this means that dipolar relaxation is evidenced in the MOS device (Fig. 1b).

Next, in order to distinguish the contribution of traps at the Si/SiO₂ interface from this dipolar-like relaxation, we apply biases low enough so as to avoid filling of the interface states. The MOS structure is therefore kept in deep depletion during the whole experiment. Moreover, since dipolar relaxation differs from emission-recombination on interface states in that the excitation time constant almost equals the relaxation time constant we have chosen $\tau_{\text{ex}} \sim \tau_r$. Figure 3 shows, at different temperatures, the DLTS signal variation as a function of bias V_r or, equivalently, as a function of the calculated electric field F_{ox} in the oxide film. The transients are sampled during time interval τ_r at $t_1 = 2.5$ ms and $t_2 = 5$ ms.

Firstly, the DLTS signal observed is not nil, indicating that the anomalous capacitance transient is not related to interface trap emission. Moreover, the signal sign ($C(t_2) - C(t_1) > 0$ during τ_r) is not compatible with the capture of carriers on deep levels located in the Si bulk. Once again, the peculiar nature of this signal is confirmed. Moreover, the relaxation amplitude increases with the oxide electric field F_{ox} . This is in agreement with an increasing polarization of defects submitted to an increasing electric field. Finally, let us note the insignificant influence of temperature on the relaxation amplitude.

Fig. 3. — Amplitude of the capacitance transient $C(t_2) - C(t_1)$ in the MOS device as a function of the oxide electric field F_{ox} for various temperatures. The voltage cycle is indicated in the inset.

We then studied the influence of excitation time duration τ_{ex} on the dipolar-like relaxation signal during time interval τ_r . Since, for practical reasons, the boxcar repetition period $\tau_{ex} + \tau_r$ is kept constant, the value $\tau_{ex} + \tau_r$ is chosen high enough (26 ms) so that the variation in τ_r remains comparatively small. In figure 4, results are shown for different applied biases at $T = 77$ K. It can be seen that the DLTS signal $C(t_2) - C(t_1)$ is closely approximated by the relation :

$$C(t_2) - C(t_1) = f(F_{ox}) \times \ln(\tau_{ex}/\tau_0) \quad (2)$$

for

$$\tau_{ex} > \tau_0$$

where $f(F_{ox})$ describes the electric field dependence of the relaxation amplitude and $\tau_0 \sim 0.2$ ms is independent of temperature and electric field, but varies with the time constant window (t_1, t_2) [9]. This logarithmic dependence on excitation time τ_{ex} is indicative of a relaxation mechanism having a distributed time constant.

This distributed time constant and the absence of temperature influence suggest a dipolar relaxation mechanism based on the tunnelling effect onto a continuum of states [10, 11]. Indeed, a distributed time constant arising from a continuum of activation energy should yield a linear dependence of the relaxation amplitude on temperature [12]. Moreover, since the electric field seems to influence the signal's magnitude but not its kinetics, this suggests that the time constant distribution is not affected by the electric field.

Fig. 4. — Capacitance transient $C(t_2) - C(t_1)$ as a function of excitation time duration τ_{ex} for various applied biases V_{ex} . The voltage cycle is also shown in the inset.

The capacitance change ΔC between t_1 and t_2 is related to the polarization variation Δp in this time constant window by the relation :

$$\Delta p = \frac{q \cdot N \cdot \epsilon_s \cdot \epsilon_{ox} \cdot A^2}{C^3} \cdot \Delta C \quad (3)$$

where N is the doping concentration, ϵ_s and ϵ_{ox} the silicon and silica dielectric constants respectively, A the sample area and ΔC the quiescent MOS capacitance during time interval τ_r . From the data in figure 3, Δp is found to be equal to $2 \times 10^{-15} \text{ C} \cdot \text{cm}^{-1}$ for an electric field variation of 50 kV/cm ($\Delta C = 0.1 \text{ pF}$) in the time constant window (2.5 ms-5 ms).

The physical origin of this dipolar relaxation is still undetermined. It may originate from dipole defects in the SiO_2 bulk. However, the dipole relaxations in SiO_2 which have been the most extensively studied in the literature, such as OH^- , are reported to vanish above 10 K [13]. These dipolar defects might be located at the Si/SiO_2 or SiO_2/Al interface (such as Si-H) where various authors [14] suspect them to induce barrier height fluctuations in MOS structures, e.g., after post-metallization annealing. Finally, these dipolar relaxation effects might originate from tunnel injection of electrons from the metal gate onto a continuum of states located in a perturbed layer near the SiO_2/Al interface. Indeed, these two types of explanations (dipole defects, tunnel injection) are electrically indistinguishable. Both consist of a displacement of charges related to a defect density N_d over a distance d .

In order to infer a defect concentration N_d from our data, we have made the following assumptions :

— The displacement d for an oxide electric field F_{ox} of 50 kV/cm is in the $10 \text{ \AA}$ range.

— The fraction of defects f which respond in the time constant window (t_1, t_2) is given by $\ln(t_2/t_1)/\ln(\tau_{\max}/\tau_{\min})$, where $\tau_{\max}$ and $\tau_{\min}$ are the extreme values of the dipolar relaxation times [10]. Taking *arbitrary* 6 decade dynamics, this yields $f = 1/20$.

With these assumptions in mind, we find either a surface defect concentration in the 10^{12} cm^{-2} range, or a bulk concentration of 10^{17} cm^{-3} if the defects are located uniformly in the SiO_2 layer.

The transient behaviour of dielectric layers related to dipolar relaxation has been known for the past 70 years as the « Curie-von Schweidel law ». The presence of such an effect has naturally been considered by many authors to be the possible origin of the electrical losses in MOS structures observed in conductance ($G(\omega)/\omega$) or capacitance ($C-V$) experiments [15]. In order to account for dipolar relaxation effects in MOS devices, Nicollian and Brews have developed a simple two potential well model, in which the equilibrium population of the two wells changes with gate bias [16]. Using Boltzmann's statistics, they have deduced a single time constant behaviour for dipolar relaxation kinetics and found that the calculated bias dependence of this time constant could not account for its experimentally observed variation of 6 orders of magnitude. They consequently discarded dipolar relaxation as the origin of electrical losses in MOS devices.

However, this latter conclusion does not eliminate the possible presence of dipolar relaxation in MOS devices but rather means that it is not detected *via* the usual conductance measurements. Actually, in classical conductance measurements, the amplitude of the probe signal v_a is small (40 mV) and dephasing related to dipole relaxation $G_d(\omega)/\omega \cdot C$ is expected to be small compared to interface state related dephasing $G_{ss}(\omega)/\omega \cdot C$. *Indeed, the amplitude of the dipole relaxation which responds to the a.c. signal frequency $\omega(G_d(\omega)/\omega \cdot C)$ is a function which increases continuously with the amplitude of v_a . This is not so for $G_{ss}(\omega)/\omega \cdot C$.* Typically, for a probe signal amplitude of 40 mV, the dephasing $G_d(\omega)/\omega \cdot C$ corresponding to data from figure 3 should be in the 10^{-5} range, whereas $G_{ss}(\omega)/\omega \cdot C$ is found to be in the 10^{-3} range.

The influence of these dipolar relaxations on the $C-V$ characteristics is more complex. Some of them, i.e. those following the voltage scan, tend to induce a *steeper C-V characteristic*, bringing about a virtual negative density of interface states. Slower relaxations result in a hysteresis opposite

in direction to the effect of ion drifting in SiO_2 . Finally, some dipolar defects might remain unaffected by the bias over a very long period of time, thereby inducing an apparent constant change in the barrier height of the MOS structure [14]. As far as the first two mechanisms are concerned, the voltage shift in the C - V characteristic associated with a concentration of 10^{12} dipoles. cm^{-2} would be hardly detectable (in the few millivolts), as it is probably masked by such other effects as surface potential fluctuations... A complete theoretical model is to be published shortly [9].

Finally, let us emphasize that these dipolar relaxation effects do not invalidate the DLTS technique as a powerful method of characterization for interface states. In order to overcome dipolar effects, the duty cycle ratio τ_{ex}/τ_r should be chosen very small (10^{-1} to 10^{-2} %). On the other hand, the use of *Metal-Insulator-Semiconductor structures together with Transient Capacitance Spectroscopy* provides a new and very sensitive method for studying the dipolar relaxation mechanism in insulators, particularly under high electric field conditions (10^5 - 10^6 V. cm^{-1}).

References

- [1] LANG, D. V., *J. Appl. Phys.* **45** (1974) 3023.
 - [2] JOHNSON, N. M., BARTELINK, D. J. and SCHULZ, M., *The Physics of SiO_2 and its Interfaces*, edited by S. T. Pantelides (Pergamon, New York) 1978, p. 421-427.
 - [3] ROSENCHER, E. and COPPARD, R., *J. Appl. Phys.* (in press).
 - [4] The possible contribution of dipole defects to the DLTS signal in GaAs bulk has already been considered by Van Vechten *et al.* in VAN VECHTEN, J. A., RANSOM, C. M. and CHAPPELL, T. I., *J. Phys. Soc. Jpn* **49** Suppl. A (1980) 251.
 - [5] ROSENCHER, E. and BOIS, D., *Appl. Phys. Lett.* **40** (1982) 601.
 - [6] JOHNSON, N. M., *J. Vac. Sci. Technol.* **21** (1982) 303.
 - [7] SZE, S. M., *Physics of Semiconductor Devices* (J. Wiley, New York) 1969.
 - [8] BRONIATOWSKI, A., BLOSSE, A., SRIVASTAVA, P. C. and BOURGOIN, J. C., *J. Appl. Phys.* **54** (1983) 2907.
 - [9] ROSENCHER, E. and COPPARD, R. (to be published).
 - [10] KLIEM, H. and ARLT, G., *Insulating Films on Semiconductors*, edited by J. F. Verweij and D. R. Wolters (North-Holland) 1983, p. 211-214.
 - [11] MOTT, N. F. and DAVIS, E. A., *Electronic Processes in non-crystalline materials* (Clarendon Press, Oxford) 1979.
 - [12] FRÖHLICH, H., *Theory of Dielectrics* (Oxford University Press) 1958.
 - [13] PHILLIPS, W. A., *Philos. Mag. B* **43** (1981) 747.
 - [14] HICKMOTT, T. W., *J. Appl. Phys.* **51** (1980) 4269.
 - [15] NICOLLIAN, E. H. and GOETZBERGER, A., *Bell Syst. Techn. J.* **46** (1967) 1055.
 - [16] NICOLLIAN, E. H. and BREWS, J. R., *MOS Physics and Technology* (J. Wiley, New York) 1982.
-