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INTERFACIAL DEFECTS IN GaAs/Si AFTER ANNEALING

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Abstract - The threading defects involved in the GaAs/Si heterostructure have been studied in as-grown and annealed specimens. Their origin is related to the imperfections of the interface : impurities, roughness and discontinuities of misfit dislocation network. Large parts of the GaAs layer are almost free of stress in the annealed specimen. Residual stresses and defects are located at the boundaries between the Lomer dislocation arrays. Small antiphase domains are also observed.

1. INTRODUCTION

It is well established that the high defect density, which appears in the GaAs layers grown on silicon, limits the possibility of applications of this heterostructure /1/. These defects are formed because of the different lattice constants and thermal expansion coefficients of GaAs and Si. As a result of these mismatches, defects in the GaAs film are formed during the growth process or during postgrowth cooling by their propagation into the epilayer. Many works on GaAs/Si and more generally on semiconductor heterostructures with large lattice mismatch are concerned with the reduction of the defect density in the active layer using post annealing /2/ or strained superlattice /3/. The fundamental question is not to know how to reduce by one or two orders of magnitude the defect density but to obtain directly a heteroepitaxial system without defects in the deposited layer. In order to progress in this direction it is necessary to determine the origin of the defects which thread in the epitaxial layer.

This paper gives some results obtained by TEM on the structural defects involved in the GaAs/Si heterostructure. More precisely, the origin of threading defects is discussed in terms of interface and misfit dislocation network imperfections.

2. SPECIMEN PREPARATION

The samples are grown by Molecular Beam Epitaxy in a RIBER 2300 and a Varian Gen II MBE systems. The (001) silicon substrates are misoriented by 4° toward <110>. The substrate preparation has been described elsewhere /4/. One of the goals of the GaAs/Si epigrowth is to obtain a uniform layer thickness. For this reason, it is necessary to limit the three dimensional (3-D) growth of GaAs by using a low substrate temperature at the beginning of the first stage of the epitaxy. 300°C is taken in this work. The first 10 nm have been grown by MEE (Migration Enhanced Epitaxy) at 300°C /5/; the next 50 nm by MBE also at 300°C. The thermal annealed samples have been heated in situ at 640°C for 75 min in order to improve the crystalline quality of the GaAs film /2/.

A thickness of 60 nm has been chosen because it is sufficiently large to obtain misfit dislocations. It is also small enough to avoid relaxation of strain associated with the thermal expansion mismatch and the difference between growth and room temperatures. In addition, this thickness is such that the GaAs/Si interface can be studied directly by plan view technique without preparation of the GaAs film.

3. TEM OBSERVATIONS

The defects of the GaAs layer are studied using plan view samples by moiré and weak-beam techniques.

The (110) cross-sectional samples are not adapted to the study of a complete misfit dislocation network. In this case, the (001) interface is imaged as a line and only the set of $\langle 110 \rangle$ dislocations can be seen [6]. Information is obtained with plan view technique. With the electron beam parallel to the growth direction, the interface between GaAs and Si is directly imaged on the TEM screen. The specimen preparation for observations consists only of the silicon substrate thinning by chemical etching from the back side, since the 60 nm layer of GaAs is transparent to the 200KV electrons.

The crystalline imperfections have been observed in the GaAs layer by the moiré technique described by ROCHER et al. [7]. Moiré patterns are formed by superposing the GaAs epilayer and the Si substrate. In the case of perfect GaAs films deposited on Si, moiré fringes are uniform and strictly parallel to the reflecting planes. The moiré fringe deviations reveal the imperfections which disturb the crystallinity of the GaAs epilayer. Techniques based on a single and double system of moiré fringes have been employed in this work. A single system of fringes is obtained with only one reflection in Bragg position. The experimental conditions for double moiré observations are defined as follows: the incident beam, nearly parallel to (001)Si, passes through GaAs and Si and produces the moiré pattern. More precisely, the (220) , $(\bar{2}\bar{2}0)$ and (400) are in Bragg position. Double diffraction effects occur [8]. The bright field and the (400) dark field images simultaneously show the two perpendicular moiré fringes related to the (220) planes of Si and GaAs.

4. EXPERIMENTAL RESULTS

Fig. 1a is a (220) moiré pattern of the as-grown specimen. The fringe system is not well defined, is related to a poor crystallographic quality of the layer. Nevertheless, the moiré spacing, equal to 5.4 nm, shows that the lattice parameter of the GaAs layer is close to its bulk value.

The weak beam image of fig. 1b gives absolutely no evidence of an organized misfit dislocation network. Below 350°C the GaAs layer cannot be deformed plastically and the layer is always under stress [9]. The partial relaxation experimentally observed could be explained by twinning processes and a density of point defects.

Misfit dislocations

After the *in situ* thermal annealing, the misfit dislocation network becomes completely different as observed on fig. 2. This figure shows the beam images given by the (220) and $(\bar{2}\bar{2}0)$ Bragg reflections where the different families of dislocations are seen. The experimental extinction conditions observed on fig. 2a and 2b characterize the misfit dislocations as Lomer type with their direction and burgers vector in the (001) GaAs/Si interface ($\langle 110 \rangle$, $b = 1/2 \langle 110 \rangle$). Their spacing is equal to 10 nm which is in agreement with the theoretical value associated with Lomer type dislocations. More than 95% of misfit dislocations are of Lomer type.

Fig.1 : Plan view of the as-grown GaAs/Si : a) moiré pattern associated to a (220) reflection; note the not well defined fringes. - b) (220) weak beam image; there is no straight misfit dislocations.

The measured length of dislocations segments is from 10 to 100 nm. It is nearly the same in each $\langle 110 \rangle$ direction. There is no influence of the steps related to the vicinal surface on the structure of the misfit dislocations. The dislocation lines are not so straight. These results are certainly related to the formation and the rearrangement of the misfit dislocations during the annealing process in relation to the physical and chemical quality of the substrate surface. They can be also related to the roughness of the interface as observed by HULL et al. and ROCHER et CHARASSE /11, 6/.

Fig. 3a is a (400) weak beam image of the misfit dislocation network. Here, it appears as complex array of small white triangles organized along the two $\langle 110 \rangle$ directions. These white triangles are due to a residual contrasts of the two families of perpendicular misfit dislocations. Similar observations have been performed by ISHIDA /10/. The triangles are organized in arrays of limited size : less than ten of them in each direction. All the areas with a perfect dislocation network are free of threading defects.

According to CHOI et al. /2/, the annealing process is very efficient for improving microstructures of epilayers having a high density of defects. No stacking faults and microtwins are observed in the annealed GaAs film.

Defects in the epilayer

The fig. 3b shows a moiré pattern obtained with the experimental conditions described above on the same area than fig. 2 and fig. 3a. The observed moiré pattern is not uniform. Perfect double moiré fringe system are seen in many areas with a typical size of about 100 nm where the GaAs film is free of stress. The directions of each system of moiré fringes are parallel to the (220)Si planes. The observed moiré fringe spacing is equal to 5 nm for the (220) reflection as given by calculation assuming bulk GaAs and Si lattice constants. Fringes are locally deformed and they can also disappear completely. Such contrast is related to local changes in the orientation of the GaAs layer and show the region under stress.

Fig. 2 : Plan view of the GaAs/Si annealed specimen. Observation of the two set of misfit dislocations using (220) and $(\bar{2}\bar{2}0)$ weak beam images. Misfit dislocations are characterized as Lomer with a mean spacing of 1 μm . Note the limited length of dislocation segments.

Fig. 3 : Same area than fig. 2. -a) (400) weak beam image shows misfit dislocation network organized as sub-arrays. Note that the dislocation sub-arrays are free of threading defects. -b) moiré pattern : note the 2-D perfect lattice and the regions, such as A, which are under stress.

A typical imperfection, arrowed A, is shown on fig. 3b. Fig. 3a is (400) weak beam image of the same region. There is a direct correspondence between A on fig. 3b and the high concentration of defects observed in

fig. 3a. This high concentration of defects is located at a boundary between two misfit dislocation sub-arrays.

The size of homogeneous moiré zones is 2 or 3 times larger than the size of the misfit dislocation sub-array. The coalescence between two interfacial dislocation sub-arrays can be then obtained without emission of defects in the epilayer.

The density of threading dislocations is, in these conditions, related to the size of the misfit dislocation sub-array. In the ideal case, the misfit dislocation network could be constituted by an unique and perfect two dimensional Lomer dislocation array covering all the interface to avoid all the threading defects.

Antiphase boundaries

The antiphase boundary (APB) is one of the most controversial defects in the GaAs/Si heterostructure. APB have been observed on these specimens using the (200) reflexion of GaAs in Bragg position. This experimental condition has been chosen because : i) the (200) is a forbidden reflection for silicon, and the intensity I_{200} given by the silicon is always very weak. There are then no moiré fringe system to mask the contrast due to APB. ii) the two different kinds of domains are characterized by the exchange of the Ga and As sites. The (200) structure factors of each domain are given by :

$$F(200) = 4 * (f_{Ga} - f_{As}) \text{ and } F'(200) = 4 * (f_{As} - f_{Ga})$$

In Bragg condition the (200) diffracted intensity is equal in the two domains. When the electron beam goes through the APB there is a change in the sign of the structure factor which give an important contrast /8/. The 60 nm layer of GaAs is thin enough to give a simple black/white contrast without fringes.

The (200) dark field image of fig. 4 shows typical dark contrasts, marked A, which are directly related to antiphase boundaries. Their shapes, looped ribbons, are elongated in a $\langle 110 \rangle$ direction. the sizes are limited to about 100 nm and 30 nm. A very large majority of the layer is constituted by the same GaAs structure. Only less than 1% of the layer is constituted by the antiphase structure AsGa. The low density of antiphase domains (GaAs/AsGa) is probably related to the roughness experimentally observed at the GaAs/Si interface /6, 11/.

Fig.4 : Observation of antiphase boundaries. (200) dark field image. Note the limited size of the antiphase domains.

5. CONCLUSION

The high density of defects observed in the GaAs/Si heterostructure appears to be directly related to the interface imperfections : roughness defects of the misfit dislocation network. In particular, the density of threading defects is a function of the size of homogeneous misfit dislocation sub-arrays.

The result concerning the thermal origin of the misfit dislocations is certainly important : at low temperature there is no plastic deformation, which relaxes the stresses due to the lattice mismatch. At high temperature growth appears which is not in good agreement with a uniform thickness deposition. This remark suggests that growth temperature must be high enough to enable to deform plastically the GaAs layer and low enough to limit the growth.

Despite the progress made up to date, the optimization of the growth conditions of GaAs on Si has not yet been achieved. The reduction of defect density in the GaAs/Si heterostructure needs a better understanding of the effect of both the three dimensional growth and the surface quality of the substrate on the mechanism of creation of misfit dislocations. Finally, theory it would be possible to obtain GaAs/Si free of threading dislocations if a perfect misfit dislocation network located at the interface could be achieved.

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