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FUTURE BIPOLAR DEVICE STRUCTURES

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Abstract - Recently developed bipolar device structures including their problems and future trends are reviewed. Polysilicon emitter-base self-aligned structures and trench isolation techniques are becoming key elements for high performance bipolar ECL device structures, by which parasitic capacitances and resistances have been reduced drastically. In order to get further improved performance, smaller parasitic capacitances associated with the pull-up resistor as well as high cutoff frequency are required. Wafer-direct-bonded SOI structures are the promising candidate, while the base resistance and the cutoff frequency should be optimized moderately. The most serious problem is the power dissipation of ECL-type circuits. Smaller logic swings and low temperature operation should be also considered.

1 - INTRODUCTION

As the integrated circuit industry has come to the mature stage, the role of each device is getting more and more distinct. CMOS is the major VLSI and/or ULSI device because of the low power dissipation, while bipolar is in the high speed ranges with less integration level, and GaAs is in the small scale high frequency IC domains. Recently, between CMOS and bipolar ECL, BiCMOS has emerged with higher speed than CMOS and less power dissipation than ECL. With the advent of BiCMOS, conventional S-TTL or IIL digital devices seem to be swept out in the field of bipolar VLSI's such as gate arrays although standard LS- or ALS-TTL families are still in volume production. At present, the major role of bipolar devices has focused on very high speed logic devices with larger integration level than GaAs, which are achieved by ECL-type circuits. ECL has just become a major driving force for the progress of high performance bipolar device technologies. In this paper, the present status of the bipolar technologies is reviewed and by examining the problems of bipolar devices especially, ECL-type circuits, future bipolar device structures and suitable features are discussed.

2 - PRESENT BIPOLAR DEVICE TECHNOLOGIES

There have been several good reviews about bipolar device and circuit technologies. Especially, in the article /1/, almost all of bipolar device structures and circuit examples before 1980 were reviewed. In the articles /2,3/, advanced bipolar device structures developed recently were compared and discussed, while the similar topic was also discussed in the article /4/. In this section, recently developed bipolar device structures are rearranged and their essential properties are pointed out.

2 - 1 Device Structures

Since the development of DOPOS technique /5/, polysilicon has been used as the emitter electrode as well as the emitter diffusion source. In the end of the seventies, a
polysilicon self-aligned (PSA) technique /6/ also utilized polysilicon as a base electrode. Based on these techniques, self-aligned techniques using the polysilicon as both the emitter and the base electrodes accompanied with anisotropic dry etching techniques made it possible to realize sophisticated self-aligned bipolar device structures /7,8/. These techniques were mainly intended to achieve
(1) reduction of parasitic base-collector capacitances
(2) reduction of base resistances
without using tight lithography rules. The key structure is the stacking polysilicon electrodes separated by a sidewall insulating spacer. Another approach was also employed to achieve those two requirements by trying to make an ideal one-dimensional structure, or to make a symmetrical emitter and collector structure. This structure was formed by mesa-etching combined with a planarizing polysilicon technique /9/ or selective-epi-silicon growth in grooves /10/. There is one more important structure implemented in bipolar devices, that is trench isolation /11,12,13/. By introducing trench isolation, the collector-substrate capacitance has been reduced much smaller than that of oxide isolation. Concerning trench isolation, there is a review in the article /14/. By improving these techniques and combining them, a lot of advanced bipolar device structures have been developed in the eighties. The stacking double polysilicon self-aligned structures are named such as SST /7/, Self-aligned transistor /8/, OXIS-III /15/, SAPT /16/, SDD /17/, ExCL /18/, MOSAIIC-III /19/ and ESPER /20/ . Similar structures were also reported in the articles /21,22,23,24,25,26/ . These structures can be easily combined with trench isolation techniques. The most advanced examples are shown in Fig.1. The mesa-etched or selective-epitaxially grown sidewall-base-contacted structures are named SICOS /9/ or Symmetrical transistor /10/. A sophisticated self-aligned transistor using selective growth of poly- and single-crystalline silicon was demonstrated /27/. There is also an advanced version of SICOS as shown in Fig.2.

Fig. 1 - Advanced double polysilicon self-aligned structures.
(a) SST-1B. A selectively implanted deep collector (SIC) region is formed beneath the intrinsic base /28/.
(b) ESPER combined with U-FOX. Typical combination with trench isolation /20/.

Fig. 2 - Sidewall base contact structures.
(a) Self-aligned transistor using selective growth of poly- and single-crystalline silicon /27/.
(b) SELECT/SICOS. Edge contact structure is applied to conventional SICOS /29/. 
2-2 Device Characteristics

Ring oscillator results demonstrated by the previously mentioned device structures are listed in Table 1. The basic gate delay time of 20.5 ps was achieved by an NTL circuit, and sub-40 ps delay times were demonstrated by ECL circuits. Practical device performances are also listed in Table 2. Subnanosecond static RAM's, sub-50 ps gate arrays, 10 GHz frequency dividers have been demonstrated. Using advanced bipolar device technologies, not only high frequency small scale IC's but also very high speed LSI's or VLSI's have been realized.

Table 1 - Ring oscillator results by advanced bipolar technolgies.

<table>
<thead>
<tr>
<th>Company</th>
<th>Circuit</th>
<th>tpd</th>
<th>Power or Ics</th>
<th>Emitter Size</th>
<th>Technology</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTT</td>
<td>NTL</td>
<td>20.5 ps</td>
<td>2.32 mW/G</td>
<td>0.35x13 um²</td>
<td>SST-1B</td>
<td>/28/</td>
</tr>
<tr>
<td>NTT</td>
<td>ECL</td>
<td>34.1 ps</td>
<td>7.54 mW/G</td>
<td>0.35x 7 um²</td>
<td>SST-1B</td>
<td>/28/</td>
</tr>
<tr>
<td>Fujitsu</td>
<td>ECL</td>
<td>38.8 ps</td>
<td>1.28 mA/G</td>
<td>0.35x10 um²</td>
<td>ESPER **</td>
<td>/20/</td>
</tr>
<tr>
<td>Hitachi</td>
<td>ECL</td>
<td>46.7 ps</td>
<td>0.58 mA/G</td>
<td>2x 3 um²</td>
<td>SELECT/SICOS</td>
<td>/29/</td>
</tr>
<tr>
<td>Plessey</td>
<td>CML</td>
<td>50 ps</td>
<td>------------</td>
<td>------------</td>
<td>HE1 **</td>
<td>/26/</td>
</tr>
<tr>
<td>NEC</td>
<td>ECL</td>
<td>52 ps</td>
<td>2 mA/G</td>
<td>1x 8 um² *</td>
<td>***</td>
<td>/30/</td>
</tr>
<tr>
<td>CETRI</td>
<td>CML</td>
<td>52 ps</td>
<td>0.16 mW/G</td>
<td>1.5x 3 um²</td>
<td>***</td>
<td>/23/</td>
</tr>
<tr>
<td>Matsushita</td>
<td>CML</td>
<td>53 ps</td>
<td>3.2 mW/G</td>
<td>0.5x12 um²</td>
<td>***</td>
<td>/24/</td>
</tr>
<tr>
<td>Tektronix</td>
<td>ECL</td>
<td>54.6 ps</td>
<td>1.8 mA/G</td>
<td>0.5x10 um²</td>
<td>***</td>
<td>/24/</td>
</tr>
<tr>
<td>SONY</td>
<td>---</td>
<td>69 ps</td>
<td>0.43 mA/G</td>
<td>0.6x 1 um²</td>
<td>***</td>
<td>/25/</td>
</tr>
<tr>
<td>IBM</td>
<td>ECL</td>
<td>73 ps</td>
<td>12 mW/G</td>
<td>0.8x 2 um²</td>
<td>Self-Aligned</td>
<td>/32/</td>
</tr>
<tr>
<td>Motorola</td>
<td>ECL</td>
<td>75 ps</td>
<td>0.8 mA/G</td>
<td>1.5x 4 um²</td>
<td>MOSAIC-III</td>
<td>/19/</td>
</tr>
<tr>
<td>Fairchild</td>
<td>ECL</td>
<td>80 ps</td>
<td>0.9 mA/G</td>
<td>1.5x2.5 um²</td>
<td>SAPT **</td>
<td>/16/</td>
</tr>
</tbody>
</table>

*; Mask size. **; Combined with trench isolation. ***; Double polysilicon self-aligned structures.

Table 2 - Recently developed high performance bipolar devices.

<table>
<thead>
<tr>
<th>Device</th>
<th>Performance</th>
<th>Technology</th>
<th>Company</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>5K ECL RAM</td>
<td>t_AA= 0.85 ns</td>
<td>Self-Aligned Tr. and Trench Iso.</td>
<td>IBM</td>
<td>/33/</td>
</tr>
<tr>
<td>16K ECL RAM (&amp; 1.2K G.A.)</td>
<td>t_AA= 2.8 ns</td>
<td>IOP-II</td>
<td>Fujitsu</td>
<td>/34/</td>
</tr>
<tr>
<td>32K RAM</td>
<td>t_AA= 3 ns</td>
<td>Trench Iso.</td>
<td>IBM</td>
<td>/35/</td>
</tr>
<tr>
<td>64K ECL G.A.</td>
<td>t_AA= 5 ns</td>
<td>IOP-II</td>
<td>Fujitsu</td>
<td>/36/</td>
</tr>
<tr>
<td>2.1K ECL G.A.</td>
<td>tpd= 43 ps</td>
<td>SST-1B</td>
<td>NTT</td>
<td>/37/</td>
</tr>
<tr>
<td>13K ECL G.A.</td>
<td>tpd= 100 ps</td>
<td>HEP</td>
<td>AMC</td>
<td>/38/</td>
</tr>
<tr>
<td>10K ECL/15K CML G.A.</td>
<td>tpd= 120 ps</td>
<td>OXIS-IIIH</td>
<td>Siemens</td>
<td>/39/</td>
</tr>
<tr>
<td>18K ECL G.A.</td>
<td>tpd= 150 ps</td>
<td>SCOT</td>
<td>Mitsubishi</td>
<td>/40/</td>
</tr>
<tr>
<td>16b Multiplier</td>
<td>tm= 4.3 ns</td>
<td>SST-1B</td>
<td>NTT</td>
<td>/37/</td>
</tr>
<tr>
<td>1/8 Divider</td>
<td>ft=10.38 GHz</td>
<td>SST-1A</td>
<td>NTT</td>
<td>/41/</td>
</tr>
<tr>
<td>8b A-D Convertor</td>
<td>fs= 400 MHz</td>
<td>SST-1A</td>
<td>NTT</td>
<td>/42/</td>
</tr>
</tbody>
</table>

* t_AA; Address access time.
** tpd; Basic gate delay time.
*** tm; Multiplication time.
**** fs; Sampling frequency.

2-3 Properties of Present Bipolar Device Structures

The technique utilizing polysilicon is one of the key properties for the present advanced bipolar device technologies. The polysilicon is used as a contact material for both the emitter and the base as well as the diffusion sources. The polysilicon electrodes are easily separated by the oxide of polysilicon, realizing the minimum distance between the base and the emitter. This causes the small base-collector capacitance and the small base resistance. At the same time, sidewall spacer techniques also provide easily lower submicron emitter widths with only upper submicron lithography rules. In addition, the polysilicon emitter contact enhances the current gain, although the mechanism is not yet clearly understood. By optimizing the process condition, the current gain can be increased
without suffering from high emitter series resistances /43/. Another major property is trench isolation. It not only enhances the packing density but reduces drastically the collector-substrate parasitic capacitance compared with conventional oxide isolation. By using these techniques, the switching speed as well as the power dissipation of ECL-type circuits has been improved. VLSI chips of ECL circuits are now coming in the market /44/.

3 - PROBLEMS OF PRESENT BIPOLAR DEVICE STRUCTURES

In this section, the problems concerning the advanced bipolar device structures of typical two cases are discussed.

3-1 Double Polysilicon Self-aligned Structures

The most serious problem of this structure is the sidewall spacer thickness control. There are two sequential ways to form the implanted intrinsic base region and the sidewall spacer; sidewall etching followed by base implantation and vice versa. In the case of the former, although there is little damage for emitter-window opening, the cross-link region between the intrinsic base and the extrinsic (graft) base should be formed by lateral diffusion from the polysilicon base electrode. Too much lateral diffusion enhances peripheral tunneling leakage, while less encroachment causes punchthrough /45/. In the case of the latter, there is little cross-link problem because the intrinsic base region exists just beneath the sidewall spacer. However, careful emitter opening using anisotropic dry etching should be required. Even in this case the emitter junction depth, the sidewall spacer thickness, and the base depth should be optimized to avoid too much lateral encroachment.

Another problem is a tight alignment control between the graft base mask and the intrinsic base opening mask when the base-collector capacitance is tried to be reduced. The double polysilicon self-aligned structures require one mask alignment step if the walled base structure is employed, even if lower submicron emitter widths and emitter-base separation can be achieved without using tight minimum lithography rules. In the case of /7,23,28/, the graft base region is formed from the same mask as that of the intrinsic base formation without any alignment step. However, there is a disadvantage of the non-walled base structure that increases the outer peripheral parasitic base-collector capacitance. If a walled-base-like structure is introduced, a tightly aligned lithographic tool is needed.

3-2 Sidewall Base Contact Structures

The philosophy of sidewall base contact structures is mainly to realize an ideal symmetrical one-dimensional structure just as written in textbooks. It is the ultimate structure, but actual processes and device operations never result in one-dimensional behavior. The graft base diffusion control is the most serious problem in this structure. Sufficient graft base diffusion is necessary to achieve lower base resistance because only the sidewall regions are contacted by the doped polysilicon. The graft base diffusion occurs not only laterally towards the emitter but vertically along the oxide wall to the collector. The lateral diffusion enhances the emitter-base leakage current and the base-emitter capacitances just as the same situation as the double polysilicon self-aligned structures. Moreover, the vertical diffusion increases the base-collector capacitance. In order to avoid these problems, some process modifications have been tried sacrificing process simplicity /28,46/. Nevertheless, there are still contradictions between the base resistance and the base-collector capacitance.

4 - LIMITATIONS CONCERNING ECL CIRCUIT

The advantages of ECL circuits are not only their high speed operation but their excellent drivability of loaded capacitances. These are originated in the non-saturating operation of the current switch and the high transconductance of the emitter follower. However, their large power dissipation is the serious problem, that limits the integration level of ECL chips. A lot of circuit techniques have been tried to reduce the power dissipation of ECL-type circuits by using e.g. series gating, cascaded circuits of differential inputs and so on, but modified circuits usually have less flexibility for various applications of system designs. So, essentially the power dissipation of the current switch emitter follower should be decreased for VLSI or ULSI applications, whereas they never reduced to be nearly zero such as CMOS that dissipates the power only when switching. This means there is always a large gap between the largest integration level of CMOS chips and that of ECL chips. Nevertheless, the strategy of the optimization for ECL-type circuits is; the smaller the current, the lower the power dissipation.

How can the currents of ECL circuits be reduced without any degradation of the switching speed? The switching delay time (tpd) of ECL circuits is roughly expressed as
\[ t_{pd} = r_b C_b + R_L C_c + k_1 t_F \quad \text{(1)} \]

\[ C_b = k_2 C_d + k_3 C_{be} + k_4 C_{cb} \quad \text{(2)} \]

\[ C_c = k_5 C_{cb} + k_6 C_{cs} + k_7 C_L + k_8 C_{ef} \quad \text{(3)} \]

where \( r_b \) is the base resistance, \( R_L \) is the pull-up resistor, \( t_F \) is the transit time, \( C_d \) is the diffusion capacitance, \( C_{be} \) is the base-emitter capacitance, \( C_{cb} \) is the base-collector capacitance, \( C_{cs} \) is the collector-substrate capacitance, \( C_L \) is the wiring capacitance associated with \( R_L \), \( C_{ef} \) is the loaded capacitance associated with the emitter follower transistor, and \( k_1 \) to \( k_8 \) are the constants. If the logic swing is kept constant, the smaller switching current is achieved by larger \( R_L \). This is the way to reduce the power dissipation especially for the larger integration chips. Lower power ECL circuits are more influenced by the second term of Eqn.(1) and \( C_c \) must be reduced much more than high power circuits to improve the switching time. These can be realized only by the improvement of the device structure and the process technology. There is also the other way to obtain smaller switching current by reducing the logic swing. \( R_L \) can be kept constant when the switching current is reduced in proportion to the logic swing while the circuit noise margins are decreased. However, supposing that low temperature operation such as 77k is introduced, the reduction of the logic swing from the value of room temperature to a few tenths is not a ridiculous approach. Additionally, there is a possibility to enhance the efficiency of the cooling system.

The first term and the last term of Eqn.(1) are strongly correlated. The first term can be reduced by smaller base resistance \( (r_b) \). This means a highly doped intrinsic base region or a wide base width as well as smaller extrinsic base resistances are required. The last term can be reduced by smaller transit time, or higher cutoff frequency \( (f_T) \). The optimization of the effects caused by \( r_b \) and \( f_T \) is very important because smaller \( r_b \) often corresponds to lower \( f_T \) directly, although \( C_{be} \) and \( C_{cb} \) can be reduced by shrinking the active area. The highest \( f_T \) reported to date corresponds to the \( f_T \) of nearly 6.2 ps \((f_T=25.7 \text{ GHz})\), that is only \( 18\% \) of the total switching time \((t_{pd}=34.1 \text{ ps})\) /28/. If only the maximum \( f_T \) \((f_{T\text{max}})\) is raised to the twice value \((>50 \text{ GHz})\), the reduction of the transit time will contribute at most 3.1-ps decrease of the switching time. Only too high \( f_{T\text{max}} \) has very little influence on the delay time. Accordingly, moderate values of \( f_T \) and \( r_b \) should be chosen avoiding punchthrough and forward tunneling. Rather little contribution of \( f_{T\text{max}} \) upon the total switching time is the most different point from GaAs HBT. In the case of GaAs HBT, the transit time is \( 42\% \) of the switching time \((t_F=2.3 \text{ ps}, \ t_{pd}=5.5 \text{ ps})\) /47/. The contribution of RC time constants of GaAs HBT is much smaller than that of Si BJT. This is mainly because parasitic capacitances corresponding to the substrate are nearly zero owing to the semi-insulating GaAs characteristics. This fact suggests that the parasitic capacitances associated with the substrate of Si BJT should be reduced drastically to the nearly zero value.

In addition to the properties of ECL circuits using Si BJT mentioned above, there are still a few problems. When the switching current is reduced, the emitter area should be decreased to keep the cutoff frequency high enough for the optimized circuit operation. This is a suitable situation for the reduction of junction capacitances, but contact resistances as well as base resistances will increase. In order to avoid this problem, the process and device structural optimizations are also required.

5 - FUTURE BIPOLAR DEVICE STRUCTURES

Double polysilicon self-aligned structures and sidewall base contact structures will go on making a progress in the near future. However, sooner or later, the most suitable structure will be selected from not only the performance point but the production cost point of view. The double polysilicon self-aligned processes have been already used in volume production. The most sophisticated device has been realized by the double polysilicon self-aligned and trench-isolated structure using submicron lithography rules. It seems that double polysilicon self-aligned structures will be the major selection in the future because of their balanced cost and performance properties. Of course, present device structures are not optimised enough to achieve the ultimate performance of Si BJT. In this section, the future Si BJT structure to achieve the ultimate performance of ECL-type circuits in ULSI ranges are discussed.

As discussed in Section 4, the most crucial factor affecting the switching time and the power dissipation is \( R_{cc} \), \( C_{cs} \) and \( C_{ef} \). Among these capacitances \( C_{cc} \) can be reduced by the decrease of the base area using tightly aligned lithography tools, but never reaches zero. On the contrary, \( C_{cs} \) and \( C_{ef} \) can be reduced if the parasitic capacitances associated with the silicon substrate are decreased. \( C_{cs} \) can be reduced to the nearly zero value while \( C_{ef} \) may be less than a half if an insulating substrate is used. In other words, SOI is a very good choice to decrease both \( C_{cs} \) and \( C_{ef} \). A lot of SOI
techniques such as beam recrystallization, epitaxial lateral overgrowth and so on have been investigated for bipolar device applications, but there has always been a serious problem; the crystalline defects. However, recently wafer direct bonding techniques to obtain a thin SOI structure are coming up as a new face. According to these techniques, the crystalline quality of the SOI is essentially the same as that of single crystalline silicon wafers. This fact was proved by experimental 64K DRAM's /48/. Now, the SOI structure of bipolar devices are not a dream but a realistic target.

Next point is the reduction of each resistance such as the base resistance \((r_b)\) and the emitter series resistance. In order to reduce series resistances, polysilicon electrodes should be covered by silicides or refractory metals /49/. Concerning the base resistance, the intrinsic base resistance is the most dominant in the case of the self-aligned structures. The intrinsic base resistance is dependent on the base doping and the base width which also affect the cutoff frequency. So, the base profile must be optimized for the moderate intrinsic base resistance and high enough cutoff frequency without suffering from forward biased tunneling and punchthrough. The emitter series resistance, which is dominantly a contact resistance associated with the polysilicon emitter contact, should be kept small when the emitter area is decreased to sustain the sufficient cutoff frequency. For this purpose nearly recrystallized extended polysilicon emitter with a silicide contact is quite suitable.

Fig.3 shows the schematic cross-section of a future bipolar device structure. The BJT itself is fully isolated by the trench-isolated SOI structure. Both the polysilicon electrodes for the base and the emitter are covered by silicides or refractory metals, and the polysilicon emitter is a nearly single-crystallized extended emitter. The lateral device dimensions are optimized to achieve the best valance between the base resistance and the base-collector capacitance avoiding the extrinsic base encroachment problem. The vertical profiles are also optimized for the emitter junction depth to avoid the narrow emitter effect and for the base junction depth to optimize the intrinsic base resistance and the cutoff frequency. In order to reduce the Kirk effect the collector doping profile should be tailored. Fig.4 is an example of such doping profiles of both the intrinsic and extrinsic base regions.

According to the two-dimensional physical DC and AC device simulation /50/ based on the device structure of Fig.3 and the impurity profiles of Fig.4, the cutoff frequency, the base-collector capacitance, and the AC base resistance were estimated. Fig.5 shows the cutoff frequency \((f_T)\) versus the collector current \((I_c)\) characteristics as well as the current gain dependence upon \(I_c\). Maximum \(f_T\) of 56 GHz at the collector current of 0.3 mA/um is obtained and more than 50 is achieved at the same time as shown in Fig.5. Fig.6 shows the base-collector capacitance \((C_{bc})\) and the AC base resistance \((r_{bb'})\) versus \(I_c\), where \(C_{bc} \) of 1.1 fF/um and \(r_{bb'} \) of 550 ohm/um are obtained at the small collector current. From these results the basic gate delay time of a typical ECL circuit \((F.I.= F.O. = 1)\) is estimated at least below 20 ps at a switching current of 0.3 mA/um in a condition of room temperature. If much lower temperature operation such as 77K is considered, the logic swing can be reduced without suffering from the decrease of circuit noise margins. In this case not only circuit designing but process conditions e.g. the doping profiles should be optimized /51,52/. Low temperature operation can achieve the lower power dissipation; the enhancement of cooling efficiency, lower wiring resistances and longer MTF of wiring metals. All of these properties are quite suitable for ULSI chips that consist of ECL-type circuits.

When the basic gate delay time reaches around 20 or 30 ps, the most serious problem is the loaded wiring delay time owing to the wiring capacitances which are physically limited. ECL-type circuits are the best solution for driving large loaded capacitances whereas they are always accompanied by the large power dissipation. Low temperature operation is advantageous to relax this problem, while it is strongly dependent on the system and circuit designing strategy. Accordingly, the optimization of cost and performance valances in the total system designs including the software, the hardware and the individual chips are the key features for the system development in the future.

6 - SUMMARY

Today's advanced bipolar device structures, their problems and future trends have been reviewed. The major role of bipolar devices has focused on ECL-type circuits. In order to reduce the switching time and the power dissipation, the double polysilicon self-aligned structures combined with trench isolation have become the major structure. For further improvement RC time constants associated with the silicon substrate should be reduced, which can be achieved by wafer direct bonding SOI techniques. Low temperature operation should be be considered although it is strongly dependent on the system designing strategy. Basic gate delay times now have little influence because loaded wiring delay times are by far larger. The total cost and performance valances of the system designs are the key features for the future system development.
Fig. 3 - Ultimate future Si BJT structure. Effective quarter micron figures of the lateral dimension are considered. Nearly single crystallized 0.1-um thick extended polysilicon emitter is also assumed. (The vertical dimension is not in proportion to the lateral one.)

Fig. 4 - Example of doping profiles corresponding to the device structure in Fig.3. $N$ is the impurity concentration. The maximum ionized impurity concentration is limited by $1.0 \times 10^{20}$/cc.
Fig. 5 - Cutoff frequency \( f_T \) and current gain \( h_{FE} \) versus collector current \( I_c \) at \( V_{ce}=3V \). The emitter width is standardized by 1.0 \( \mu \text{m} \).

Fig. 6 - Base-collector capacitance \( C_{cb} \) and AC base resistance \( r_{bb'} \) versus collector current \( I_c \) at \( V_{bc}=0V \). The emitter length is also standardized by 1.0 \( \mu \text{m} \).
REFERENCES