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MAXIMUM OPERATING VOLTAGE LIMITATIONS DUE TO PARASITIC BIPOLAR ACTION IN VLSI CMOS

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Abstract-The influence of the PBTA (Parasitic Bipolar Transistor Action) induced by impact ionization on the maximum operating voltages as well as on the isolation performance in VLSI CMOS structures was investigated using the sensitivity of the nMOS- and bipolar-parameters to the operating voltages.Strong coupling between the MOS- and bipolar-currents exists due to the potential drop caused by the impact ionization currents of the nMOSFET.The base currents of the bipolar transistors reduce the measurable substrate current.The maximum operating voltage in CMOS is limited by the impact ionization induced PBTA.The isolation performance is reduced by the collector current of the vertical transistor.

1. INTRODUCTION

The driving force to reduce dimensions in VLSI is to increase the speed and the packing density of the circuits. The main difficulty in scaling down CMOS designs in the future will be the reduction of the effective channel length $L_{\texttt{eff}}$ of the MOSFETs and the n⁺/p⁺ isolation spacing between them. By reducing $L_{\texttt{eff}}$, the breakdown properties of the MOS transistors are affected. Reducing the n⁺/p⁺ spacing will affect the electrical separation between the n- and p-MOSFETs.

When scaling down to submicron levels at constant operating voltages, the electric field in the channel and the related impact ionization rates increase rapidly. The potential drop ΔV_{BB} produced by the impact ionization currents in the electrical substrate of the nMOSFET gives rise to Parasitic Bipolar Transistor Action (PBTA). The resulting bipolar current is an injection current. It increases exponentially with ΔV_{BB} (≈1 decade/60 mV). The PBTA leads to interactions between the currents of the n- and p-channel areas that can be enhanced by the positive feedback of the npn and pnp bipolar transistors in CMOS.

Although potential drops ΔV_{BB} below 0.6V will only lead to relatively low bipolar currents, they can significantly influence the MOS currents and the isolation between the well and the substrate. The MOSFET parameters are affected by the impact ionization dependent change of the back gate bias V_{BB} and by the bipolar current $I_{\rm E}$ injected from the source of the nMOSFET. The isolation performance is then affected by the collector current of the npn transistors. The result is a limited operating voltage and a reduced isolation performance.

The purpose of this work was to investigate the influence of the impact ionization induced PBTA on the maximum operating voltage of the nMOSFETs and on the isolation performance in CMOS.Experiments were carried out on samples fabricated in p-well based twin-tub CMOS processes with 1.0µm to 1.5µm feature sizes and gate oxide thicknesses from 20nm and 25 nm, respectively.

2. MAXIMUM OPERATING VOLTAGE

Fig.1 shows the cross sectional view of a p-well CMOS structure with the nchannel MOSFET, the parasitic npn bipolar transistors and the current generator $I_{1 \circ n}$ representing the impact ionization current. At sufficiently large potential drop ΔV_{BB} caused by $I_{1 \circ n}$, electrons are injected from the n⁺ source into the p-well leading to PBTA.Since the emitter efficiency of the n⁺ area is very high, two effective npn parasitic bipolar transistors contribute to the injection current. The consequences of the PBTA in p-well CMOS can become increasingly important considering the voltage limitations and the hot carrier degradation of the nMOSFETS.



Fig.1:Cross sectional view of the test structure with MOSFETs, parasitic bipolar transistors and the current generator I_{ion} .

The lateral npn transistor can cause the well known drain induced barrier lowering (DIBL) for short channel lengths. It represents a drain to source voltage limitation for the nMOSFET.

The vertical npn transistor can cause:

* A reduction of the isolation between p-well and n-substrate due to its collector current.

* A reduction of the maximum operating voltage $V_{DD}=V_{CE}$ for a CMOS relevant functional unit (to retain the same current levels in the well and the substrate as without PBTA).

* A reduction of the maximum operating voltage V_{DS} of the nMOSFET because of an enhanced injection from the source. An increased injection of electrons from the source leads to increased drain current due to the attraction of the injected electrons by the gate field. An increased drain current leads to an increased impact ionization and thus to a positive feedback.

The two basic conditions for starting PBTA are: the impact ionization current $I_{1\circ n}$ and a certain collector to emitter voltage $V_{CE}=V_{DD}$. The current $I_{1\circ n}$ is determined by the operating point of the nMOSFET e.g. V_{GE} , V_{DS} and V_{BB} . V_{CE} is the CMOS relevant operating voltage V_{DD} . The degree of the V_{DS} and V_{DD} limitations by the PBTA will be demonstrated by the dependences of the more important MOSFET parameters on the operating voltages.



Fig.2:Influence of the operating voltages on nMOST-and CMOSparameters.Fig.2a:substrate current I_{BB} , normalized by I_{BB} at $V_{CE}=V_{DS}=6.4V$ vs. V_{CE} . Fig.2b:the maximum operating voltage V_{DD-max} vs. V_{GS} for different V_{DS} .

The normalized substrate current of the nMOSFET as a function of the operating voltage $V_{CE}=V_{DD}$ for different gate voltages V_{GS} at $V_{DS}=6.4V$ is shown in Fig.2a. The normalizing factor is the substrate current at $V_{CE}=V_{DS}$. The filled circles for each gate voltage correspond to the condition that injection from the source occurs. This condition is verified by measuring the

drain and source currents of the nMOSFET. The first filled circle going to higher V_{CE} voltages for each V_{GS} indicates the condition at which the value of the source current becomes just equal to the drain current. The last value of V_{CE} before injection represents the maximum operating voltage V_{DD-max} for the given CMOS structure. At low gate voltages the substrate current (=current in the p-well) of the nMOSFET is very low too so that it results in a high relative change.Increasing V_{GS} , injection occurs at lower $V_{CE}=V_{DD}$ voltages indicating a respective operating voltage limitation.



Fig.3:Operating voltage-sensitivities of the collector current I_{c} (Fig.3a) and of the n-channel substrate current I_{BB} (Fig.3b) as a function of V_{GS} .

Fig.2b shows the maximum operating voltage V_{DD-max} as a function of the gate voltage V_{GS} for different V_{DS} voltages of the nMOSFET.The shape of the V_{DD-max} curves reflects the well-known substrate current shape for all drain voltages V_{DS} . V_{DD-max} decreases with increasing V_{DS} .

The collector current of the vertical npn bipolar transistor I_c , the substrate and the drain currents I_{BB} and I_D of the nMOSFET characterized by their sensitivities to $V_{CE}=V_{DD}$ as a function of the V_{GS} for different V_{DS} voltages are shown in Fig.3a, 3b and Fig.4, respectively.



Fig.4:Sensitivity of the n-channel drain current vs.V_{GS} for different V_{DS} .

Fig.3a shows that injection occurs only for $V_{DS} \ge 6.5 V$. The curve follows the V_{GS} -dependent substrate current shape.Even at $V_{DS} = 6.5V$ the injection from the source is significant only in that gate voltage range where the substrate current is sufficiently high. Below $V_{DS} = 6.5V$ no injection into the substrate takes place.The nMOST parameters in this case are influenced by the body effect changing the threshold voltage V_T .Due to the modulation of the depletion width at the well/substrate junction,the well resistance R_W and thus the potential drop ΔV_{BB} are modulated too.

The influence of the PBTA on the substrate and drain currents is demonstrated in Fig.3b and Fig.4. Without injection (circles) both substrate and drain sensitivities are increased when V_{DS} is increased. With injection (filled circles) both substrate and drain sensitivities are reduced. The reduction can be estimated from the difference between the dashed line (i.e.the curve approximated from points without injection) and the measured curve in the V_{GS} range where injection occurs. The I_{BB} reduction shows clearly that a part of C4-390

the impact ionization current I_{ion} is consumed by the base current of the npn transistors. Therefore the impact ionization in MOSFETs will be underestimated using the measurable I_{BB} to monitor it. The reduction in I_D is a consequence of the decreased voltage drop ΔV_{BB} caused by the reduced I_{BB}.

3. ISOLATION PERFORMANCE

The influence of the PBTA on the isolation performance of a CMOS relevant functional unit e.g. inverter is demonstrated in Fig.5a. The substrate currents of the n- and p-channel MOSFETs in the inverter circuit , I_{BBn} and Currents of the n- and p-channel MOSFETS in the inverter circuit I_{BBn} and I_{BBp} , respectively are shown vs. the input voltage V_{IN} . The regular substrate currents I_{BBn} and I_{BBp} generated by impact ionization in the respective MOSFETs are denoted by solid lines. However, an additional peak of the I_{BBp} is observed (denoted by dashed lines). This is the collector current of the vertical npn transistor. Preventing PBTA by reverse biasing the p-well/source invertice. junction, the additional peak disappeares (dotted line).

The maximum values of the additional peaks for different doping levels in the p-well vs.Vpp are shown in Fig.5b. Reducing the PBTA by increasing the Gummel number, the collector currents I_{BBP} are reduced effectively.



Fig.5:Substrate currents of the MOSFETs in a CMOS inverter.Fig.5a:IBBn and I_{BBp} vs.V_{IN}.Fig.5b:Maximum values of the additional peaks I_{BBp} normalized by the channel width W vs. V_{DD} for different doping levels in the p-well.

CONCLUSIONS

(a)

Voltage drops ΔV_{BB} below .6V caused by impact ionization currents in the electrical substrates of the respective MOSFET's lead to PBTA in VLSI CMOS. This action results in limitations of the maximum operating voltages of the discret MOSFETs and of the CMOS functional unit. These influences were investigated using operating voltage- sensitivities of the MOS- and bipolar-currents.

The obtained results demonstrate clearly that:

* The nMOSFET- and the bipolar-currents in CMOS are strongly coupled by the potential drop caused by the impact ionization currents.

* The maximum operating voltage in CMOS is limited by the PBTA induced by the operating point dependent impact ionisation in nMOST.

* Any increase of the well-doping effectively reduces this effect. * The base currents of the parasitic bipolar transistors reduce the measurable substrate current of the corresponding MOST.

* The isolation performance of a functional unit in CMOS is reduced due to the collector current of the vertical bipolar transistor.