HIGH VOLTAGE SWITCHING P-CHANNEL STRUCTURE FOR CMOS ARCHITECTURES

C. Mori, G. Crisenza, P. Picco

JOURNAL DE PHYSIQUE
Colloque C4, supplément au n°9, Tome 49, septembre 1988

HIGH VOLTAGE SWITCHING P-CHANNEL STRUCTURE FOR CMOS ARCHITECTURES

C. MORI, G. CRISENZA and P. PICCO

SGS-Thomson Microelectronics, Via C. Olivetti 2, I-20041 Agrate (MI), Italy

RÉSUMÉ

On presents ici l'analyse d'une structure à canal p à haut voltage complétement compatible avec toutes les architectures CMOS. Elle met en évidence le rôle critique joué par la couche du "drain extension" sur la prestation électrique du dispositif et par l'épaisseur de l'oxyde de champ périphérique sur la fiabilité du dispositif. Ces résultat sont utiles pour dessiner des dispositifs à haut voltage avec un procés compatible dans une technologie CMOS avancée.

ABSTRACT

An analysis of a P-ch High Voltage structure fully compatible with all CMOS architectures is presented. It points out the critical role played by drain extension layer on electrical device performance, and by the field thick oxide periphery on the device reliability. These results are useful in designing HV process compatible devices in advanced CMOS technology.

1 Introduction

The electronic evolution towards submicron dimensions finds an important constraint in the compatibility with existing systems. Many of these must be supplied with voltages greater than the maximum voltages allowed for scaled circuits, but must often be directly interfaced to them. Hence, the problem of designing and characterizing High Voltage MOS devices compatible with submicron technologies must find an increasing interest [1,2].
Luckily, the general trend from NMOS to CMOS technologies introduces some degrees of freedom to build-up new, not standard structures, which may be useful for high voltages.
But unluckily, the well known technological tricks to produce low-threshold MOS devices weaken the structure with respect to HV effects, and especially with respect to hot electron effects.
In this paper we examine a particular, self-aligned P-ch structure compatible with all CMOS processes. We consider its evolution on different process generations, and after technological and electrical simulations, we identify the critical points and some design criteria for such a structure in the advanced processes.

2 P-channel structure

Three main effects limit the HV perfomances in a MOS structure: the thickness of the gate oxide over the drain junction, the drain dopant concentration and the curvature of the drain junction.
The P-ch structure shown in Fig.1 is an optimization of these three points with respect to an usual P-ch structure. The oxide over the drain junction is the field oxide, the thickest one available in the process. The transistor drain extension is made by P-isolation implant, at least two order of magnitude less doped than normal P^+ drain. The junction curvature is softed by the long diffusion necessary for field oxide (LOCOS) growth.
The interest of this structure resides in the fact that it is the only structure compatible with both P- and N-well CMOS technologies, since it is based on P-isolation, i.e. the P-type channel stopper necessary in both types of architectures. In the shown section an N-well technology has been chosen, but the only difference with P-well technology is that in the latter the transistor is embedded in the N-type substrate instead of in the N-well.

In any case, the P-iso layer determines the transistor performance. To improve it, the P-iso sheet resistance ought to be reduced by increasing its doping density. This induces a (process compatible) increase in N-ch parasitic threshold, but might equally induce an excessive lowering of N^+/P-iso junction breakdown on N-ch devices [3].
At the first glance, the device optimization looks to be simply to find the best compromise of opposite requirements. But other structural parameters must be taken into account.

3 Experimental

The P-channel structure has been simulated by using the program *TITAN* [4] and performed on silicon in two different processes, according to the scheme shown in Tab.1, to verify the suitability to be scaled down in different process generations and to verify the full compatibility with the assigned process architecture (no extra mask, ion implant or thermal treatments). Both these processes are CMOS: Process 1 is P-well based and its typical gate length is 3μm; Process 2 is N-well based and its typical gate length is 1.5μm.
In Fig.2 a comparison is made between the output characteristics of HV P-channel structure and the output characteristics of a standard P-ch transistor of same length achieved by the same process.
But since reliability is a major concern when strong electric fields are involved, a main parameter to be carefully taken into account is the drain/channel overlap [5,6], i.e. the encroachment between the P-iso and the thin oxide region, simulated in Fig.3 according to the process schemes given in Tab.1.
Fig.4 shows the substrate parasitic currents for transistors produced by Process 1 and Process 2. It is worthwhile to note that the bell-shaped curve is associated with the structure that in Fig.3 results well overlapped (Process 1), while the diverging current is related to the not overlapped structure (Process 2).
After considering these currents, it is straightforward to consider the degradation of the Process 2 transistor. The Fig.5 shows that no degradation occurs on the not overlapped transistor.

4 Discussion

In the general trend of CMOS processes towards thinner oxides and tighter design rules, the described experimental data show the critical role played in the discussed HV device not only by P-iso layer, but also by the LOCOS bird's beak shape.
P-iso sheet resistance is critical in determining the transistor gain and current drive capability [7]. Its effects are apparent in the output curves of Fig.2: the decrease of current drive capability is heavier for Process 2 (10 kΩ/$\square$ P-iso layer) than for Process 1 (3 kΩ/$\square$ P-iso layer), while the device reliability more strongly feels the shape of LOCOS beak.
From the beak height/width ratio F the drain/channel encroachment strongly depends. For the considered Process 1 and Process 2 HV transistors, the different Nitride/Pad oxide ratio, and the different field oxide growth conditions, produce different LOCOS beak shapes. The different shape produces the different P-iso/channel overlap of Fig.3, and this produces the different substrate currents shown in Fig.4.
The unexpected and important effect found in this work, i.e. the absence of degradation on the non overlapped transistor, is just explained by considering the LOCOS beak shape and the underlying region. If the beak is very steep as in Process 2 (F=3, in contrast to Process 1, where the shape is very soft (F=1)), an almost vertical gap exists between the channel region and the lateral P-iso diffusion. This gap is not controlled by the gate voltage (then substrate current diverges, Fig.4), the maximum electric field is not close to the thin gate oxide but it is deeper in the semiconductor. This inhibits any charge injection into the gate oxide, then inhibiting device degradation too.
The correctness of this interpretation is confirmed by considering the Fig.6, that shows the degradation occurring on a normal P-ch transistor achieved by Process 2, after a stress comparable to that performed on the HV transistor. For this normal P-ch transistor, the gate oxide thickness is the same as for the HV transistor, body concentration is the same, and there is evidence of a

positive drain/channel overlap (see Fig.7), but a 15% degradation occurs. The reason is that the maximum electric field is close to gate oxide, so that charge injection may occur.

5 Conclusions

A HV P-ch structure has been shown and discussed on different CMOS processes. Its reliability has been related to the local physical characteristics of and under the LOCOS periphery. This structural element is of increasing importance in the general process trend towards thinner oxides, for which reliability is a major concern.

REFERENCES

1. Z.Parpia,C.A.T.Salama,R.Hadaway, IEEE Trans.El.Dev..34,2335(1987)
2. V.Rummenik,D.L.Heald, IEDM 1982, 77
3. S.Ochi,T.Okabe,I.Yoshida,K.Yamaguchi,M.Nagata, IEEE Trans.El.Dev., 27.399 (1980)
4. A.Gerodolle,S.Martin, TITAN 4 2D PROCESS SIMULATION, CNET GRENOBLE (1987)
5. P.K.Ko,T.Y.Chan,A.T.Wu,C.Hu, IEDM 1986,292
6. T.Mizuno,Y.Matsumoto,S.Sawada,S.Shinozaki,O.Ozawa, IEDM 1985,250
7. J.G.Mena,C.A.T.Salama, Sol.St.El.,29,647(1986)

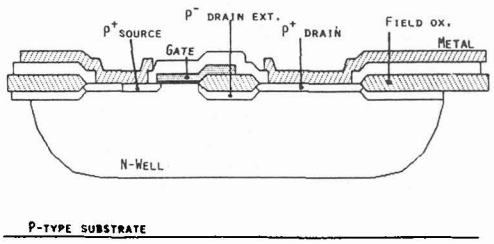

Figure 1: HV switching P-ch structure for N-well CMOS architecture.

Tab.1

	Process 1	Process 2
Transistor body concentration	8 10^{15} cm^{-3}	1.6 10^{16} cm^{-3}
Nitride thickness	3000 Å	1900Å
Pad oxide thickness	900 Å	100Å
P-iso ion dose	7 10^{13} cm^{-2}	2 10^{13} cm^{-2}
P-iso energy	40KeV	25 KeV
Field oxide growth	1000°C 260'wet	1000°C 160'wet
Field oxide thickness	9500 Å	7000Å
Gate oxide growth	875°C 48'wet	800°C 100'wet
Field oxide thickness	700 Å	330Å
Threshold shift dose	1 10^{11} B cm^{-2}	5 10^{11} BF_2 cm^{-2}
Threshold shift energy	40KeV	60 KeV

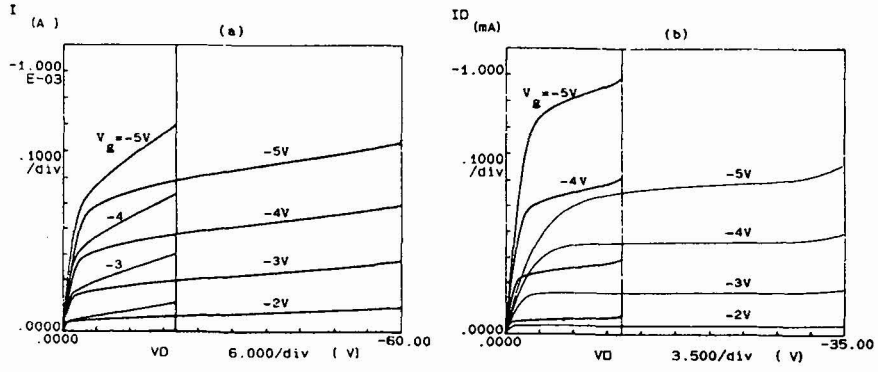

Figure 2: Output curves for Process 1 (a) and Process 2 (b) HV transistors.

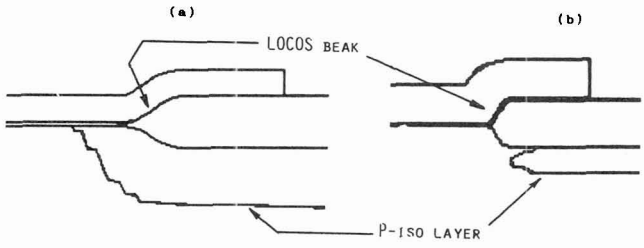

Figure 3: Drain-channel overlap in Process 1 (a) and Process 2 (b) HV transistor.
Note, in (b), the almost vertical gap between channel and P-iso layer.

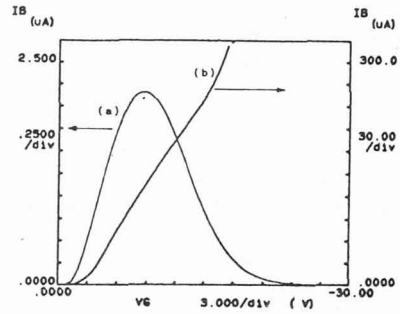

Figure 4: Substrate current vs gate voltage for Process 1 (a) and Process 2(b) HV transistors.
For (a) L_{eff}= 5 μm
For (b) L_{eff}= 3 μm

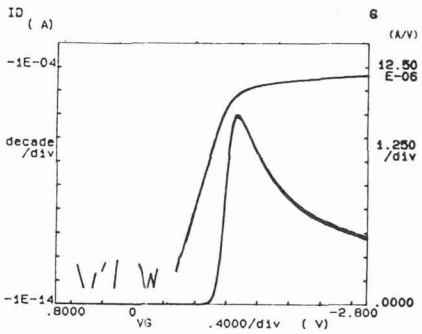

Figure 5: Process 2 HV transistor.
Comparison of I_D current (also in subthreshold region) and transconductance before and after voltage stress: no difference is appreciable.

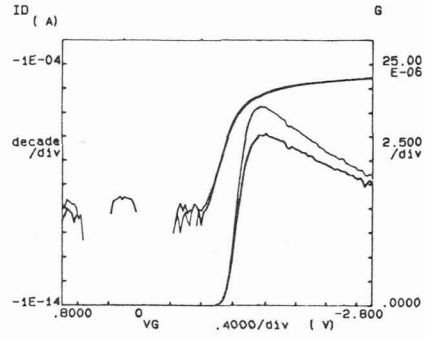

Figure 6: Process 2 std not HV transistor.
Comparison of I_D current (also in subthreshold region) and transconductance before and after a voltage stress comparable to that performed on H.V. transistor.
The gain (G) degradation is apparent.

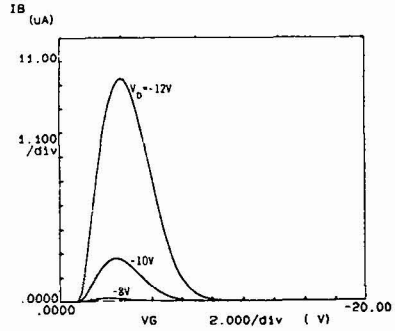

Figure 7: Substrate current of Process 2 std not HV transistor.