A NOVEL METHOD FOR DIMENSIONAL LOSS CHARACTERIZATION

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Abstract. *The present tendency toward devices scaling in VLSI technology makes more and more difficult the electrical characterization of channel dimensions.*
The narrow channel effects have had a great consideration for what concern device modeling, but a minor attention about dimensional loss problems. The aim of this work is to propose an effective width characterization method based on transconductance and not affected by the typical problems related to narrow channel devices.
Moreover, a compared analysis of this method to an other one previously proposed [1] is shown pointing out the phenomenological differences.

1 Introduction

In 1 μm processes development the active areas pitch scaling is not necessarily associated to an adequate scaling of the isolation process.
For EPROM devices the dimensional losses induce poor current and speed performances and the possibility of a marginal verification of the memory cell.
For this reason it is useful the implementation of a reliable electrical evaluation of the effective channel width of a MOST to control the process; moreover the evaluation method must be independent from the process variations.

2 Experimental and results

The measures were carried out on two sets of n-channel transistors with 280Å gate oxide thickness, polysilicon gates and ion implantation process.
The first set was constitued by native and enhancement mode devices with a channel stop implant of 6.5×10^{12} cm^{-2} and has been treated at a temperature of 920 °C (low T); the other set was in the same mode with a channel stop implant equal to 7.5×10^{12} cm^{-2} and treated at 1100 °C (high T).
The threshold shift implant was equal to 7×10^{11} cm^{-2} for both sets and the substrate concentration was 7×10^{15} cm^{-3}.
The channel length was 10μm for all the samples and the width varied between 2.6μm and 1.0μm with a W_{step} equal to 0.2μm.

We are interested in the evaluation of the MOST effective geometrical width W_{eff}, that is by definition the width of the active area below the gate oxide and delimitated by the bird's beak.
The selective oxidation by Si_3N_4 pattern permits the field oxide penetration under the Si_3N_4 itself; for this reason the final active area dimension will be less than the one on mask.
Now we can consider the behavior of drain current of a MOST operating in the linear region:

$$I_d = \frac{W_{eff}}{L}\mu C(V_g - V_t)V_d$$

where $W_{eff} = W_{nom} - \Delta W$
W_{eff} is the active area width covered by the gate oxide and limited by the bird's beak, ΔW is the dimensional loss and W_{nom} is the dimension on mask.
By plotting the drain current values as a function of W_{nom} for a set of constant length MOS devices and choosing the best straight line, the value of ΔW is determined as intersection with the W_{nom} abscissa.
In order to avoid the narrow channel effects on threshold voltage it is advisable to apply a $V_g \gg V_{th}$ [1].
In figure 1 we show the application of the method with V_{gs} as a parameter; it is evident the strong dependence of ΔW by the gate voltage value.
On the other hand the dependence of the I_d method by temperature treatments is shown in figures $2(a, b)$ where the SEM analysis results of the dimensional loss are reported as a comparison.
This behavior is explainable with different diffusion profiles of channel stop implant; in fact we can consider the real MOST as a parallel of an ideal transistor with $W = W_{eff}$ and a "parasitic" one whose gate oxide is the bird's beak and the isolation implant is the threshold implant.
To understand the behavior of the narrow channel MOST it is useful to plot the I_d and the trasconductance (beta) against gate voltage. In figure 3 the curves of low T n-channel native transistor are shown; it can be noted the beta canonic shape.
Viceversa when we get an high T treatment of the isolation implant the drain current grows almost linearly with V_{gs} as showed by the constant beta value also for high gate voltage values (fig.s $4.a, b$); this effect is stronger for the enhancement mode device as reported in fig.$(4.b)$.

3 Transconductance method

By considering the previous results we can summarize the following considerations:

- the enhancement transistor presents a more evident drain current contribution of the bird's beak parasitic than the native one; this is due to the similarity of the two "parallel" devices threshold voltages (fig.s $4.a, b$) and is enhanced by an higher T treatment on channel stop implant;
- the transconductance *plateau* is induced by the"parasitic" contribution compensating the mobility loss;
- in figure 5 the mobility loss gets over the parasitic when V_{gs} is higher than $4 \div 5$ Volts.

Avoiding the effect described above we implemented the transconductance measure in the same way as we treated the drain current, that is by plotting the maximum beta versus W_{nom}.
The implementation of this method is shown in figures 6 and 7; in both cases we measured native and enhancement transistors where in fig.6 the samples were.treated at low T, while in fig.7 at high T.
As we can see in the insert the agreement with SEM analysis is good.
This method is more precise than the I_d one because it permits to identify the same channel status (the strong inversion beginning) irrespectively of the threshold voltage. Because we check the beta maximum, the problem connected with the non-linear effect of V_{gs} on mobility is no more a constraint.

4 Conclusions

The method presented and based on transconductance seems to be quite reliable because it overcomes the problems related to mobility saturation [2], narrow channel effects, threshold voltage and isolation process.
We have outlined the problems connected with the drain current method pointing out the behavior of the narrow channel devices.

References

[1] Ying-Ren Ma et al.(IEEE TRANS. ON ELECTRON DEV.,VOL.ED-29,NO.12, DEC.1982).
[2] P.Wang (IEEE TRANS. ON ELECTRON DEV.,VOL.ED-25,NO.7,JULY 1978).
We thank A. Maggis of S.T. for the useful discussions and suggestions.

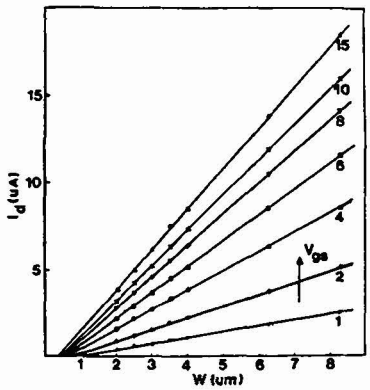

Fig.1 - I_d vs. W_{drawn} with V_{gs} as a parameter for n- channel enhancement transistor.
[Gate length 10μm]

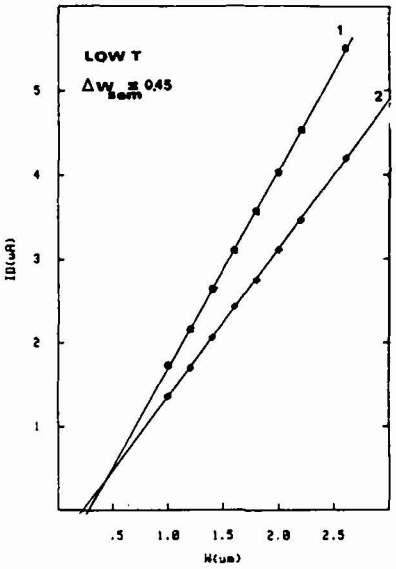

Fig. 2.a - I_d vs W_{drawn} on native (a) and enhancement (b) transistors for low Temperature treatment (920 C).
[V_{gs}= 3 V native - V_{gs}= 5 V enhanc.]
[Gate length 10μm]

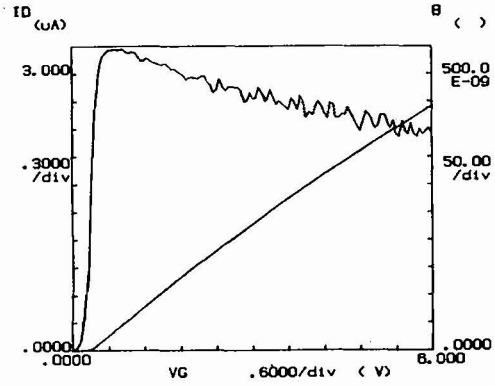

Fig. 3 - Threshold voltage and transconductance characteristics against gate voltage for native n-channel transistor at low T.
[W_{drawn} = 1μm, L = 10μm]

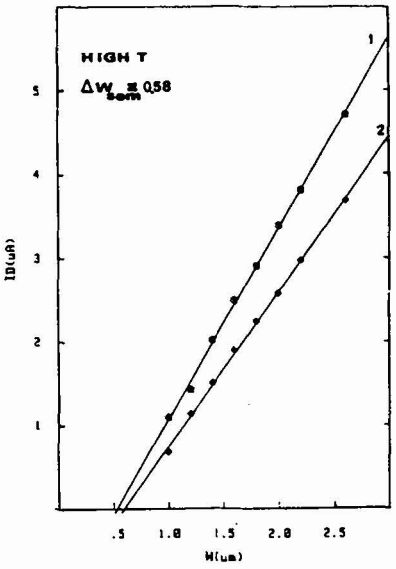

Fig. 2.b - I_d vs W_{drawn} on native (a) and enhancement (b) transistors for high Temperature treatment (1100 C).
[V_{gs}= 3 V native - V_{gs}= 5 V enhanc.]
[Gate length 10μm]

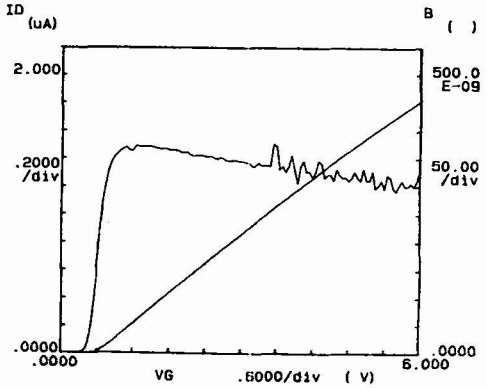

Fig. 4.a - Threshold voltage and transconductance characteristics against gate voltage on n-channel native transistor at high T.
[W_{drawn} = 1μm, L = 10μm]

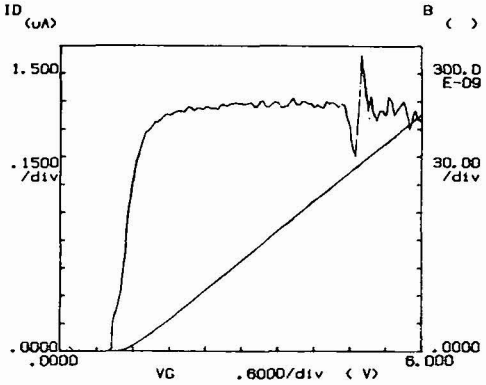

Fig. 4.b - Threshold voltage and transconductance characteristics against gate voltage on n-channel enhancement transistor at high T.
[W_{drawn} = 1μm, L = 10μm]

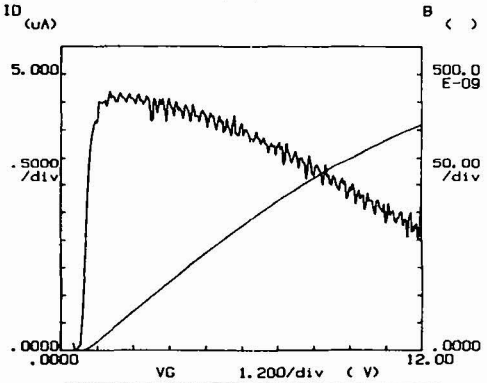

Fig. 5 - Threshold voltage and transconductance characteristics on n-channel transistor till high V_g, values (high T treatment).
[W_{drawn} = 1μm , L = 10μm]

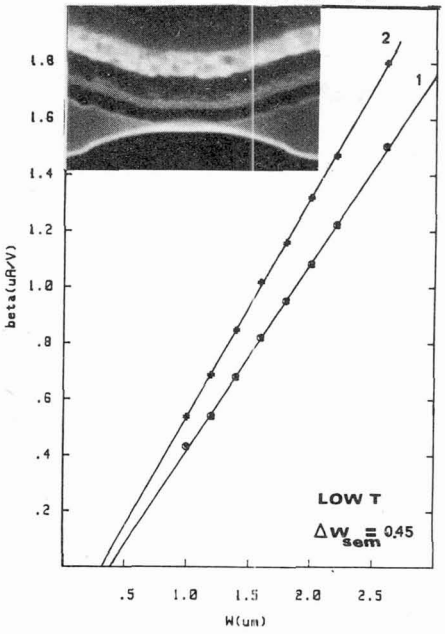

Fig. 6 - Transconductance versus W_{drawn} for n-channel native (1) and enhancement (2) transistors.
The SEM cross section is reported in the insert [21K magnification].

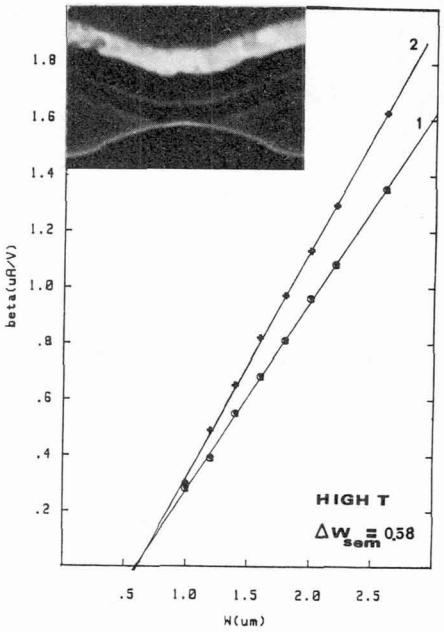

Fig. 7 - Transconductance versus W_{drawn} for n-channel native (1) and enhancement (2) transistors.
The SEM cross section is reported in the insert [21K magnification].