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JOURNAL DE PHYSIQUE
Colloque C4, supplément au n°9, Tome 49, septembre 1988

DEGRADATION OF SHORT-CHANNEL MOS TRANSISTORS STRESSED AT LOW TEMPERATURE

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Résumé - Nous étudions le vieillissement à 77 K de transistors MOS de type N soumis à de fortes contraintes électriques: tension de drain V_d = 5,5 V et tension de grille V_g variant de 1,5 à 6,5 V. Nous montrons que les maxima de la dégradation de transconductance et du décalage de la tension de seuil ne se manifestent pas pour les mêmes conditions de contrainte. Les résultats sont expliqués par la nature plus ou moins localisée des défauts créés qui est aussi responsable de la distorsion des courbes de transconductance et de son augmentation temporaire lors du vieillissement. Une augmentation inhabituelle de la transconductance en régime de saturation est également mise en évidence.

Abstract - Hot-carrier stressing was carried out on 1 µm n-type MOSFETs at 77 K with fixed drain voltage V_d = 5.5 V and gate voltage V_g varying from 1.5 to 6.5 V. It was found that the maximum transconductance degradation and threshold voltage shift do not occur at the same V_g. This behavior is explained by the localized nature of induced defects which is also responsible for a distortion of the transconductance curves and even a slight temporary increase in the transconductance during stress. An anomalous increase in the saturation transconductance is also reported.

1 - INTRODUCTION

The hot carrier induced degradation is known to be more accentuated for MOSFET operation at low temperature but most of the experimental work was carried out at 300 K. Recent papers show a lack of concordance concerning the physical mechanisms involved in the device degradation at 300 K and 77 K (generation of interface states /1/ or charge trapping /2/). In relatively long MOSFETs, maximum degradation occurs for a given drain voltage V_d when the gate voltage V_g is approximately $V_d/2$ (maximum substrate current) /3/.

In this work, we study the defect nature and localization in short channel n-type MOSFETs subjected to high-field stressing at 77 K by regarding threshold voltage V_t shift and changes in the transconductance G_m value and shape. Both the linear region and saturation region are reported. Some particularities in the transconductance behaviour of stressed devices are discussed for the first time.

2 - EXPERIMENT AND RESULTS

The devices used were conventional n-channel MOSFETs with effective channel length $L_{eff} \approx 1$ µm, channel width W = 20 µm and oxide thickness t_{ox} = 25 nm fabricated at LETI Laboratories in Grenoble (France). The devices were directly immersed in liquid nitrogen and stressed at a fixed drain voltage V_d = 5.5 V and various gate voltages V_g. The device characterization was performed at 77 K and 300 K, before and after stress, by using HP 4145B Analyzer. We measured the drain current $I_d(V_g)$ and transconductance $G_m(V_g)$ characteristics in the linear (V_d < 100 mV) and saturation region with both forward and reverse modes of operation, the substrate current and the subthreshold slope. V_t was determined at I_{ds} = 0.2 µA/µm of channel width or by extrapolating the linear $I_d(V_g)$ curve.

The transconductance reduction rate $\Delta G_m = (G_{mo}-G_m)/G_{mo}$ and threshold voltage shift $\Delta V_t = V_t - V_{to}$ occuring after one hour stress is presented in Fig. 1. Here G_{mo} and V_{to} denote pre-stress values. We notice that maximum ΔV_t and ΔG_m do not occur at the same V_g : ΔV_t is very small for the $V_g < V_d$ stressing, becomes significant at $V_g \approx V_d$ and then rapidly increases with increasing V_g, while ΔG_m has its maximum in the region of maximum substrate current.

Although for $V_g < V_d$, the degradation rate follows roughly a law of $\Delta G_m \propto t^{0.25}$, the behaviour for $V_g > V_d$ stressing is more surprising ; a temporary increase in G_m is found after 10^4 sec of stress (Fig. 2a). This transconductance "overshoot" is also clearly seen in $G_m(V_g)$ curves (Fig. 2b). Very similar curves have been obtained by 2-D simulation /4/ for the case where generated defects are localized in a region of ΔL = 0.15 µm close to the drain and explained by a two-piece model : the total transconductance of the stressed MOSFET may be dominated by that of the defective region ΔL which has a higher threshold voltage but a much shorter length compared to the defect-free region. Our results offer the first experimental support for the predictions of a transconductance overshoot during the transistor aging.

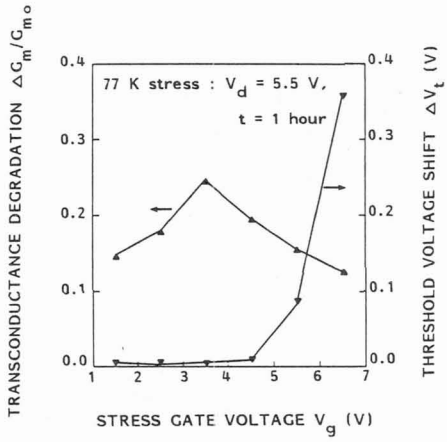
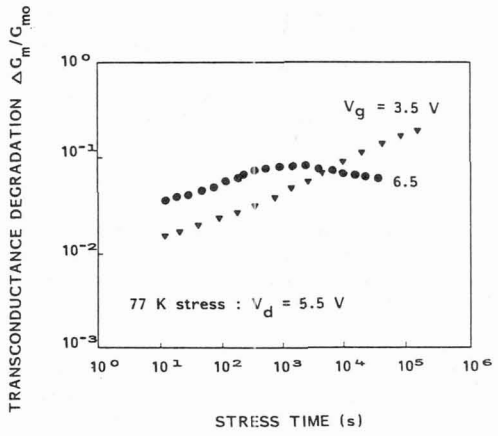


Fig. 1 - Maximum transconductance degradation and threshold voltage shift versus stress gate voltage after 1 hour's stress at 77 K with V_d = 5.5 V.



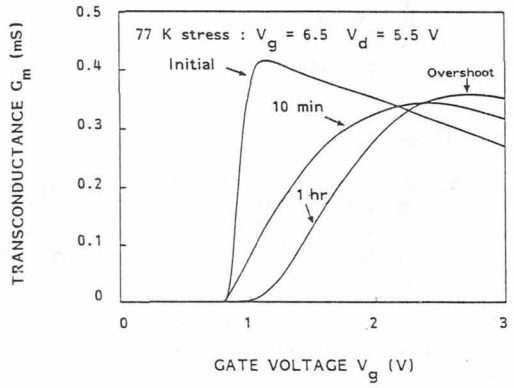


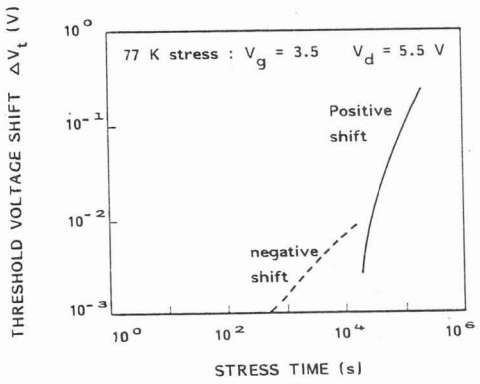
Fig. 2a - Maximum transconductance degradation versus stress time for two typical stress conditions.

Fig. 2b - Transconductance versus gate voltage characteristics of a device stressed at V_d = 5.5 V and V_g = 6.5 V; measurement at 77 K with V_d = 50 mV and stress time as a parameter.

For $V_g < V_d$, we observe first a slight negative shift in the extrapolated V_t followed by a discontinuous transition to positive shifts (Fig. 3a). The negative ΔV_t may be misinterpreted as being due to the generation of positive charge. We propose another explanation based on the fact that V_t depends also on the slope of $I_d(V_g)$ curve /5/ :

$$V_t = V_{gmax} - \frac{G_{dmax}}{G_{mmax}}$$

where G_{dmax} et G_{mmax} are maximum conductance and transconductance, respectively, and V_{gmax} is the gate voltage corresponding to G_{mmax}. It is shown in Fig. 3b that for short stressing periods, the maximum value G_{mmax} decreases while its position V_{gmax} does not change, so that V_t decreases. For longer periods of stress (t ≥ 1 hr) a second G_m maximum emerges which can exceed the first one and leads to an *apparent* increase in the extrapolated V_t. It is, therefore, more reasonable to consider that the important role is played by the generation of defects in a very narrow region ΔL situated above the channel and beside the drain. Indeed, the curves of Fig. 3b are very similar to those obtained by 2-D simulation, for the case where acceptor states or fixed negative charges of density of 5 to 10×10^{11} cm^{-2} are localized in ΔL = 0.05 µm /4/.



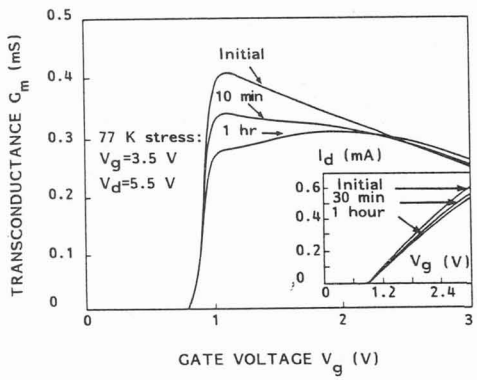


Fig. 3a - Extrapolated threshold voltage shift versus stress time for a device stressed at V_g = 3.5 V and V_d = 5.5 V.

Fig. 3b - Transconductance versus gate voltage characteristics of a device stressed at V_g = 3.5 V and V_d = 5.5 V; measurement at 77 K with V_d = 50 mV and stress time as a parameter.

The relaxation effect at 77 K was found to shift back the curves compared to those taken immediately after stress (curve 3 of Fig. 4); approximately 30 % of the initial degradation is recovered after 60 hours relaxation. This requires the stress-induced degradation to be caused partly by the electron capture in shallow-level traps in the gate oxide as suggested by Ning /6/. Warming up the stressed samples to 300 K shows yet a more beneficial influence; subsequent measurement at 77 K shows a larger decrease (≈ 50 %) in ΔV_t (curve 4). As the effect of damage created by the aging cannot be completely removed we conclude that the stress-induced defects in the MOSFETs studied here consist of (i) reversible electron capture in existing shallow-level traps and (ii) irreversible creation of interface states and/or electron traps in the oxide.

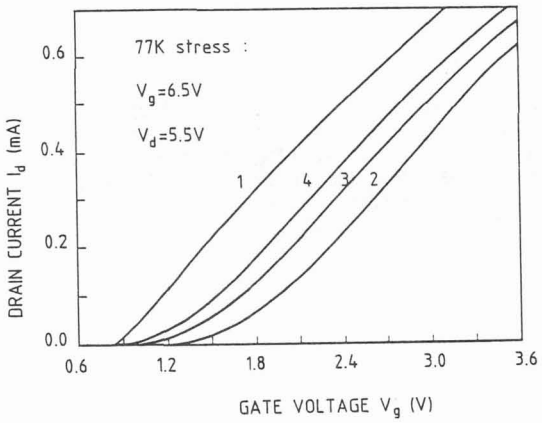


Fig. 4 - $I_d(V_g)$ characteristics showing the relaxation effect; (1) initial, (2) 3 hours stress at V_g = 6.5 V and V_d = 5.5 V, (3) 60 hours pause at 77 K, (4) + 1 hour pause at 300 K.

Another relevant result is observed in the case of $V_g > V_d$ stressing; after stress the saturation transconductance measured for V_d = 5 V in the reverse mode becomes larger than in the forward mode (which remains almost the same as the pre-stress value) (Fig. 5). This improvement in G_{msat} for degraded MOSFETs may be explained by the interaction between the defective and defect-free regions of the channel (as proposed above for the ohmic operation). In the forward-mode operation, G_{msat} of the degraded MOSFET should be the same as the pre-stress value because the defective region is completely screened by the pinch-off region. In contrast, when the source and drain are interchanged, the stressed device can be cosidered as a series combination of two transistors. The total transconductance depends on the interaction of these two regions and can exceed the transconductance of a homogenous MOSFET.

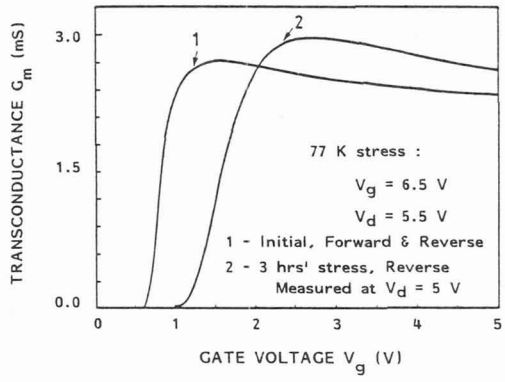


Fig. 5 - Saturation transconductance versus gate voltage of a MOSFET stressed at V_g = 6.5 V and V_d = 5.5 V.

3 - CONCLUSION

Hot carrier degradation has been carried out on 1 µm n-MOSFETs at 77 K and constant drain voltage, with the gate voltage as a variable. It has been found that the extension of the defective region into the channel depends strongly on the V_g/V_d ratio and determines the behavior of the device degradation. For the $V_g < V_d$ stress regime, the degradation of the maximum transconductance is dominant while the threshold voltage hardly changes. In contrast, at $V_g > V_d$ the stress-induced shift of V_t is important and increases with increasing V_g while the change in the transconductance maximum is found to be attenuated and a transconductance overshoot is observed for several periods of stress. The increase in the saturation transconductance of the stressed devices is explained by the two-piece model. The comparison with the results of 2-D numerical calculations allows us to conclude that for a drain voltage as high as 5.5 V, increasing V_g makes the extension of the defective region go deeper into the channel. The partial relaxation at 77 K and 300 K of the created defects suggests that they consist of the electrons captured in shallow-level neutral traps and the acceptor-like interface states and/or negative fixed charges.

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