ANALYSIS OF HOT CARRIER DEGRADATION IN AC STRESSED N-CHANNEL MOS TRANSISTORS USING THE CHARGE PUMPING TECHNIQUE

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ANALYSIS OF HOT CARRIER DEGRADATION IN AC STRESSED N-CHANNEL MOS TRANSISTORS USING THE CHARGE PUMPING TECHNIQUE

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Résumé

La dégradation par porteurs chauds (hot carriers) de transistors nMOS, induite lors de l'application de tensions alternatives (AC-stress) a été évaluée en utilisant la technique Charge Pumping et les résultats ont été comparés à ceux d'une contrainte sous tension continue. En outre d'une composante de dégradation uniquement dépendante du temps de vieillissement, une composante additionelle a été observée qui est proportionelle au nombre d'impulsions appliquées (fréquence * temps). La dégradation s'avère fortement dépendante de la forme de l'impulsion à la grille. En effet, nos expériences prouvent d'une part que le temps de descente de l'impulsion de grille est beaucoup plus important que le temps de montée, et d'autre part que la largeur de l'impulsion de grille détermine le degré de compensation de la charge positive piégée durant la période de tension basse à la grille, par des électrons injectés durant la période de tension haute.

Abstract

Hot carrier degradation induced during AC-stressing of NMOS transistors is evaluated using the charge pumping technique and the results are compared with those from DC-stress. Besides a degradation component that is only dependent on stress time, an additional component is observed that is proportional to the number of applied pulses (frequency * time). A strong dependency of the degradation on the shape of the gate pulse is demonstrated. The falling edge of the gate pulse is shown to be much more important than the rising edge and the width of the gate pulse determines the amount of compensation of the trapped positive charge by injected electrons.

1. Introduction

In the last decade much effort has been spent in the characterization and understanding of hot carrier degradation in DC-stressed n-channel and p-channel transistors /1/. Although there is still no unanimous agreement on the mechanisms causing this DC-degradation, the question already arises whether the results obtained under DC-stress conditions can be simply extrapolated towards AC-stress conditions /2/ or if some additional effects have to be accounted for /3,4/. Therefore, in this study, AC-stressed n-channel transistors are evaluated with the charge pumping measurement technique /5/, which is shown to be a powerful and indispensable tool for evaluation of this kind of degradation /6,7/. The AC-degradation results are compared with those obtained during DC-stress conditions. The influence of the used frequency and of the shape of the gate pulse is studied and a possible explanation of the enhanced degradation is given.

2. Devices and experimental conditions

The devices used in this study had an effective channel length of 2.4 µm and a channel width of 100 µm. The oxide thickness was 27 nm. The devices came from different suppliers with different technologies. In this way, technology-dependent effects could be ruled out.
As illustrated on Fig. 1, during the AC-stressing, a constant voltage V_d was applied at the drain while the gate was pulsed between V_{glow} and $V_{ghigh} = V_d$. The other features of the applied pulse are illustrated on Fig. 1. Source and substrate are grounded.

For the charge pumping measurements rectangular pulses were applied at the gate with an amplitude of 5 V and a frequency of 100 kHz. Drain and source were kept at a small reverse bias of 0.1 V while the substrate current was monitored.

3. Expected behaviour based on extrapolation of DC-degradation

By using the charge pumping technique in combination with conventional I-V measurements, the DC-degradation mechanisms have been revealed recently /8,9/. It was found that at medium gate voltages ($V_g \approx V_d/2$) maximum degradation occurs, due to interface trap generation. At low gate voltages ($V_g \approx V_t$), the interface trap generation is masked by positive charge trapping, due to hole injection /9,10/. The latter effect is dominant on the V_t-shift for these conditions. At high gate voltages ($V_g \approx V_d$), interface trap generation is minimal, as is the

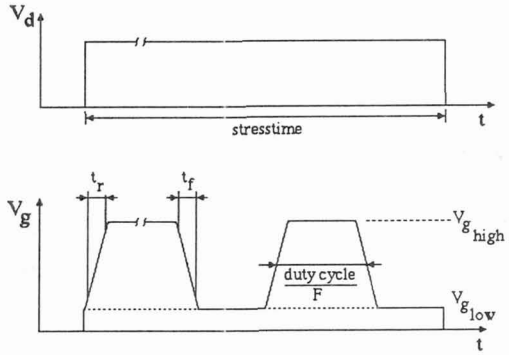

Fig. 1 : Drain and gate voltages applied during AC-stress conditions

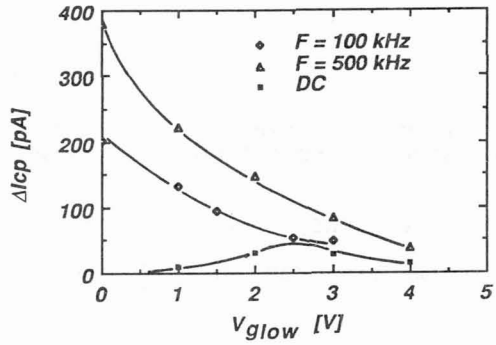

Fig. 2 : ΔI_{cp} as a function of V_{glow} for V_d=7.5V, t_r=t_f=10ns and duty cycle=50%. Stress time was 1000s for AC-stress, 500s for DC-stress. L=2µm, W=100µm

degradation of the I-V characteristic. However, when this condition is applied after a stress at $V_g = V_t$, compensation of the trapped holes occurs, and the interface traps generated at $V_g = V_t$ suddenly influence the I-V characteristics /8,9/. By simply extrapolating the DC-results to pulse shapes as on Fig. 1, one could therefore be inclined to neglect the minor degradation during the part of the gate pulse when $V_g = V_d$ and the degradation would be expected to occur mainly during the $V_g = V_{g_{low}}$ part of the gate pulse. However, during the rise and fall of the gate pulse, a contribution is expected that increases with increasing t_f and t_r. The maximum AC-degradation would however never surmount the worst case of the DC-degradation at the same V_d. Finally, the compensation of the trapped holes mentioned before is expected to be complete during the $V_g = V_d$ part of the pulse, if the trapping time of the electrons is smaller than the pulsewidth.

4. Measurement results

In the same way as for DC-stress conditions, the AC-degradation was studied as a function of stress time for different combinations of the stress parameters. While for DC-stress conditions V_d, V_g and the stress time are the most important parameters, for AC-degradations with a constant V_d, one has to evaluate the possible influence of the frequency F, the rise time t_r and the fall time t_f, the duty cycle, the low value of the gate voltage $V_{g_{low}}$ and the width of the gate pulse. All these parameters will now be studied one by one.

Comparison of AC-degradation with DC-degradation

Fig. 2 shows the increase in charge pumping current ΔI_{cp} as a function of the low value of the gate pulse $V_{g_{low}}$ for a total stress time of 1000 s. In all these experiments $V_{g_{high}}$ was equal to V_d = 7.5 V, $t_f = t_r$ = 10 ns, duty cycle = 50 %. For comparison ΔI_{cp} for DC-stresses during 500 s at V_d = 7.5 V and various V_g was plotted on the same figure. For high $V_{g_{low}}$, i.e. a small difference between $V_{g_{high}}$ and $V_{g_{low}}$, the curve for the AC-degradation approaches that of the DC-stress. For small $V_{g_{low}}$ however, the two curves differ completely and the highest degradation occurs for $V_{g_{low}}$ = 0 V and strongly exceeds the maximum DC-degradation. Moreover, the difference is proportional to the used frequency, which is already indicative of an enhanced degradation during the edges of the gate pulse.

Influence of the frequency of the gate pulse

The stresses at $V_{g_{low}}$ = 0 V were studied extensively in order to clarify the enhanced degradation. Fig. 3 shows the time dependency of the degradation for different frequencies. All degradations were performed with $t_r = t_f$ = 6 ns, duty cycle = 90 %, $V_{g_{high}} = V_d$ = 6.5 V. It follows from the figure that the time dependency of ΔI_{cp} has a slope factor of 0.67 for all frequencies, which is identical to the time dependency during DC-stress. As already illustrated on Fig. 2, one can also observe a dependency on the frequency at a given stress time. This dependency has the same slope factor n = 0.67. In Fig. 3, the time during which $V_g = V_{g_{high}}$ is independent of the frequency for a fixed stress time, since the duty cycle is fixed. Consequently, if the degradation at $V_g = V_{g_{high}}$ would be dominant, the curves for different frequencies would coincide, which is clearly not the case. When one plots the curves of Fig. 3 as a function of the number of applied pulses, i.e. N = F * stress time, one obtains more or less a unique dependency independent of the stress time and the applied frequency, as is shown on Fig. 4. This dependency once more has a slope of 0.67 which again points to a main degradation contribution during the edges of the gate pulse. One can conclude that for the AC-stress case $V_{g_{low}}$ = 0 V, the main degradation occurs only during the falling and/or rising transition edges of the gate pulse, and therefore is proportional to the number of pulses N with a dependency $\Delta I_{cp} = A\, N^n$ with n = 0.67.

Influence of the low part of the gate pulse

In the previous paragraph $V_{g_{low}}$ was always taken equal to 0 V, which means that during the part of the gate pulse when $V_g = V_{g_{low}}$ no degradation occurred while during the high part of the gate pulse ($V_g = V_d$) the DC-degradation is negligible as compared to the degradation during the transition edges of the gate pulses. For conditions where $V_{g_{low}}$ is different from 0 V however one can observe a contribution of

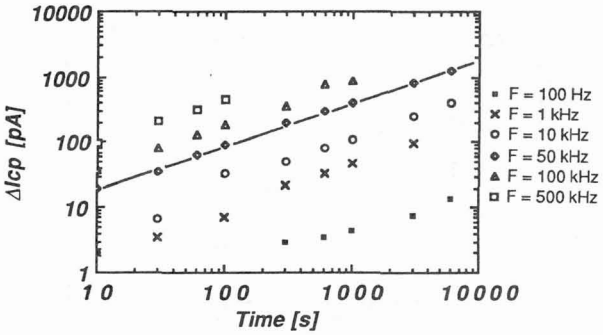

Fig. 3 : ΔI_{cp} as a function of stress time for V_d=6.5V, V_{glow}=0V, t_r=t_f=6ns and duty cycle=90%. L=2µm, W=100µm

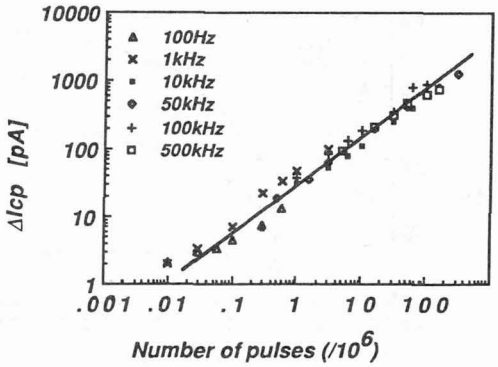

Fig. 4 : ΔI_{cp} as a function of the number of applied pulses for V_d=6.5V, V_{glow}=0V, t_r=t_f=6ns and duty cycle=90%. L=2µm, W=100µm

the DC-degradation during $V_g = V_{glow}$. On Fig. 5, ΔI_{cp} is plotted as a function of the frequency for V_{glow} = 1 V, $t_r = t_f$ = 6 ns, duty cycle = 50 %, $V_{ghigh} = V_d$ = 7 V, stress time = 1000s. As can be seen ΔI_{cp} does not increase linearly with frequency in this case. At low F, the DC-degradation during the part of the gate pulse when $V_g = V_{glow}$ is much larger than the extra degradation during the transition edges of the gate pulse. The latter shows up on Fig. 5 as the frequency dependent component, while the former is frequency independent, because the duty cycle is kept constant. When one subtracts the part of the degradation occurring at $V_g = V_{glow}$ from the total degradation curve, only the degradation during the transition edges remains. This is shown on Fig. 5 on the curve labeled "AC component". This curve has a slope factor n = 0.7, as is the case for V_{glow} = 0 V.

Influence of the edges of the gate pulse

In order to reveal the cause for the enhanced degradation occurring during the transition edges of the gate pulse, the influence of the edges on ΔI_{cp} for transistors stressed at F = 100 kHz, V_{glow} = 0 V, $V_{ghigh} = V_d$ = 6.5 V, duty cycle = 50 % and $t_f = t_r$ is shown on Fig. 6. It is obvious that decreasing t_f and t_r increases the degradation. This definitely proves that this degradation is not DC-related, since in this case one would expect a decreasing degradation with decreasing t_f and t_r. In order to find an explanation for the observed behaviour, rising and falling edges were varied independently. It was found that the enhanced degradation almost completely occurs during the fall time, while changing the rise time has little effect. For very large t_r and t_f the degradation again increases because DC-degradation during the transition edges now becomes more important.

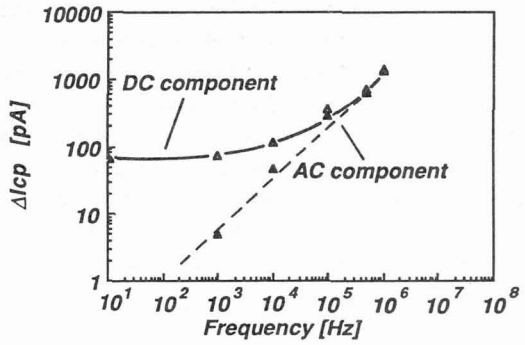

Fig. 5 : ΔI_{cp} as a function of the frequency for stress time=1000s, V_d=7V, V_{glow}= 1V, t_r=t_f=6ns and duty cycle=50%. L=2µm, W=100µm

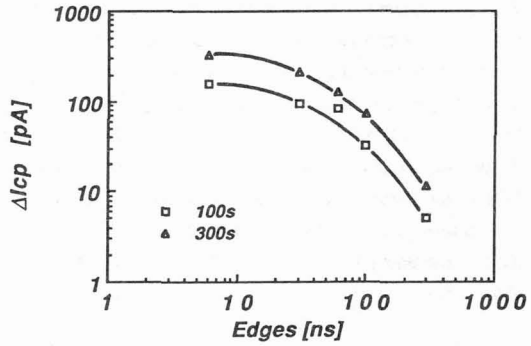

Fig. 6 : ΔI_{cp} as a function of the rise and fall times at 2 stress times for V_d=6.5V, V_{glow}=0V, F=100kHz and duty cycle= 50%. L=2µm, W=100µm

Influence of the duty cycle of the gate pulse

From DC-experiments, it is known that during a stress at $V_g = V_t$ positive charge is trapped in the oxide, that can be compensated by a subsequent stress at $V_g = V_d$ /10/. Since this sequence of stresses is repetitively applied during AC-stress, we were able to study in more detail the hole trapping and subsequent compensation using AC-stress conditions. From charge pumping measurements, it was found that positive charge trapping during $V_g = V_{glow}$ still occurs up to frequencies of 10 MHz. This proves that this hole trapping process has a time constant, smaller than 50 ns. In order to study the compensation effect by electron trapping, stresses at different duty cycles were performed. Fig. 7 shows the influence of the duty cycle on ΔI_{cp} for transistors stressed at F = 100 kHz, $t_r = t_f$ = 6 ns, V_{glow} = 0 V, $V_{ghigh} = V_d$ =

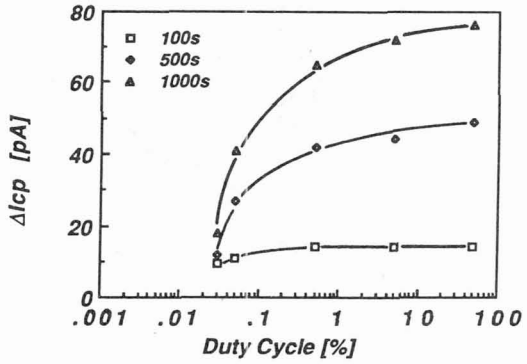

Fig. 7 : ΔI_{cp} as a function of the duty cycle at 3 stress times for V_d=6.5V, V_{glow}=0V, F=10kHz, t_r=t_f=6ns. L=2μm, W=100μm

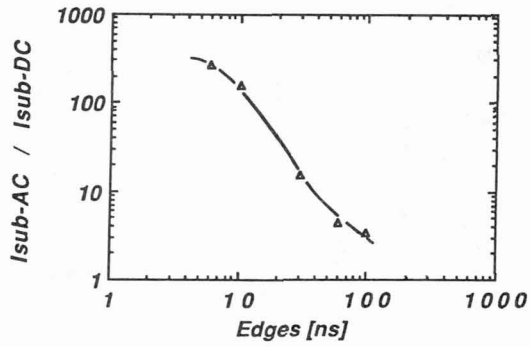

Fig. 8 : AC-component of measured I_{sub} / DC-simulated I_{sub} as a function of the edges for V_d=7.5V, V_{glow}=0V, F=100kHz and duty cycle= 50%. L=2μm, W=100μm

7.5 V and stress time = 200 s . ΔI_{cp} decreases for the lower values of the duty cycle. This behaviour will be explained in the next paragraph.

5. Discussion

From the experiments in the previous paragraph, it can be concluded that the degradation during AC-stress with constant drain voltage is composed of two components : one component is DC-related (mainly occurring at $V_g = V_{glow}$ or during the fall and rise times of the gate pulse); the other component, which is proportional to the number of applied pulses, is not observed during the DC-degradation, and occurs only during the falling edge of the gate pulse. This component has often caused the extrapolation of DC-results towards AC-conditions to fail. In these extrapolations the substrate current is always assumed to be the integral of DC substrate currents. However, for small fall times, this assumption is no longer valid. Indeed, we performed substrate current measurements under identical conditions as during the stress experiments, and compared them with measurement results under DC-conditions. The results are shown on Fig. 8 as a function of the fall time, for F = 100 kHz, V_{glow} = 0 V, V_{ghigh} = V_d = 7.5 V. The substrate current under AC-conditions, for fall times of 10 ns, is seen to be a factor of 250 larger than what is expected from DC-measurements. This enhancement decreases to a factor of 3 for larger fall times. These results are in qualitative agreement with the degradation as a function of the edges, showed on Fig. 6. Moreover, it is observed that this enhancement is not dependent on the rise time, as is also the case for the degradation behaviour. Therefore, this enhanced substrate current can be correlated with the degradation component during the falling edge of the gate pulse. At present, experiments are being performed to clarify the exact origin of this substrate current enhancement. Together with the substrate current increase and accompanying increase in interface trap density for decreasing fall time, a large build-up of positive charge is expected. For the conditions of Fig. 7 with a low duty cycle this positive charge is only partially compensated by the electrons injected during the part of the gate pulse when $V_g = V_d$ /9,10/. Because of the incomplete compensation, a net positive charge remains at the drain which decreases the lateral electric field during the falling edge resulting in a reduced generation of interface traps. For larger duty cycles, the positive charge is however completely compensated within each cycle and the electric fields will be maximal during the fall-off of the gate pulse. From Fig. 7 and from similar additional charge pumping experiments, the time constant for the compensation process (electron trapping on trapped holes) is found to be about 0.5μs.

6. Conclusions

An enhanced degradation has been observed for AC-stress conditions using gate voltage pulses and a constant high drain voltage. This enhancement is dependent on the shape of the gate pulse. Decreasing fall times enhance the effect, while the rising edge has little influence. An enhanced substrate current has been observed for identical stress conditions. At present experiments are being performed to explain this phenomenon. The duty cycle determines the amount of compensation of the positive charge by the injected electrons.

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