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PHYSICAL BEHAVIOUR MODELLING OF VDMOS DEVICES

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Abstract - An analytical model is proposed in order to explain the physical behaviour of VDMOS devices at any DC current level. The quasi-saturation effect is included considering the carrier saturation velocity at high electric fields. Interdigitated VDMOS devices have been fabricated and 2D simulations have been carried out to check the model.

1 - INTRODUCTION

The vertical DMOS transistor is one of the most usual drivers in power MOS ICs /1/. The linear region of its I-V characteristic has been modelled considering a surface accumulated layer, the JFET resistance between cells and a bulk epilayer resistance together with the active channel /2/. Moreover, in previous works /3, 4/ the current pinching was responsible for the quasi-saturation (q-s) effect or limitation in the current handling capability typical at high current levels. In contrast, 2D simulations /5/ have not shown current pinching between cells but, contrarily, there is a majority carrier excess in the JFET region, suggesting that q-s effect is due to carrier velocity saturation. The carrier excess was explained by means of a dipole similar to the one formed in a JFET channel under carrier velocity saturation conditions. However, none of the previous models has quantitatively explained these phenomena.

This work is aimed to study the detailed physical behaviour of the VDMOS to avoid the tedious 2D CAD. Interdigitated VDMOS structures have been fabricated and 2D simulations /6/ have been carried out in order to check the proposed model.

2 - MODEL

Due to the axial symmetry of the VDMOS structure (see fig 1), current and electric field equations can be simplified to one-dimensional analysis:

\[
\frac{I}{A(y)} = q \mu \left[ n E + \frac{kT}{q} \frac{dn}{dy} \right] \quad (1)
\]

\[
\frac{d}{dy} \left[ A(y) E \right] = \frac{q}{e_s} A(y) (n_0 - n) \quad (2)
\]

where \( n_0 \) is the epilayer doping level and \( A(y) \) is the cross-section area of the current path. Suitable approximations in the different regions of the epitaxy have been taken into account in order to obtain analytical solutions for the electric field distribution and for the majority carrier concentration; as shown in fig. 1, these regions are, namely: a) the surface accumulated layer induced by the gate effect of the MOS structure; b) the JFET region between cells and c) the drift region up to the drain contact.

a) SUPERFICIAL REGION. The limits of this region are the Si-SiO\(_2\) interface and the null electric field point inside the epilayer (\( y_B \)), which is a consequence of the device bias; i.e., \( V_G \) and \( V_D \) are both positive while the source is grounded, so it must exist a point of
minimum potential between gate and drain. This region has been splitted into two zones since the electric field changes from very high values at the interface to zero at the other edge. In the first zone under the gate electrode, \( S_1 \), the electric field and the carrier concentration gradient are very sharp so that the drift \( (J_d) \) and the diffusion \( (J_d) \) currents are much greater than the total current flowing through the VDMOS. Consequently, \( n \gg n_o \) and \( J_d = J \) are appropriate approaches, the solution being:

\[
E = \left[ \frac{1}{E_s} + \frac{q}{2kT} \gamma \right]^{-1}
\]

\[
n = \frac{E_s}{2kT} \gamma^2
\]

where \( E_s \) is the surface electric field.

The second zone, \( S_2 \), lies by the zero electric field point; therefore, \( J \) is small and a linear dependence on the electric field has been assumed, \( J = q \mu n_s E \), \( n_s \) being the carrier concentration at the \( y_b \) point. Under these conditions the solution is:

\[
E = A \exp(-ay) - \frac{I}{q \mu n_s E}
\]

\[
n = n_o + a \frac{E_s}{q} A \exp(-ay)
\]

where \( A \) is an integration constant and \( a = (n_s q^2/kT) E_s^{1/2} \). The boundary point of \( S_1 \) and \( S_2 \) zones, the constant \( A \), and \( y_b \) are determined imposing the continuity condition of their solutions.

b) JFET REGION. This region spans from the edge of the former zone up to the point where current is no longer confined by the depletion layer of the body-epitaxy junction. This point is found assuming this junction to be plane in punchthrough mode at the onset of the junction curvature (see fig. 1). Obviously, the length of this region depends on the drain voltage but its width remains constant and equals the cell spacing \( \xi \). In this sense, and according to this model, there is a modulation of the JFET length instead of a modulation of the JFET width as considered in previous works /3,4/.

In this region, the carrier concentration is close to \( n_o \) and consequently \( J_d \) is negligible. An accurate solution is:

\[
n = n_o \left[ 1 + \frac{4}{1 + 4} \frac{n_b}{n_o} \left[ \frac{n_b}{n_o} - 1 \right] \left[ 1 - \exp(-r(y-y_b)) \right] \right]^{1/2}
\]

\[
E = \frac{I}{q \mu n \xi}
\]

where \( r = (q^2 \mu n \xi) / (E_s I) \). The carrier concentration (7) tends asymptotically to \( n_o \) at a rate which depends on \( r \) and \( \xi \), therefore, on the current level \( I \). According to this analysis the tail of the accumulated layer can extend inside the epitaxy and it could even reach significant depths.

c) DRIFT REGION. Once the current flow leaves the JFET region, it spreads inside the epilayer with a 45° angle /2/ forming a trapezoidal zone followed by a rectangular zone if the epitaxy is thick enough. Solutions for this region are obtained similarly to the former case but considering a cross section \( A(y) \) linearly depending on the \( y \) coordinate in the trapezoidal
zone.

The above formulation is valid for electric fields below the saturation value, \( E_{sat} \). For higher fields we have supposed a carrier mobility \( \mu(E) = \frac{v_{sat}}{E} \) according to \( /7/\). The solutions of the general equations (1) and (2) under this condition in the different regions, with its respective approximations, are straightforward calculated.

Finally, the voltage drop across any region and its resistance are analytically obtained integrating the electric field distributions.

3 - RESULTS

Electric field distributions obtained from the proposed model and from 2D simulations are plotted on fig. 2, for \( V_D = 5 \) and 20 V, the last value corresponding to the q-s mode. Note that the peak electric field moves inside the epitaxy as the drain voltage increases, showing the JFET length modulation effect predicted by the model. A good agreement between theory and 2D simulations is achieved not only inside the epitaxy but at the accumulated surface as shown in the insert.

Normalized carrier concentration is plotted on fig. 3. Let us remark that the tail of the accumulated layer extends up to the body depth even though the device is not in the q-s region. Similarly to the field distribution, the formulation fits the 2D simulations all through the epilayer.

The I-V characteristics of the fabricated devices are shown in fig. 4, where the gate voltage has been chosen high enough to reach the q-s region. Experimental as well as 2D simulations points are in good agreement with the model. On the same figure, the theoretical results without considering carrier velocity saturation are plotted. Note that this effect is just responsible for the current limitation when the transistor is under q-s conditions. The proposed model has been successfully checked as well for the VDMOS devices referred in \( /3,5/\).

4 - CONCLUSIONS

An analytical model for VDMOS devices has been presented. It is based on the solution of the general semiconductor equations with suitable approximations for the different regions into which the epitaxial layer has been divided. This model accounts for the electric field and for the majority carrier concentration distributions which have been checked using Bambi. This formulation also explains the quasi-saturation effect considering the carrier velocity saturation at high electric fields. Interdigitated VDMOS devices have been fabricated and their output characteristics are in good agreement with the proposed model as well as with the 2D simulations performed.

REFERENCES

Fig. 1. - VDMOS cross-section. Fabricated structure parameters: \( W=40 \mu \text{m}, h=5 \mu \text{m}, \)
\( r=60 \mu \text{m}, l=10 \mu \text{m}, n_0=2\times10^{14} \text{ cm}^{-3}, \)
channel length = 2 \( \mu \text{m} \) and channel width = 25 \( \mu \text{m}. \)

Fig. 2. - Electric field along the \( \text{AA}' \) line.

Fig. 3. - Normalized carrier concentration along the \( \text{AA}' \) line before q-s.

Fig. 4. - I-V characteristics.