THEORETICAL ANALYSIS OF THE TWO-TERMINAL MOS CAPACITOR ON SOI SUBSTRATE

P. Paelinck, D. Flandre, A. Terao, F. van de Wiele

JOURNAL DE PHYSIQUE
Colloque C4, supplément au n°9, Tome 49, septembre 1988

THEORETICAL ANALYSIS OF THE TWO-TERMINAL MOS CAPACITOR ON SOI SUBSTRATE

P. PAELINCK[1], D. FLANDRE[1], A. TERAO[2] and F. VAN de WIELE

Laboratoire de Microélectronique, Université Catholique de Louvain, Place du Levant 3, B-1348 Louvain-la-Neuve, Belgium

Résumé - Des modélisations analytiques et numériques de la capacité métal-oxyde-semiconducteur sont proposées pour les substrats sur isolant comportant un film flottant. Le traitement théorique repose sur des considérations physiques et met en évidence l'influence de la distribution des diverses charges à l'intérieur de la structure globale. Les caractéristiques capacité-tension sont directement interprétables à partir des mécanismes physiques internes du dispositif.

Abstract - The present paper deals with the analytical and numerical study of MOS capacitors on SOI substrates. The major concern is the theoretical treatment of such devices with floating substrate. Special care has been taken to keep the mathematical modeling consistent with physical considerations. The importance and the role of the underlying silicon substrate have been highlighted. The different operating conditions of the capacitance-voltage characteristic have been interpreted in terms of device intrinsic physical mechanisms.

1 - INTRODUCTION

Owing to its simplicity of fabrication and analysis, the MOS capacitor is now intensively used for the control and the study of the electrical properties of MOS circuits integrated in the bulk.On the contrary, in SOI technology, alternative techniques to standard C(V) measurements have been proposed for characterizing the MOS system [1,2]. However, the structures that are considered in these experiments are 3 or 4 terminals devices, allowing to get rid of problems related to the floating substrate. Unfortunately, the need for minimizing parasitic capacitance effects (w.r.t. pure capacitance measurements) results in an increased complexity in the method for extracting the material parameters. Our purpose, guided by physical reasoning, is to propose accurate analytical and numerical modelings of the two-terminal MOS/SOI capacitor (Fig. 1). We will show that the capacitance characteristic is somewhat different from that of the classical bulk MOS capacitor. The discrepancies will be explained from the charges distribution within the whole structure. The influence of several technological and electrical parameters will be discussed.

The study is based on the one-dimensional solution of the Poisson equation. Since no current flows through the capacitor, the Fermi potentials are constant but different in the film and in the substrate. This implicitly assumes that a gradient of the Fermi potential exists within the buried oxide. Nevertheless, since the carriers densities vanish in the insulator, there is no current in the oxide. However, the Fermi potential in the SOI film can not be a priori known since there is no physical contact on the latter. Moreover, owing to the fact that the film is sandwiched between two insulators, carriers are impedded from leaving the film. These physical considerations lead to state that, whatever the voltage applied to the gate, the overall charge in the floating SOI layer remains constant and equal to the charge stored in the film at equilibrium. This constant charge depends on the doping profile, the interface charges and the geometrical characteristics of the structure. This is to say that, for any gate voltage, any variational charge appearing underneath the front gate must be compensated by an other charge (of opposite sign) above the back interface so as to keep constant the integrated space charge density in the film.The low-frequency capacitance-voltage characteristic is then easily derived by calculating the variation of the potential drop across the gate oxide with respect to the gate voltage.

---

(1) P. Paelinck and D. Flandre are granted by I.R.S.I.A.
(2) A. Terao is a research assistant of the National Fund for Scientific Research

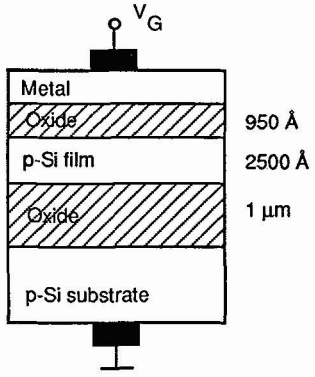

Fig. 1 - The MOS capacitor on SOI substrate

2 - MODELING

2.1. Analytical modeling

The analytical model is limited to fixed oxide charges and uniform doping levels. An analytical model for an ideal SOI MOS capacitor (zero interface charges, zero work function differences) has recently been published [3]. It points out that, in contradiction with classical approximations [4], the SOI MOS capacitor analysis requires to take into account the non zero width of the accumulation layer in the SOI film as well as the space charge region in the underlying non metallic silicon substrate.
Our model has now been extended to non zero interface charges and work function differences.
In order to solve the one-dimensional Poisson equation in the SOI film, we need an additional boundary condition, which depends on the following situations :
- as long as front and back space charge regions are not in interaction, we assume that they are separated by a quasi-neutral region
- when they interact, the sum of the widths of the front and back space charge regions is a constant equal to the film thickness; in that case, we have to approximate the different space charge region widths[5] and these constitute the single analytical approximations.
Finally, the analytical model consists in a set of nonlinear equations which can be solved using a classical iterative method.

2.2. Numerical modeling

Numerical modeling takes all the capacitor characteristics into account : film thicknesses, nonuniform impurities concentrations, fixed oxide charges and fast interface states densities.The strategy relies on a two-step procedure [6]. In a first phase, the structure under equilibrium conditions is simulated in order to determine the integrated charge in the SOI film. Then, for other gate biases, the Poisson equation is solved at each node of the discretization grid. The related set of equations is to be augmented with an integral conservation constraint, allowing to determine the unknown Fermi potential. This additional relationship requires that the overall variational charge must vanish in the floating substrate for any gate voltage. The latter entails a reasonable increase in the system matrix complexity, provided that the equations are reordered. The resulting system of equations is easily solved using a gaussian elimination.

3 - RESULTS

The first structure that has been investigated includes interface states densities at the three silicon dioxide/silicon interfaces. The impurities concentration in the film is one order of magnitude higher than in the substrate. The C(V) curve is quite dissimilar to the typical characteristics exhibited by classical bulk capacitors (Fig. 2).

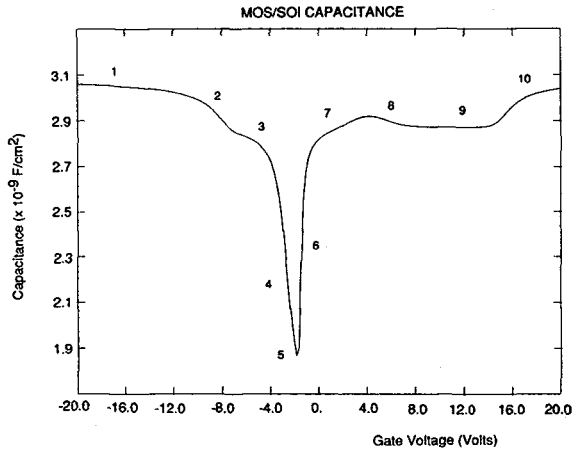

Fig. 2 - Capacitance-Voltage curve ($N_{A,film}=10^{15}$ cm^{-3}, $N_{A,subs}=10^{14}$ cm^{-3}) ($N_{ssf}=5.10^{10}$,$N_{ssb}=10^{11}$ and $N_{sss}=5.10^{10}$ cm^{-2}) ($t_{film}=2500$ Å)

This is due to the various charges appearing in the structure. The basic keypoint lies in the fact that the different interfaces reach accumulation, depletion and inversion for different gate voltages. In Table 1 are listed the charges controlled by the three interfaces for different operating conditions of the capacitor as referred in Fig. 2 (a=accumulation, d=depletion, w.i.=weak inversion, i=inversion).

Case	1	2	3	4	5	6	7	8	9	10
Front interface	a	a	d	d	w.i.	w.i.	w.i.	i	i	i
Back interface	i	i	i	i	i	i	i	w.i.	a	a
Substrate	a	a	a	d	w.i.	i	i	i	i	i

Table 1 - Modes of operation of the MOS/SOI capacitor

The charge in the substrate depends on the gate voltage in the same manner as in the classical capacitor . However, charges in the SOI film may interact or not, depending on the film thickness, the doping level and the interface charges densities. Under non equilibrium conditions, it can be observed that the overall variational charge in the floating film is zero. This is responsible for the modulation of the electrical potential at both front and back interfaces. Fig. 3 shows the influence of the substrate doping level on the capacitance. For substrate doping levels lower than the SOI film doping level, the capacitance depends on the substrate behaviour only over a small range of voltages around the minimum value. When the impurities concentration increases, the influence of the charge stored in the underlying substrate tends to modulate the C(V) curve over a wider gate voltage range. This explains why the silicon substrate must be included in the model instead of replacing it by a metallic gate.

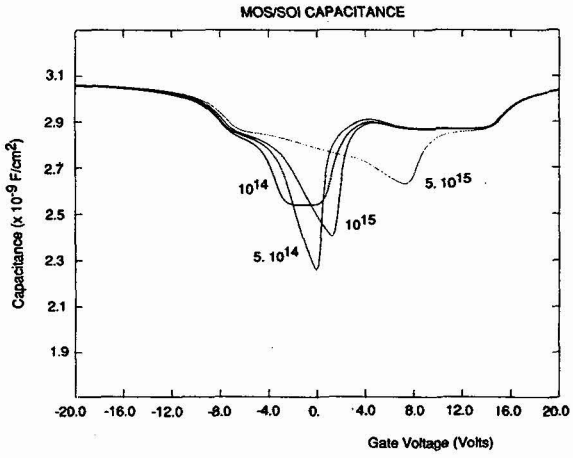

Fig. 3 - Capacitance-Voltage curve ($N_{A,film}=10^{15}$ cm^{-3}, $t_{film}=2500$ Å)
($N_{ssf}=5.10^{10}$, $N_{ssb}=10^{11}$ and $N_{sss}=5.10^{10}$ cm^{-2})

4 - CONCLUSION

A consistent theoretical treatment of MOS capacitor on SOI substrate has been proposed. We have shown that, under non equilibrium conditions, the Fermi potential within the floating substrate has to adapt itself so as to maintain the charge stored in the film at equilibrium. At present time, no experimental results concerning the MOS/SOI capacitor as a two-terminal device have been yet reported. This could be attributed to the quite unusual shape exhibited by the capacitance-voltage characteristic of this structure. From this point of view, the above-mentioned approach gives some insight into the major physical mechanisms and enables to state clearly the correspondence between the various modes of operation of the capacitor and its electrical behaviour. However, it is still to be determined whether the MOS/SOI capacitor can be used as a characterization device as in bulk technology.

REFERENCES

[1] Lee, J.-H. and Cristoloveanu, S., IEEE Electron Device Letters Vol. EDL-7 (1986) 537-539
[2] Vu, D.P. and Pfister, J.C., Applied Physics Letters 48 1 (1986) 50-52
[3] Flandre, D. and Van de Wiele F., IEEE Electron Device Letters Vol. EDL-8 (1988)
[4] Lim, H.-K. and Fossum, J.G., IEEE Trans. Electron Devices Vol. ED-30 (1983) 1244-1251
[5] Hauser, J.R. and Littlejohn, M.A., Solid-State Electr. 11 (1968) 667-674
[6] Van de Wiele, F., to be published