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TRANSISTORS MADE IN SINGLE-CRYSTAL SOI FILMS

J.P. Colinge, E. Demoulin, D. Bensahel and G. Auvert

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<u>Résumé</u>.- Des transistors ont été réalisés dans des films de silicium déposés sur isolant et recristallisés par laser. L'utilisation de bandes anti-reflets de nitrure de silicium a permis de contrôler l'interface liquide-solide à l'arrière du spot laser, lors de la recristallisation. Cette technique permet de contrôler la posítion des joints de grains avec une bonne précision. Les joints de grains ont été ensuite dissous dans une étape d'oxydation localisée classique, laissant des bandes de silicium monocristallin complètement entourées d'oxyde. Des transistors MOS à canal N, ainsi que des oscillateurs en anneau ont été fabriqués dans ce matériau. La mobilité de surface des électrons y atteint 850 cm²/V.sec., et le délais par étage est de 1 nsec. dans les oscillateurs (L = 5 µm).

Abstract .- Transistors have been realized in laser-recrysallized siliconon-insulator films. Antireflecting stripes of silicon nitride were used to shape the trailing edge of the silicon as it quenches under laser scan, which allows accurate control of the grain boundary location. The grain boundaries were oxidized in a standard LOCOS process which left singlecrystal silicon stripes completely embedded in the oxide. N-channel transistors as well as ring oscillators were made in the recrystallized material. A surface mobility of 650 cm²/V.sec. was observed in the transistors, and a 1 nsec. delay per stage was measured in the ring oscillators (L = 5 μ m).

1. <u>Introduction</u>.- Silicon-On-Insulator (SOI) technologies are an attractive alternative for VLSI circuit manufacturing, owing to such advantages as reduced parasitic capacitances, latch-up immunity and insensitivity to alpha particles. Furthermore, the cost per wafer is promisingly low when such techniques based on the recrystallization of a polysilicon film deposited on a low-cost substrate (glass or oxidized metallurgical silicon wafer) are used.

Many different energy beams have been investigated for the melting and recrystallization of silicon films deposited on an insulator, among them cw lasers (1), lamps (2), or strip heaters (3). All these techniques operate in the same way: the silicon film, which may be encapsulated or not, is melted during the scanning, then quenched in such a way that large crystallites are obtained. Typical grain sizes of 5 μ m X 10 μ m are obtained with cw laser systems, while much larger grains (1000 μ m X several mm) are obtained using lamps or strip heaters. However, in all these techniques, the location of the remaining defects (grain boundaries or subgrain boundaries) is always random. The consequence of this random location of defects is that a grain boundary may be located in a transistor somewhere in the SOI chip resulting in a malfunction of that transistor, and of the circuit, which is of course unacceptable.

2. <u>Control of the grain boundary location</u>. - Control of the temperature gradients in the quenching silicon film immediately following beam irradiation is a key to achieving large single-

Immediately following beam irradiation is a key to achieving large singlecrystals. This can be managed either by controlling the heat flow from the silicon film towards the substrate (4) or by spatially modulating the energy deposited in the film (5). In this experiment, we have used the so-called





Figure 1: Illustration of the process for controlling the grain boundary location. Sample is shown after decoration with Secco etch to reveal grain boundaries. Distance between two grain boundaries is 20 µm.

"selective annealing" technique (6) which is based on a very simple phenomenon: the enhancement of laser power absorption caused by the presence of an antireflection cap.

For the purpose of our illustration, we will now define the effective spot size of the focused laser beam as the diameter of the laser-induced melted area. This spot size obviously increases when the silicon is capped with an antireflection coating. The antireflecting cap being now patterned into stripes, the trailing edge, under the scanning conditions illustrated in Fig. 1, becomes a succession of concave interfaces ressembling the teeth on a gear when a round spot is used. The result is that grain boundaries will originate at the points where this trailing edge lags behind, i.e. at the tips of the gear teeth. Were the spot a straight line perpendicular to the scan, or elliptical in shape with a large excentricity, the grain boundaries would be located exactly beneath the center of the antireflection stripes. As can be seen in Fig. 1, such is not the case when a round beam is used, because the cooling down of those stripes which are nearest to the edges of the scanning spot is somewhat faster than that of the stripes scanned by the centre of the spot. It can also be seen in Fig. 1 that the silicon which has recrystallized in between the antireflection stripes has a smooth surface, while the silicon beneath stripes, which in this case acts also as an encapsulant, retains original surface roughness.

Since the scan speed used was relatively high (20 cm/sec.), and no encapsulant was used, the crystal orientation is random, although the crystal quality of each grain is very good (Fig. 2). Giving the combined effect of the micro-floating zone process and our locally concave trailing edges, defects are swept towards the grain boundaries, leaving behind device-worthy material in the grains.



Figure 2: Electron diffraction pattern of a <100> single-crystal. Traces of SiO₂ remaining on the sample scatter the electrons, giving rise to white "clouds". 3. Device fabrication process.-

The samples were made on <100> P-type silicon wafers. After growth of a 1 micron thick oxide.

a polysilicon film of 500 nm was deposited by LPCVD. A 50 nm thick film of silicon nitride was then deposited and patterned into stripes 10 μ m wide and 10 μ m apart (*i.e.* 20 μ m center to center). Laser annealing was then performed to grow large grains (here: 20 μ m X 1 mm) the boundaries of which were localized underneath the nitride stripes (Fig. 3.1). Since the location of the grain boundaries is fully controlled by a photolitho-

Since the location of the grain boundaries is fully controlled by a photolithographic step, they can be aligned with further process steps in view.

A second Mask of silicon nitride (which is roughly complementary to the first one was used to grow a LOCOS field oxide, which dissolved the grains boundaries and insulated the silicon stripes (or islands) the one from the other (Fig. 3.2/3) Samples then underwent a standard NMOS process (growth of gate oxide, E & D threshold adjustment, polysilicon deposition, doping and patterning, source and drain formation by arsenic implantation, LTO passivation, contact opening and metallization (Fig. 3.4).

Transistors with mask gate lengths ranging from 10 down to 4 μm were realized, as well as 7-stage ring oscillators (NMOS, depletion load).





Figure 3: Transistor fabrication process

3.1 : Growth of the single-crystals

3.2 : Nitride mask before field oxide growth

3.3 : Field oxide growth

3.4 : Transistor fabrication

4. Device characterization.-

Three different kinds of transistors were realized: those without grain boundaries, and those having

straight grain boundaries, purposefully placed in the channel of transistors, either parallel or perpendicular to the current flow. The devices with grain boundaries were realised in order to validate theoretical models: enhanced dopant diffusion along grain boundaries in the case of parallel grain boundaries (7), threshold voltage increase and mobility dependence on gate voltage in the case of perpendicular grain boundaries (8) (Figs 485).

In the devices having no grain boundaries, a surface mobility of 650 $\rm cm^2/V.sec.$ was observed.



- 1: single-crystal
- 2: with a grain boundary

Figure 4: Comparison between a transistor showing no grain boundary and a transistor having a grain boundary parallel to the current flow.



Figure 5: Same sa Fig. 4, but with the grain boundary perpendicular to the current flow.

The leakage current, which might be a problem in N-channel SDI devices, was in the 20 $nA/\mu m$ range. This can be reduced by a factor of 5000 when the bulk silicon substrate (back gate) is negatively biased at -5 V, suggesting that leakage current is mainly caused by back channel effects. The junction breakdown voltage was higher than 20 volts.

Ring oscillators were also realized, with the following transistor dimensions: W/L = 8/5 (driver and W/L = 4/5 (load). The delay per stage is 1 ns, which is excellent for devices of such channel lengths.

7-STAGE RING OSCILLATOR



driver: w/l=8/5 load : w/l=4/5

delay per stage: 1 nsec.

Figure 6: Photograph and output wave of a ring oscillator.

5. <u>Conclusions</u>. Transistors and ring oscillators have been realized in singlecrystal islands of silicon on SiO₂.

The method used to achieve single-crystallinity is suitable for manufacturing circuits exhibiting a repetitive design, such as memories or gate arrays, because the silicon single-crystals are parallel stripes insulated from one another by oxide stripes. The crystal quality and the surface smoothness of the films appear to be of good enough quality to be a serious SOI material for VLSI. Furthermore, this technology provides "ideal" samples for investigating the influence of grain boundaries in SOI TFTs.

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