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THIN FILMS OF III-V COMPOUNDS AND THEIR APPLICATIONS

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Résumé.— Les films minces de composés III-V ont de nombreuses applications potentielles comprenant les cellules solaires, les dispositifs à microondes et les circuits intégrés. Cet article est une revue des techniques qui ont été développées pour la préparation de film de composés III-V monocristallins et polycristallins. Un modèle d'ancrage du niveau de Fermi est introduit pour expliquer les propriétés des joints de grains et autres défauts présents dans ces films. On montre l'efficacité de différentes méthodes de passivation des effets des joints de grains.

Abstract.— Thin films of III-V compounds have many potential applications, including solar cells, microwave devices and integrated circuits. This paper will review the techniques that have been developed for preparing single-crystalline and polycrystalline III-V films. A Fermi-level pinning model is introduced to explain the properties of grain boundaries and other defects in these films. Various methods of passivating the effects of the grain boundaries have been proven to be successful.

1. Introduction.— Currently, there is much interest in III-V compounds for semiconductor devices. The two most widely-studied III-V semiconductors are GaAs and InP. Microwave devices fabricated on GaAs have been used for quite some time. Solar cells and integrated circuits made of GaAs and InP are being seriously investigated. These devices are commonly fabricated in a layer of material a few micrometers thick on the surface of a semiconductor wafer. The rest of the wafer, which is hundreds of micrometers thick, serves mostly as a supporting substrate. For large-scale applications of III-V compounds, the material costs and availability may become major problems for using these semiconductors as substrates. Therefore, there has been strong motivation to develop techniques for producing thin films of III-V compounds on inexpensive substrates. Before we begin to describe the thin films of III-V compounds, we have to clarify the definition of "thin films." Certainly, free-standing thin layers less than tens of micrometers thick should be called "thin films." Although strictly speaking homoepitaxial layers grown on single-crystal substrates may also be classified as "thin films", they are generally not. Heteroepitaxial thin layers grown on substrates of different materials, e.g., thin single-crystal GaAs layers grown on single-crystal Ge substrates, should be so classified. Depending on the substrate properties and growth conditions, thin films can be either single-crystalline, polycrystalline or amorphous. We will first discuss single-crystalline films, then polycrystalline films. Amorphous films are outside the scope of this paper. We will concentrate on GaAs and to a lesser extent InP; however many of the comments should also be applicable to other III-V compounds.

2. Single-Crystalline Films.— There are two basic techniques in obtaining thin single-crystalline III-V films. One technique is to grow these films directly on single-crystal substrates of materials which have similar crystal properties (Fig. 1). For example, we have succeeded in growing GaAs films by chemical vapor deposition (CVD) on single-crystal Ge substrates,1,2 or Ge-coated Si substrates.3,4 When bulk Ge substrates were used, the GaAs layers were found to contain very few defects, since Ge and GaAs have almost identical lattice constants and thermal coefficients of expansion. Thin-film GaAs solar cells on Ge, which have a GaAs epilayer only 4 micrometers thick, have already attained1,2 conversion efficiencies as high as 21% at AM1, similar to the cells obtained on GaAs epilayers grown directly on GaAs substrates.
The primary motivation for investigating Si as a substrate material for GaAs growth has been to lower the cost of efficient GaAs solar cells. A major reduction in cost would be achieved if such cells could be produced on inexpensive Si sheets that are currently being developed for low-cost Si cells. In addition, the development of monolithic GaAs/Si integrated circuits will require the preparation of GaAs epilayers on Si. However, attempts to grow such epilayers directly on Si by CVD have been largely unsuccessful because of difficulties in nucleation, which are also encountered in GaP deposition on Si.\(^5\) (GaAs epilayers have been deposited directly on Si by ion-beam sputtering.\(^6\) However, no devices have been reported on these layers). We have overcome these difficulties by coating Si substrates with a thin epitaxial films of Ge before GaAs deposition. Since Ge and GaAs have almost the same lattice constant, this procedure also has the advantage of locating the lattice mismatch (~ 4%) at the Ge-Si interface, away from the GaAs layer.

Figure 2 is a schematic diagram summarizing the dislocation densities determined by transmission electron microscopy for the GaAs/Ge/Si structure.\(^7\) The
Si substrate was characterized by transmission x-ray topography both before and after GaAs deposition and was found to have a very low dislocation density. Misfit dislocations generated at the Ge-Si interface result in threading dislocations that propagate up through the Ge film. The GaAs-Ge interface acts as a barrier to these dislocations, the majority of which bend over and become part of a dislocation network at this second interface, leaving a dislocation density of about $10^7$ cm$^{-2}$ in the GaAs layers. This relatively high dislocation density increases the p-n junction leakage current. Therefore, the conversion efficiency of such cells is only about 12% at AM1. Although further decrease in dislocation densities must be achieved before better solar cells can be fabricated, these cells are the first reported thin-film GaAs devices of any type to be fabricated on Si substrates.

A second characteristic of the GaAs layers on Ge-coated Si substrates is the presence of cracks. Since the thermal expansion coefficient of GaAs is roughly twice that of Si, these layers are placed under tensile stress by the substrate during cooling from the growth temperature. Cracking due to such stress has also been observed in other systems, including GaP on Si\textsuperscript{8} and InGaP on GaAs.\textsuperscript{9} The most serious effect of cracks in the GaAs layers on Ge-coated Si occurs during the cell fabrication procedure. The junction will be shunted if the underlying GaAs exposed by a crack is plated with metal contacts.

Heteroepitaxy InP films have been grown by liquid-phase epitaxy on a variety of ternary and quaternary substrates,\textsuperscript{10,11} mainly for optical laser applications. In general, the lattice matching was kept to within 1% so as to keep the misfit dislocation density low.

Another approach in obtaining thin single-crystal films is the peeled-film technology. The basic idea of peeled-film technology is to grow a thin single-crystal epilayer on a single-crystal mold, to separate the epilayer from the mold, and then to use the mold again (see Fig. 3). This technique is especially advantageous for solar cells, such as GaAs or InP cells. Conventional GaAs cells consist of an epitaxially grown active layer less than 5 μm thick, and a GaAs or Ge substrate wafer 250-400 micrometers thick.\textsuperscript{1,2,12} The substrate wafers are cut from melt-grown single crystal so that cutting and polishing losses further increase the total quantity of semiconductor material used in solar cell preparation. If reusable substrates can be used for growth of the active region, the quantity of semiconductor material consumed will be drastically decreased. Furthermore, the elimination of the semiconductor substrate from the cell should result in a significant weight reduction, an important advantage for space applications. A chemical peeled-film technique has been reported\textsuperscript{13} for GaAs. A thin single-crystalline GaAs film was deposited by molecular beam epitaxy on a GaAlAs layer about 5 micrometers thick grown on a GaAs substrate. The GaAlAs intermediate
layer was removed by selective etching with HF introduced through small openings at the edge of the substrate, and the GaAs film was then separated from the substrate. Conversion efficiency of 13.5% has been achieved for GaAlAs/GaAs heteroface solar cells using GaAs films ~ 50 micrometers thick separated by this chemical technique. Such a technique is inconvenient, however, even if the intermediate layer is relatively thick, since it is difficult to circulate an etchant through the small openings. The CLEFT process is an alternative technique that provides a practical way of separating epilayers from their substrates.

The key element of the CLEFT process is the use of lateral epitaxial growth performed in an AsCl₃-Ga-H₂ reactor. Our experiments have shown that if a mask with appropriately spaced stripe openings is deposited on a (110) GaAs substrate, the epitaxial growth initiated on the GaAs surface exposed through the openings will be followed by lateral growth over the mask, eventually producing a continuous single-crystal film that can be grown to any desired thickness. The upper surface of the film is then bonded to a secondary substrate of some other material. If there is poor adhesion between the mask material and the GaAs, the film will be strongly attached to the GaAs substrate only at the stripe openings. Since a weak plane has been created by the mask and because the (110) plane is the principal cleavage plane of GaAs, the film can be cleaved from the GaAs substrate without degradation of either. We have found that carbonized photoresist is a suitable mask material, since it has the necessary poor adhesion to GaAs and is chemically inert under the conditions that we employ for CVD growth. Reference 15 also describes several alternate mask materials and configurations.

The technique used for separating the GaAs film from the GaAs substrate is illustrated by the schematic diagram shown in Fig. 4. The upper surface of the film is bonded with epoxy to a glass secondary substrate. The GaAs and glass substrates are then bonded to glass plates that serve as cleaving supports. A wedge is inserted between the two glass plates and tapped gently, causing the GaAs film to be cleaved from the GaAs substrate but leaving it mounted on the glass substrate. Finally, the GaAs primary substrate is removed from its glass cleaving support plate, leaving it ready for another cycle of the process.

As a demonstration that the CLEFT process can be used to prepare multiple GaAs films, we have carried out four CLEFT cycles with the same single-crystal GaAs substrate. Four successive films of excellent quality were obtained, with thicknesses of 5, 10, 10, and 8 micrometers, respectively. The area of each film is about 4 cm². The films prepared and separated in this manner have been shown by Hall measurements to be comparable in quality to conventional single-crystal CVD layers.

The dislocation density of the CLEFT films was investigated by transmission electron microscopy, dislocation etching and scanning cathodoluminescence. These studies showed that the CLEFT films have very few defects, with a dislocation density lower than 10⁴ cm⁻², and no defects were observed at the intersections.
between growth fronts. Some doping non-uniformity was observed at the initial phase of growth, but doping was uniform when the films became continuous.\textsuperscript{16}

In a demonstration of the applicability of the CLEFT process to solar cell fabrication, we first grew GaAs layers (n⁺/p/p⁺ structure) on (110) GaAs substrates that had been masked with carbonized photoresist and coated with 1000 Å SiO₂. (The surface morphology of GaAs CLEFT films is somewhat better when the SiO₂ coating is also used.) The surface was then bonded by epoxy to a cover glass, and the film was separated from the GaAs substrate. An electroplated Au contact was then made to the back surface. This procedure has been used to make three CLEFT cells, with GaAs films 10 micrometers thick, which have conversion efficiencies of 15 to 17% at AM1. The 17% cell has an area of 0.51 cm\(^2\) (Ref. 17).

Figure 5 is a schematic diagram of the cross section of a CLEFT solar cell. The structure of this cell is interesting in several respects. The entire thickness of GaAs is about 10 micrometers. The glass substrate supports the film and serves as the cover glass for the cell. Another advantageous aspect of the structure is that there are metal contacts on both sides of the GaAs film. This might simplify the construction of integrated circuits, since the problems of fabricating two levels of interconnect metallization might be reduced by applying one metallization layer on each side.\textsuperscript{16}

Since the CLEFT films have been found to contain few crystalline defects, these films should be useful for devices where high crystalline quality is required. In addition, CLEFT films can be bonded to insulating substrates, with potential applications for multi-level devices. In such applications, proper heat sinking will be a major obstacle.

Another potential application of the CLEFT process is the formation of structures in which films of different semiconductors are stacked on top of one another. Such structures could be utilized for tandem solar cells consisting of two or three cells with successively smaller bandgaps, which should have conversion efficiencies over 30\%.\textsuperscript{18}

The CLEFT process has the potential for being applied to the growth of many semiconductors. For example, by using the PC13-InP-H₂ method, single-crystal InP overgrowth on phosphosilicate glass has been found\textsuperscript{19} to be sufficient to obtain single-crystal sheets of InP for device applications. By using carbonized photoresist masks, CLEFT InP films have been obtained.\textsuperscript{20} No detailed electrical and structural characterization has yet been done on these CLEFT films.

3. Polycrystalline Films.- There has been much effort in developing low-cost III-V solar cells by depositing such semiconductors on conducting substrates, such as W or graphite. The use of such substrates results in polycrystalline III-V films. The solar cells obtained from these films have low efficiencies.\textsuperscript{21} The cells suffer low open-circuit voltage and fill factor, while the photocurrent is often comparable
to that of single-crystal cells. Therefore, there is a need to understand the mechanism of the grain boundaries in these compounds. We have proposed a simple model that can explain many of the results. The model is based on the observation that Fermi levels at GaAs and InP surfaces usually are pinned. The pinning effects have been attributed to surface states. Such surface states may be caused by metallic impurities, surface oxides, or gaseous absorption. The structural configuration may also be a source of the pinning. Although this pinning effect has been documented only for surfaces, we proposed that similar Fermi-level pinning occurs at defects (grain boundaries, slip planes, etc.) in III-V compounds. In GaAs, the Fermi level is found to be pinned below the middle of the energy gap, that is, closer to the valence band than the conduction band. Therefore, at thermal equilibrium, as shown in Fig. 6, the barriers that are produced by the pinning will be higher in n-type than in p-type GaAs. In this figure, the Fermi level is drawn so that it is pinned at the same location in both n and p type samples. In reality, the exact position of pinning can vary with the number and energy of the "quasi-surface" states at the defects, but the general trend is retained. The formation of the barriers implies not only that the flow of carriers is impeded, but that the high density of states in the gap (which cause the Fermi-level pinning) trap the mobile carriers and reduce the net conduction.

When the doping concentrations in these compounds are low, the double-depletion regions around the barrier are large, and the effects of the barriers are widely felt. The barriers will reduce the electrical conduction and the Hall mobility values. Since the Fermi level is pinned towards the valence band in GaAs, these detrimental effects are more noticeable in n-type GaAs than p-type GaAs. When the doping concentrations are increased, two phenomena occur that can reduce the effects of the defect barriers. With increasing concentration, the barriers become narrower and tunneling becomes more probable. In addition, the trapping centers can begin to be filled, i.e., the Fermi level at the defect becomes unpinned, resulting in a reduction in barrier height. At high doping concentrations (over $10^{19}$ cm$^{-3}$), the barrier effects are expected to be minor, and good electrical conduction results. The defects, however, may still have some detrimental effect on mobility.
For InP, the Fermi level at the surface has been found to pin very near the conduction band. Therefore in contrast to GaAs, the barrier heights at the defects will be much larger in p-type than in n-type material. In fact, it appears that the difference in barrier heights between p and n type is larger in InP than in GaAs (Fig. 6).

There is some evidence that suggests this model is correct. Results obtained on laser-annealed ion-implanted GaAs and InP samples strongly indicated that the defects in these materials affected the electrical characteristics exactly in the same manner proposed by the model. In addition, recent results on electrical properties of grain boundaries in n-type and p-type GaP bicrystals also suggest that the Fermi levels are pinned below the middle of energy gap in GaP. Although we are not aware that the surface states in GaP have been measured, the surface states in GaAs and GaSb have been found to be pinned as such. It is conceivable such pinning effects are prevalent in all Ga compounds.

In polycrystalline films, the most prevalent defects are grain boundaries (GB). It has been found that GBs in the same material can vary significantly in their electronic properties, and studies on GaP and GaAs have shown that these properties are influenced by both GB structure and composition. A systematic experimental study of these effects requires the availability of samples containing GBs that have different well-specified structures with geometries suitable for electronic characterization.

We have now developed a new technique that utilizes the lateral overgrowth process developed for the CLEFT process to grow bicrystal GaAs layers containing a tilt boundary with predetermined rotation axis, misorientation angle, and boundary plane. The geometric structure of the GB is therefore completely specified. The technique has been demonstrated by preparing a series of GaAs bicrystals with a [110] tilt boundary and a (111) boundary plane that differ only in misorientation angle.

The growth substrate is a composite consisting of two rectangular (110) GaAs wafers that are bonded along one side by means of a Pb-glass layer. The bonded side of one wafer is a (111) plane, while that of the other wafer is rotated from the (111) plane by the desired misorientation angle. The exposed interface between the two wafers in the (110) substrate plane is covered by a film of SiO₂ in the form of a narrow stripe that masks the Pb-glass layer and extends a short distance over each wafer. When the thickness of the GaAs epilayers exceeds that of the SiO₂, the layer on the wafer with the off-(111) side seeds lateral growth over the SiO₂; the layer on the other wafer does not, because it forms a bounding (111) facet. The overgrowth continues until the layers join to form the bicrystal, after which growth continues normally.

Bicrystal n-type layers containing GBs with misorientation angles from 0° through 30° have been grown. The properties of majority-carrier transport across the GBs have been evaluated by means of current-voltage (I-V) and capacitance-voltage measurements. The results are consistent with a double-depletion-region model for GB transport. The 0° boundary has an ohmic I-V characteristic and thus has no associated potential barrier. As the misorientation angle is increased, the I-V characteristics generally become increasingly non-ohmic until saturation is reached in the 24° to 30° range. The increase in barrier heights with increasing misorientation angles can be attributed to a corresponding increase in surface states at GBs. When the misorientation angle reaches about 30°, the structural effects on the density of surface states probably saturate. The effect of carrier concentration on GB properties is also being investigated by the growth of layers with identical GB orientations that are doped to different levels. We believe that GBs prepared by the lateral overgrowth technique can be used for the systematic investigation of the effects of GBs on the performance of polycrystalline materials. This technique should be applicable to other orientations and other materials that exhibit lateral overgrowth.
The advantage of studying oriented bicrystal layers is obvious, but so far polycrystalline films of GaAs\(^{30-32}\) and InP\(^{33-34}\) are usually composed of small crystallites, with a large variety of GB structures and compositions. Therefore, systematic studies on GB effects are difficult. However, a trend of the electronic properties of these films has evolved. In general, these polycrystalline films have high leakage current. Good Schottky-barrier junctions are hard to attain, while Metal-Insulator-Semiconductor (MIS) junctions are much better. These films also tend to have very poor p-n junction characteristics. These results can be explained in terms of our simple Fermi-level-pinning model. In GaAs, GBs are supposed to be pinned p-type, even if the layers themselves are n-doped (unless the layers are heavily n\(^+-\)doped). Since Schottky barriers on p-type GaAs have lower barrier heights\(^{35}\) than n-type GaAs, Schottky junctions on polycrystalline n-type GaAs have lower barrier heights, resulting from higher leakage currents induced at the intersections between the p-type GBs and the Schottky metals. In InP, GBs are always pinned to be n-type. Since the Schottky barrier heights in InP are lower\(^{35}\) for n-type than p-type, the leakage currents are also high for polycrystalline InP. In fact, it is very likely that GBs in other III-V compounds are also pinned either like GaAs or InP and Schottky-barrier junctions are always more leaky.

For MIS junctions, the thin insulating layer between the Schottky metal and semiconductor reduces the leakage current between the metal and GBs; thus the junction characteristics improve. In MIS devices, the insulating layer is continuous across the semiconductor. In fact, for passivating the shunting effects of the GBs, insulating caps are needed only at the intersection of GBs with the semiconductor surfaces. Such selective insulating caps can be conveniently formed by selective anodization.\(^{36,37}\) By electrolytically growing anodic-oxide caps on GBs in GaAs, much better solar cells were obtained in polycrystalline layers, with lower leakage currents. Another passivating treatment was a surface treatment with a ruthenium-based solution.\(^{38}\) This surface treatment is reported\(^{39}\) to have converted the chemical composition of the surface and grain boundaries, thus reducing surface recombination velocities in both GaAs and InP. Such a chemical treatment was performed on n-type finely-polycrystalline GaAs films grown on W-coated graphite substrates. Interestingly, not only was the cell voltage much improved, but the photocurrent was increased by as much as 30-40\%.\(^{32,39}\) This large increase in photocurrent was probably not just due to passivation of surface recombination at the GBs, but may be due to the fact that before passivation the GBs in n-type GaAs are p-type, greatly affecting the diffusion of photogenerated minority carriers to the junctions. This effect was found to be consistent with our results\(^{22}\) on ion-implanted, laser-annealed GaAs and InP cells. Therefore, based on the Fermi-level pinning model, it appears for polycrystalline optoelectronic devices such as solar cells, it is preferable to have a p-type active layer in GaAs. For InP, however, an n-type active layer is preferred. The proper choice is particularly important for finely-polycrystalline samples where the grain boundaries are not close to vertical, as illustrated in Fig. 7. The photogenerated carriers in the shaded areas of the figure have difficulty diffusing to the n/p junction.

![CONTACT FINGER](image)  
**Fig. 7.** Schematic diagram of an n\(^+/p/p^+\) solar cells fabricated from InP layers that contains many defects and/or grain boundaries.
For p-n junctions, Fermi-level pinning at the GBs also greatly increases the leakage currents of the junctions. Figure 8 shows an idealized polycrystalline n+/p/p⁺ GaAs solar cell on a conducting surface. As described earlier, GBs in GaAs are usually pinned to be p-type even in n⁺ layers (unless they are very heavily doped). The presence of p-type GBs in an n⁺ layer will greatly increase the junction leakage current and series resistance, lowering the open-circuit voltage and fill factor of the solar cells. To reduce the pinning effects, heavy incorporation of additional dopant atoms into GBs is preferable. For example, in the structure shown in Fig. 8, n-type dopant atoms, such as Sn, should be introduced. The technique has been shown to be successful for large-grained GaAs solar cells having a conversion efficiency as high as 13% at AM1. The diffusion of Sn along GBs must, however, not reach the conducting substrate, or otherwise the junctions will be shorted. This technique is illustrated in the expanded view shown on the right-hand side of Fig. 8. On the left-hand side, we have included an expanded view of selective anodic-oxide capping of GBs so that the metal contacts on the GaAs surface will not shunt the cells through the GBs. This anodic-oxide passivation is very similar to that used for passivation of GBs of Schottky-barrier cells, as discussed above.

In summary, Fermi levels at GBs of polycrystalline III-V compounds are most likely pinned similarly to the Fermi levels at surfaces. Because of the Fermi-level pinning effects, various electrical and device characteristics at GBs can be predicted. If the Fermi levels of the semiconductor are pinned below the middle of the energy gap, as in the case of GaAs, then the detrimental effects on electrical conduction are more noticeable in n-type than in p-type. In addition, for optoelectronic devices of this compound, it is preferable to have a p-type active layer. If the Fermi levels of the semiconductor are pinned above the middle of the energy gap, as in the case of InP, the detrimental effects on the electrical conduction will be more noticeable in p-type, and for optoelectronic devices, it is
preferable to have an n-type active layer. Furthermore, because of the Fermi-level pinning at GBs, the polycrystalline III-V layers often form poor p-n and Schottky junctions. A passivation scheme should be used. For Schottky-barrier junctions, either MIS or selective insulating-caps have proven to be quite successful. For p-n junctions, incorporation of dopant atoms of the opposite type to the conductivity associated with the GBs should be effective. Hydrogen passivation on GBs of III-V compounds, however, has so far been unsuccessful. This may be due to hydrogen not bonding very strongly with either Ga or As atoms, as suggested by evolution of hydrogen from hydrogenated amorphous GaAs films at temperatures as low as 150°C.41

4. Conclusion.- Single-crystalline and polycrystalline III-V films have been grown on various kinds of substrates. We have described several of these techniques and the properties of the resulting layers. A simple model has been proposed to explain their electrical and device characteristics. Various schemes for passivating the effects of grain boundaries in these films have proven to be successful.

References


20. P. Vohl, private communication.


DISCUSSION

D. EGER.- Did you find any correlation between the degree of the misorientation of the two crystallites and the leakage current along the grain boundary?

J.C.C. FAN.- Yes, but this is a part of the P.H. Thesis to be published later on. In any case, it appears that there are no dangling bounds for the GaAs grain boundaries.

R. SURYANARAYANAN.- You mentioned you used a dirty $p^+$ Si to grow Ge and GaAs. Was it single crystal dirty or poly crystal dirty?

J.C.C. FAN.- Currently, we are using single-crystal Si wafers. If we succeed in bringing the misfit dislocations down, we will go to dirty or polycrystalline Si wafers.

H.F. MATARÉ.- You showed clearly that a g.b. has a longitudinal conduction in spite of the thinness of the crystallographic layer (10-100 Å), since conduction goes through the space charge layer. Is the improvement of perfection due also here to lateral dislocation outgrowth?

J.C.C. FAN.- Yes!
M. RODOT.- Surface recombination velocity is very much lower in InP than in GaAs. Would it be the same for grain boundaries?

J.C.C. FAN.- Grain-boundary pinning effectively should be lower in InP than in GaAs, leading to lower recombination effects. However, because the Fermi levels are pinned very close to the conduction band, the barrier heights in p-type InP are very high.

G.O. MULLER.- 1) There are a lot of possibilities in this very interesting lateral overgrowth process of tilted crystals to form well defined bi-crystals e.g. the cleavage along the g.b. by moving the seed crystals against each other. Did you do, does it cleave along g.b., how does it look?

2) Did you measure wave-guiding attenuations in the layers you described, how do they compare?

J.C.C. FAN.- 1) No we have not cleaved along the grain boundaries and investigate. It is a good idea, and maybe we should try.

2) Yes, we have published in Applied Phys. Lett. in 1980, or 1981.

P. MANUEL.- Could you comment on the speed of the lateral growth process for solar cell production?

J.C.C. FAN.- In order to grow a 10 μm thick solar cell, you need about 70 min., and one half of this time is for the lateral growth itself. But of course it depends on the distance between the openings.

A. PARRETTA.- Which method do you use to grow monocrystalline films of germanium on silicon?

J.C.C. FAN.- By electron beam deposition the Ge film is about 0.1 μm thick.