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CHEMICAL AND ELECTRICAL CHARACTERIZATION OF POLYCRYSTALLINE SEMICONDUCTORS

L.L. Kazmerski and P.E. Russell

Solar Energy Research Institute, Golden, Colorado 80401, U.S.A.

Résumé - La composition et la chimie des régions entre et dans les grains des semiconducteurs polycristallins peuvent se rapporter aux et même dominer les caractéristiques électriques de ces matériaux et des dispositifs où ils sont utilisés. Dans cette étude, des techniques complémentaires de haute résolution pour l'analyse des surfaces, y compris la spectrométrie Auger (AES), la spectrométrie de masse par ions secondaires (SIMS), la radiospectrométrie photoélectronique (XPS) et la spectrométrie de perte électronique à basses énergies (EELS), sont employées pour examiner les propriétés de composition des grains et des joints de grains dans le silicium et dans le GaAs. Les positions des impuretés séparées aux joints de grains et d'autres défauts sont trouvées par spectrométrie Auger exploratrice ayant une résolution latérale de moins de 500 Å par combinaison avec une technique de fracture in-situ. Des comparaisons entre les régions dans les grains et entre les grains sont données. L'activité électrique de ces impuretés à l'intérieur du plan du joint de grains est évaluée par un mesurage modifié de spectrométrie Auger pour déterminer le potentiel de la surface. Les effets de l'illumination sur le potentiel de barrière et sur le temps de vie des porteurs minoritaires des joints de grains de silicium purs et intentionnellement dopés (Al, Ti, Cu) sont données. Les effets de la recuitaison sur les joints de grains de diverses impuretés sont discutés. Des résultats montrent que la ségrégation de l'oxygène aux joints de grains de silicium influe fortement sur l'activité électrique des joints de grains sont offerts. AES, EELS, SIMS et la microscopie ionique sont utilisées pour examiner la chimie des joints de grains ce qui indique que l'oxygène se déplace aux régions entre les grains pendant des traitements de chauffage à hautes températures. Des données des positions des ions (resolution ~ 1 um) sont données en fonction de temps et de temperature pour montrer la ségrégation de l'oxygène aux joints. Des données complémentaires des temps de vie de porteurs minoritaires et des mesurages du courant induit par rayons électroniques (EBIC) corroborent le modèle de la ségrégation de l'oxygène et indique que ce mécanisme est la cause probable de l'activation électrique de tels joints de grains.

Abstract - The chemistry and composition of inter- and intragrain regions in polycrystalline semiconductors can be related to, as well as dominate, the electrical characteristics of the materials, and devices fabricated from them. In this paper, high-resolution, complementary surface analysis techniques, including Auger electron spectroscopy (AES), secondary ion mass spectroscopy (SIMS), X-ray photoelectron spectroscopy (XPS) and low-energy electron loss spectroscopy (EELS), are used to investigate the compositional properties of grains and grain boundaries in Si and GaAs. Segregated impurities localized at grain boundaries and other defects are mapped using scanning AES with better than 500 Å lateral resolution, in conjunction with an in-situ fracture technique. Comparisons between grain and grain boundary regions are presented. The electrical activity of these impurities is evaluated...
within the grain boundary plane using a modified AES measurement to determine surface potential. The effects of illumination on the barrier potential and minority-carrier lifetimes of clean and intentionally-doped (Al, Te, Cu) silicon grain boundaries are presented. The effects of annealing on grain boundaries containing various impurities are discussed. Evidence is presented to show that oxygen segregation to silicon grain boundaries strongly influences grain boundary electrical activity. AES, EELS, SIMS and ion microscopy are used to investigate grain boundary chemistry — indicating that oxygen moves to the inter-grain regions during high-temperature heat-treatments. Direct ion mapping data (~1 μm resolution) are presented as functions of time and temperature to show the grain boundary oxygen segregation. Complementary minority carrier lifetime data and electron beam induced current (EBIC) measurements support the oxygen segregation model and identifies this mechanism as the probable source for electrical activation of such grain boundaries.

1. Introduction — Polycrystalline semiconductors have become important entities in the electronics industry, with applications ranging from passive micron-size interconnects using poly-silicon to active, cm-size solar cells using a variety of elemental and compound semiconductors [1,2]. Because of growing interests in their applications and in providing low-cost, device-quality semiconducting layers, research activities aimed at controlling and understanding the electrical behavior of grain boundaries have increased substantially in recent years [3-10]. The ability to predict the transport properties of polycrystalline semiconductors and the characteristics of polycrystalline devices has been enhanced by the development and refinement of modeling techniques. The control of grain boundary parameters by chemical methods has been demonstrated, including the utilization of H, Li and O in various semiconductor hosts [11,15]. These studies have further highlighted the importance of the chemistry of the grain boundaries in determining and controlling the electrical characteristics of these inter-crystalline regions. It is the purpose of this paper to focus on the correlation between the inherent chemistry/composition of grain boundaries in semiconductors, with the resulting electrical properties.

The extent to which grain boundaries affect the properties of a semiconductor depends upon several factors including grain size, grain boundary orientation, material treatment and semiconductor type. The intercrystalline regions can impede the flow of majority carriers, act as recombination centers for minority carriers, or provide electrical shunts across the polycrystalline layer. Which of these processes (or combination thereof) dominate differs, for example, from Si to GaAs, and within any single semiconductor type itself depending upon its history. It is apparent in the literature on polycrystalline semiconductors that all observations are not generalizations, but must be evaluated in terms of the processing, material and measurement conditions used [16].

This paper focusses on the properties of cast [17], large-grain Si, with some comparative examples presented from other Si types (e.g., CVD) and GaAs. In general, the Si grain boundary studies have a common (211) plane, with approximately a 30° mismatch in the (111) — planes. This common boundary type (determined by electron channeling and X-ray diffraction is classified as a medium-angle grain boundary, and provides a common basis of comparison.

The chemistry and composition of the grain boundaries are evaluated using surface analysis techniques, including Auger electron spectroscopy (AES), electron-energy loss spectroscopy (EELS), secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS). These methods, compared in Table 1, provide information from the topmost atomic layers of the material being analyzed and their utilization in the study of grain boundaries is emphasized. Results of these investigations are correlated with microelectrical characterizations of the same regions using electron-beam induced current (EBIC), minority-carrier lifetime, and specialized scanning AES techniques. The segregation of impurities to the intergrain
Table 1. Summary of Selected Surface Analysis Techniques

<table>
<thead>
<tr>
<th></th>
<th>AES</th>
<th>EELS</th>
<th>SIMS</th>
<th>XPS</th>
<th>UPS</th>
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</thead>
<tbody>
<tr>
<td>Probe</td>
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<td>electron</td>
<td>ion (+, -)</td>
<td>x-ray</td>
<td>ultraviolet</td>
</tr>
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<td>electron</td>
<td>ion (+, -)</td>
<td>electron</td>
<td>electron</td>
</tr>
<tr>
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<td>-300 Å</td>
<td>&lt;1 µm</td>
<td>10² - 10³ µm</td>
<td>-10³ µm</td>
</tr>
<tr>
<td>Depth Resolution</td>
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<td>5 - 50 Å</td>
<td>≥3 Å</td>
<td>5 - 50 Å</td>
<td>5 - 50 Å</td>
</tr>
<tr>
<td>Detection Sensitivity</td>
<td>0.1 at-%</td>
<td>0.1 at-%</td>
<td>&lt;0.001 at-%</td>
<td>0.1 at-%</td>
<td>0.1 at-%</td>
</tr>
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</table>

regions is investigated, including the properties of specific, intentionally-added species (e.g., Al, Ti, Cu in Si; Sn in GaAs). Grain boundaries are evaluated using these techniques both perpendicular to the planar defects, and within their plane using in-situ fracturing to expose them [18]. Finally, the effects of heat-treatment on the diffusion of O to the Si grain boundaries, and potential electrical activation, are reported.

2. Experimental Details - The compositional and chemical determination were performed primarily with surface analysis equipment. These include: (1) Perkin-Elmer/Physical Electronics model 595 Multiprobe, having better than 500 Å AES resolution, complementary SIMS, EBIC and EDS capabilities; (2) Perkin-Elmer/Physical Electronics model 590 Scanning Auger microprobe, with 1500 Å resolution, complementary SIMS and EBIC; (3) Perkin-Elmer/Physical Electronics model 550 XPS/AES system, with EELS, SIMS and EBIC; and, (4) CAMECA IMF-3f Ion microprobe, with Ce and O ion sources. AES measurements were typically taken under low current (~ 20 nA) conditions, using the pulse counting detection mode. XPS data were taken with a 10 kV (40 mA) X-ray source, configured with a Mg anode, utilizing a double pass cylindrical mirror analyzer 10 eV pass energy was used for high resolution. The EELS was done using the double-pass analyzer with an incident energy of 100 eV. A 0.5 eV modulation energy was used in these studies. Electron beam induced current studies were performed in-situ, as well as in a JEOL 35C SEM, equipped with digital imaging capabilities. Minority carrier lifetimes were determined using a spatially resolved surface photovoltage method [16,19]. Resolution was typically 15 µm, using a microfocussing stage. Measurements for the Si samples were taken over the range 0.88 < X < 1.0 µm, with better than a 5% reproducibility. Grain boundary potentials were determined under zero-bias conditions [5], using a four-terminal method and Keithley 616 electrometers. A filtered xenon lamp served as the illumination source for the photogeneration grain boundaries studies. The irradiation level was determined using a blackbody radiometer - with intensities accurate within 5%.

The polycrystalline Si was produced by casting [17]. The substrates were p-type (B-doped) with Na ~ 3 x 10¹⁶/cm³, with grain sizes 0.5-1.0 cm. Individual grain boundaries were isolated by cutting 1 mm - thick wafers. For some studies, small concentrations of Al, Fe and Ti (0.001 at. -%) were added during Si growth to determine the effects of these impurities. Samples were annealed in argon and the (600–900°C) to study the diffusion of various impurities. The heat-treatment was done either in a tube furnace with flowing Ar-gas or in the He-backfilled quartz ampoules. GaAs grain boundary samples were produced by molecular beam epitaxial growth on high-resistivity, Cr-doped substrates containing single-grain boundaries. Au was used to form a Schottky barrier to the GaAs for the EBIC studies. The thickness of this metal layer was typically 100-200 Å.

3. Results and Discussions - The interrelationships between the composition or chemical properties of grain boundaries and their measured electrical properties have been recently reported for polycrystalline silicon [16,18,20]. In these studies, the ability to demonstrate impurity localization at grain boundaries is
primarily due to the inherent surface sensitivity of the analysis methods and the relatively high spatial resolution of the electron and ion probes used [21,22]. The complementary approach used in these analyses allows not only multiple surface analysis techniques to provide compositional information on the same, specific areas, but also correlated electrical characteristics, and (in some cases), compositional properties of the bulk material. In this section, the analyses of grain boundary semiconductors are discussed. First, the detection and evaluation of impurities at grain boundaries are presented. The presence of these impurities are correlated with EBIC results, minority-carrier lifetime measurements, and illumination-grain boundary potential barrier studies. Second, the effects of impurity movement are indicated for heat-treated polycrystalline samples. Evidence for the activation of the intergrain regions due to oxygen segregation is presented.

(a) Grain Boundary Impurities: The direct evidence for the segregation of impurities to grain boundaries in cast and directionally solidified multigrained Si has been reported [18]. Since grain boundaries lie essentially perpendicular to the available wafer surface, they offer a low-profile for analysis, even by now-available surface analysis high resolution probes. In-situ fracturing has been demonstrated to be a successful method to expose these internal surfaces, providing larger areas for analysis and minimizing potential contamination from sorbed species [18]. Fig. 1 presents AES survey scans for a grain and grain boundary region, which have been exposed for side-by-side analysis by the fracturing method. Differences in the composition of the two regions are readily apparent. The intragrain is clean within the 0.1 at.-% detection limit of the AES technique. The boundary (Fig. 1) is seen to have several impurity species present, including C, O, F, Fe and Al. The chemical nature of the oxygen present is indicated to be primarily SiOx by the shape and position of the low-energy Si(KLL) transition [23]. Although the impurity species are easily detected on the grain boundary surfaces indicating compositions \(~ 10^{13}/\text{cm}^3\) in the regions, their compositions averaged over the entire bulk are typically in the range \(10^{11} - 10^{13}/\text{cm}^3\). This has been confirmed by bulk analysis of these materials [18].

The high-spatial resolution of AES can be used effectively to map the impurity concentrations on the surface being examined. This is accomplished by tuning the
spectrometer to one of the AES peaks - shown in Fig. 1 - and scanning the incident e-beam across the surface. An AES mapping sequence of a fractured Si boundary is presented in Fig. 2. This particular sample had 0.001 at. % Al added during the growth process in order to study its segregation mechanisms. The secondary electron detection (SED) image shows several contrasted features. The Auger maps of this same region give evidence of the impurities (C, O, P, Fe and Al) localized in this area. The localization on the grain boundary surface is illustrated by the depth-profile shown in Fig. 3 taken at point (a) of Fig. 2. The Si (SiKLL), Al and O signals diminish as a function of sputtering time until the grain material is reached (indicated by the emergence of the elemental SiKLL signal. Several aspects of the AES maps of Fig. 2 are noteworthy. The complementary positions of the Si and Si(SiOx) signals are evident. This may be a result of the fragmentation during fracturing. Oxygen containing grain boundaries are more likely to fracture than clean ones. In the Al maps, the AlKLL signal is more intense and covers a greater area than the AlKLL. This is accounted for by the difference in escape depths and sensitivity factors for these two transitions [21].

Several correlations between grain boundary impurity composition and the electrical response of these regions have been previously reported [16, 20, 24-36]. One method examined a given grain boundary first by EBIC to establish its electrical activity [20]. Subsequently, the boundary was exposed for compositional analysis by fracturing. This procedure is difficult, both from the ability to fracture the identical grain boundary region examined by EBIC, and from the certainty of identifying the impurities responsible for the electrical activity. Another method has utilized the direct measurement of the electrical properties of the grain boundary.
Fig. 3. Depth-compositional profile taken at point (a) indicated in Fig. 3.

Fig. 4. Electrical properties of grain boundary area shown in Fig. 2. (a) SED image; (b) Electrical potential mapping across regions a and b shown in SED. Impurities corresponding to AES signal changes are indicated. (From ref. 16).

along its length (i.e., within the boundary plane), and the direct correlation with the region's composition [16]. The analysis presented in Fig. 4 is for the same region shown in Fig. 2.

In this method, two Ag contacts (whose AES signal does not interfere with the detected impurities) are applied to the extreme edges of the grain boundary surface exposed by fracturing. A carbon film (~20-40 Å) is formed on the surface. The C(271 eV) signal is then monitored while stepping the incident electron beam across the surface (see insert, Fig. 4a). When the sample is biased via the Ag-contacts, the AES spectrum is shifted by an energy that is proportional to the applied bias and surface potential [27]. The observed shift in the carbon Auger peak position provides information on the relative surface potential. Assuming a uniform carbon layer (verified by AES depth-profiling), a correlation between electrical activity and specific impurities is gained. Two such scans are presented in Fig. 4b.

Further indications of exact impurity effects are provided by using light-generated processes. For polycrystalline solar cells, the effects of light on the grain boundary properties are particularly important. Fig. 5 presents the consequence of illuminating a p-type grain boundary in terms of the band diagram. For the dark case, the states are filled (in equilibrium) to the Fermi level, and band-bending results to preserve charge neutrality (double-depletion layer). Under illumination, the interface states adjust their charge by initial capture of minority carriers. This, in turn, reduces to diffusion potential and results in the
maximum recombination rate. Effects of uniform illumination on the barrier heights ($q\phi_b$), recombination velocity, photogeneration rates, and conductivity of grain boundaries in Si have been previously reported [33,29]. Seager has provided a thorough theoretical and experimental evaluation of light effects at grain boundaries [3]. It was predicted and verified that grain boundaries with large ($>0.4$ eV) barrier potentials are very sensitive to even low-level illumination. Conversely, barriers with small $q\phi_b$ are relatively light-insensitive, since very small readjustments of the barrier heights produce substantial excess hole (electron) currents for recombination with collected electrons (holes). These regions which are relatively conductive remain loss sites for photogenerated carriers.

Fig. 5. Energy band diagrams in vicinity of grain boundary in p-type material, (a) dark case; (b) illuminated case.

Fig. 6. Grain boundary barrier height dependence upon illumination (0.001 to 0.1 suns) for various clean and impurity-containing intergrain regions. Annealed samples were processed at 900°C for 20 min.
The effects of the impurity content of the grain boundary on the barrier heights and the illumination effects are illustrated in Fig. 6. These data involve a set of Si samples prepared with: (i) no additional impurities added (clean); (ii) with 0.001% Al added; (iii) with 0.001% Ti; and, (iv) with 0.0004% Cu. Compositional analysis showed that these impurities did accumulate in the intercrystalline boundary region. The effect of illumination on the barrier heights are presented in Fig. 6. The measurement of \( q_\Phi \) was made according to the zero-bias conduction method [5]. As expected [3], the barrier potential of all sampled grain boundaries decreases with increasing illumination, over the 0.001 to 0.1 sun range. The data on clean grain boundaries (Fig. 6(a) and (a')) follows the predictions and observations of Seager [3]. In general, the unannealed grain boundaries had lower measured values of \( q_\Phi \) (measured in the dark) than the same region after annealing (typically, 900°C, 20 min). The higher barrier height for the annealed case is also more light sensitive than its lower barrier counterpart. The higher barrier potential provides a larger attractive field, making the depletion layer edge a region of very high minority carrier collection.

Fig. 7. Minority-carrier lifetime line maps over Si grain boundaries of Fig. 5.

The effect of adding impurities to the grain boundaries is, in general, to increase this carrier collection process [16]. This is observed by comparing the data for segregated Al, Ti, and Cu, in Fig. 6, with the clean boundary case. For each impurity situation, the barrier height increases, as does the field at the space charge layer edge. Although the segregation coefficients of Al, Cu and Ti, do not differ greatly, and the relative concentrations of each species at the grain boundary are approximately the same (~ \( 10^{17} \text{cm}^{-3} \)), the effects of Ti and Cu are more pronounced since they act as more efficient minority-carrier lifetime sinks than Al [16]. This is further illustrated in Fig. 7 which presents a series of minority-carrier lifetime scans across the grain boundaries presented in Fig. 6. It is apparent that the three unannealed samples (Figs. 7(a), (b), (c) and (d) show a lower lifetime for the intergran regions with the intentionally added impurities. Again, the lifetimes for the Ti and Cu cases are significantly lower. These data correlate well with the grain boundary barrier height measurements of Fig. 6 and the predictions of Seager. Note that some effect in the grain regions for the Ti and Cu
cases can be observed in Fig. 7, indicate that some portions of these impurities do not segregate efficiently during the casting process.

The segregation of impurities to grain boundary regions can be observed in different growth techniques and in different semiconductors as well. Figure 8 shows $q_\Phi$ vs irradiation data for a grain boundary in GaAs for two cases: (a) clean; (b) with Sn added during MBE growth. These layers are both 1.0 \mu m thick, grown on a Cr-doped, high resistivity substrate having a single low-angle grain boundary. An AES map (Fig. 9) clearly shows the Sn accumulation for the Sn-doped case. The minority carrier lifetimes of these two grain boundaries were evaluated using a picosecond laser (mode-locked, cavity-dumped operation, with $\lambda = 0.832 \mu m$)

![Gallium Arsenide Grain Boundaries](image1)

**Fig. 8.** Grain-boundary barrier height dependence on irradiation for (a) undoped, and (b) Sn-doped regions in GaAs.

![Gallium Arsenide Grain Boundaries](image2)

**Fig. 10.** Grain-boundary height dependence on irradiation for (a) undoped, and (b) Sn-doped regions in GaAs.

![GaAs](image3)

![Sn](image4)

**Fig. 9.** Secondary electron image and AES Sn-map of GaAs boundaries measured in Fig. 8.

and measuring the photoluminescent decay via single photon counting methods [30]. The effect of Sn in lowering the lifetime at the grain boundary is evident in Fig. 10.
Unheated

Fig. 11. EBIC maps for grain boundaries in polycrystalline Si for unheated, 600°C and 750°C anneals showing increased electrical response with heat-treatment.

(b) Annealing and Oxygen Segregation: The electrical activity of some grain boundaries in cast polycrystalline Si has been reported to be strongly affected by heat treatments [16, 24, 31-33]. Redfield [32] observed this using liquid crystal detection techniques. Figs. 6 and 7 also indicate such properties. In each case, the heat-treated grain boundary had a higher value of \( q_{\text{p}} \), and a corresponding lower measured value of \( T \). EBIC data also confirm this heat-treatment effect. Fig. 11 presents a series of EBIC maps for a region of several grain boundaries, for unannealed, \( T = 600°C \) and \( T = 750°C \) heat treatments in Ar. The minority carrier collection can be seen to increase significantly at the higher annealing temperatures. Fig. 12 shows individual EBIC line scans across the grain boundaries of Fig. 11 (i.e., (a) unheated; (b) heated to 600°C; and (c) heated to 900°C) [24]. These data contain further information on the electrical properties of the boundary region. The slope of the lnI vs. EBIC scan for the 900°C grain boundary anneal (≈ 0.08 μm⁻¹) is considerably larger than for the 600°C case (≈ 0.02 μm⁻¹). Assuming that the diffusion coefficient is the same for both samples, the value of the effective surface recombination velocity, \( S_{\text{eff}} \), for the grain boundary heated to 900°C is approximately four times larger than the lower temperature case. Russell, et al. [24] have used the EBIC linescan technique to determine the grain boundary recombination velocity and effective minority carrier diffusion length as functions of these heat treatments. Statistically, the data show an increase in \( S_{\text{eff}} \) and decrease in \( L_{\text{eff}} \), both as functions of time and temperature for these Si grain boundaries.

The activation of these grain boundary regions has been attributed to either the movement of impurities to the grain boundary, or away from it. Fig. 13 presents SIMS data taken on fractured grain regions, before and after annealing. A signifi-
Slope = 0.007/μm  
(a) Unheated

Slope = 0.02/μm  
(b) 600°C 30 min

Slope = 0.08/μm  
(c) 900°C 30 min

E_p = 45 keV

Silicon
Grain Boundaries

Fig. 12. EBIC linescans across (a) unheated (b) 600°C, 30 min, and (c) 900°C, 30 min heat-treated grain boundaries indicating increase in electrical activity of these regions with heat-treatment.

cant increase in the SiO⁺, SiOH⁺, and Si₂O⁺ signals is observed after heating (900°C, 201 min.), indicating the segregation of oxygen to these internal surfaces. Also shown in SIMS data for an annealed Al-containing grain boundary. Almost no change in the oxide species response was observed. This is consistent with the measured electrical properties of such grain boundaries (see Figs. 6 and 7).

In addition, the grain boundary surfaces were examined by fracturing and SIMS depth-compositional profiling. The results are shown in Fig. 14(a). Some oxide is observed on the unannealed boundary surface. By comparison, however, a more pronounced oxide layer is measured on the annealed surface. Since the data were taken under identical conditions, the relative depths and Si-O coverage can be qualitatively compared. In order to ensure that those differences were not due to artifacts of the fracture procedure, both sides of the fractured surface were examined. This painstaking procedure resulted in the two sets of data shown on each depth profile. For this particular grain boundary, a minority carrier lifetime scan was also recorded (before fracture) in Fig. 14(b). The annealed grain boundary has a lower τ, which complements both the EBIC and the SIMS data. Further evidence of the oxide present at this grain boundary is presented by the XPS and EELS data of Figs. 15 and 16. Fig. 15 presents angle-resolve XPS data for both a fractured, unheated grain boundary, and one heated at 900°C. The Si-2p signals are shown as a function of the effective analyzer acceptance angle, θ. EELS data, shown in Fig. 16, also indicates the differences in the unheat-treated and heat-treated grain boundaries. The loss peaks associated with the oxide species are easily observed (shaded regions) in the annealed grain boundary case. Therefore, the origin of the enhanced grain boundary electrical activity in heat-treated polycrystalline Si is due to the
Fig. 14. Si grain boundary: (a) SIMS depth-profile (annealed and unannealed). Data for both sides of fractured region are presented; (b) Minority carrier lifetime scan for each region. (From ref. 16).

Fig. 13. SIMS data for annealed and unannealed and unannealed boundaries, (a) no intentional impurities, (b) with Al.

Fig. 15. Angle resolved XPS data showing oxygen at fractured grain boundary.

Fig. 16. EELS data for (a) annealed (showing oxygen peaks); and (b) unannealed Si grain boundaries.
segregation of the oxygen to the intercrystalline boundary regions. A final illustration of this effect is shown in Fig. 17, which presents a SIMS map of oxygen on a polycrystalline Si sample annealed at 900°C. The accumulation of oxygen at the boundary region (intersection of the grain boundary with the wafer surface) is readily apparent. It must be stressed that not all grain boundaries exhibit the enhancement in electrical activity after annealing. This may well be due to other impurity effects—such as those discussed previously in this paper—or to crystallographic properties of the grains and grain boundaries.

4. Summary—The compositional and chemical properties of Si and GaAs grain boundaries have been correlated with their microelectrical characteristics. The usefulness and importance of surface analysis methods (scanning AES, EELS, SIMS, XPS) in determining the composition of these intergrain regions have been demonstrated. Several micro-area-techniques have also been reported that provide information on the electrical properties of the same regions compositionally analyzed. In general, the composition of the grain boundary has been shown to be a controlling factor in determining both materials and device properties.

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References

DISCUSSION

H.F. MATARÉ.- 1) The actual crystallographic width of a grain-b. is of the order of 10 to 100 Å. EBIC and other electronic tests show width of a factor 100 to 1000 greater. Also your AUGER, SIMS, ESCA - tests show large areas. How do you explain this discrepancy?

2) Heat treatment often also decreases the g.b. barrier, in accidently grown wacker material all this is less controllable than in monocrystals with one g.b. (bicrystals).

L.L. KAZMERSKI.- 1) The AES and SIMS analysis indicate an impurity-width of 30-60 Å, based upon the knowledge of the sputter ribs of the materials. Indeed, the surface photovoltage (minority-carrier lifetime) in Si shows a much greater width, but due primarily to the inability to focus the light source to less than ~12 µm. Therefore, an integrating effect across the boundary is encountered, making the width appear much larger than it actually is. Some similar effects accompany the EBIC measurements, although the probe width and area analyzed are much closer to what is expected.

2) The analysis of bicrystals provides a more controllable experimental condition. However, this work was concerned primarily with those grain boundaries encountered in actual solar cell devices.
1) In the first AES spectra you showed, the grain was pure Si and at the boundary there was essentially no pure Si, all was oxidized. Does this mean that oxygen diffuses from the air to the grain boundaries?

2) How do you determine, a-priori, which region of zone broken surface corresponds to bulk material, and which to grain boundaries?

L.L. KAZMERSKI.- 1) These AES data were taken with a background pressure $\sim 10^{-10}$ torr in the analysis chamber during and after fracture. All hot filaments (e.g., the ionization gauges) were off during the process. Beam currents on the AES were low (> 30 nA, pulse-counting) to minimize the event of e-beam induced oxidation. The fact that the adjacent grain data of Fig.1 shows no oxygen supports the condition that the oxide was not measurement-induced. The source of the oxygen is thought to be defects within the grains (e.g., dislocations, etc.). The heat-treatments themselves were performed in non-oxygen containing environments.

2) The process involved examination before and after fracture in optical and scanning electron microscopes. This examination of the topography, especially the intersection of the grain boundary with the surface, was the basis for determining whether the fracture was through the boundary or through the grain.

M. MAUTREF.- Do you study and notice any influence of the heating and cooling rate for annealing processes at a same temperature and time duration?

L.L. KAZMERSKI.- Ce point n'a pas été particulièrement étudié.