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INSULATOR PHYSICS AND ENGINEERING: ELECTRICALLY-ALTERABLE READ-ONLY-MEMORY APPLICATIONS

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Abstract: - Current advances in the study of insulating materials, in particular SiO₂ and Si-rich SiO₂, have led to new types of electronic devices. Si-rich SiO₂, if placed between a contacting electrode and SiO₂, has been demonstrated to give enhanced electron injection into the SiO₂ layer at moderate average electric fields. This phenomenon is believed to be due to localized electric field distortion at the Si-rich SiO₂–SiO₂ interface caused by the two phase nature (Si and SiO₂) of the Si-rich SiO₂ film. Chemically-vapor-deposited layers of Si-rich SiO₂, SiO₂, and Si-rich SiO₂ have been used to charge and discharge floating poly-crystalline Si storage layers in a new type of non-volatile electrically-alterable memory.

I. Introduction

Several recent publications have demonstrated that high electronic current injection into SiO₂ can be achieved at moderate average electric fields by interposing a thin Si-rich SiO₂ layer (50-300 Å in thickness) between SiO₂ and a contacting electrode.1 Data demonstrating this phenomenon are shown in Fig. 1 where a control structure (without the Si-rich SiO₂ layer present) is compared to several structures with Si-rich SiO₂ layers of varying composition. For these structures the SiO₂ was thermally grown from the Si substrate and the Si-rich SiO₂ layer was chemically-vapor-deposited (CVD) from N₂O and SiH₄ gaseous reactants.

The Si-rich SiO₂ material has recently been shown to be composed of at least two phases (Si and SiO₂) using transmission-electron-microscopy (TEM).5 Raman spectroscopy,6 x-ray diffraction,3,4 and x-ray photoelectron spectroscopy (XPS).3,4 This two phase nature of the Si-rich SiO₂ is believed to cause the observed electronic current enhancement by locally increasing the electric field near (within 50 Å) the Si-rich SiO₂–SiO₂ interface. The curved surfaces (as compared to the normal planar surfaces of most contacting electrodes) of the last layer of interfacial Si islands in the Si-rich SiO₂ layer are believed to create the field distortion as depicted in Fig. 2 using energy band diagrams. The field-enhanced electron current has been shown to obey a Fowler-Nordheim tunneling mechanism which is highly non-ohmic and strongly dependent on the electric field near the injecting interfaces.1,7

The data in Fig. 1 is obtained using a structure where one layer of Si-rich SiO₂ under the top gate electrode is used to give enhanced electron injection only under negative gate voltage polarity. Figure 3 shows two other variations of Si-rich SiO₂–SiO₂ structures which have been demonstrated to give enhanced electron injection for positive (Fig. 3b) gate voltage polarity where the Si-rich SiO₂ injecting layer is between the Si.
substrate and SiO₂ or for either positive or negative polarity where a stacked structure of Si-rich SiO₂-SiO₂-Si-rich SiO₂ is sandwiched between the Si substrate and top contacting gate electrode. The structures in Figs. 3a and 3b are called single electron injector structures (SEIS’s) while that in Fig. 3c is called a dual electron injector structure (DEIS). A previous publication has demonstrated that the sum of the dark current as a function of gate voltage characteristics for the structures in Figs. 3a and 3b essentially add to give those characteristics observed for the structure depicted in Fig. 3c. A distinct asymmetry has been observed between the current-voltage characteristics of DEIS’s for positive and negative gate voltages in which positive polarity gives higher electron currents for the same applied average electric fields. This asymmetry is independent of whether the top gate contact is Al or poly-crystalline Si (poly-Si), or whether the bottom substrate contact is single crystal Si or poly-Si. It is believed to be due to microscopic differences in the Si-rich SiO₂ interfaces of the bottom and top injectors.

II. Applications

A. DEIS Memories

A particular application of the electronic properties of a DEIS stack has recently been demonstrated in the area of non-volatile electrically-alterable read-only-memory (EAROM). The basic device configuration of this structure is shown in Fig. 4. It is essentially an n-channel field-effect-transistor (FET) with a floating poly-Si storage layer which is charged or discharged by means of the DEIS stack separating this floating gate from a top control gate electrode. The voltages used to "write" (put electrons on the floating poly-Si layer by means of the top injector) or "erase" (take electrons off the floating poly-Si layer by means of the bottom injector) the device are always larger than those used to "read" the FET. The read operation is performed by sensing the electron current flowing from the source to the drain for a constant gate voltage bias (usually $\approx +5$ V). The internal electric field caused by negative charge on the floating poly-Si layer would shut off the channel and no drain current would be measured. An uncharged or positively charged (due to ionized donors) floating gate would cause the device channel to be turned on for the set reading voltage. Therefore, the charge state of the floating poly-Si layer performs a memory function.

Figure 5 shows typical cycling data for a DEIS EAROM where the FET threshold voltage is used as a measure of the charge state after the device has been written or erased with the values of voltage indicated. These values of write/erase voltage are some of the lowest values ever recorded for an EAROM structure. The threshold voltage window in Fig. 5 starts to significantly collapse after approximately $10^4$ cycles. This collapse is due to electron trapping on energetically deep sites in the intervening CVD SiO₂ layer. The internal electric field due to the negative trapped space charge build-up on these sites reduces the electric fields near the injecting Si-rich SiO₂ interfaces of the DEIS. The electron trapping sites are believed to be due to bonded OH and H₂O incorporated into the film during deposition. Figure 6 shows that a 1000°C anneal in N₂ for 30 min after DEIS stack deposition reduces the density of some of the trapping sites and allows the device to be cycled somewhat more than one order of magnitude more times.

The DEIS EAROM’s described here have been shown to have excellent charge retention at low fields for either positive or negative stored charges on the floating gate. Retention of electrons is controlled by either thermally activated electron
emission from the floating poly-Si (at temperatures $\geq 200^\circ$C) or Fowler-Nordheim emission from the bottom Si-rich SiO$_2$ injector at low temperatures and high internal electric fields.$^{(2,9,10)}$ Retention of positive charges (ionized donors) is controlled by injected electron compensation by either thermal emission (at high temperatures) or by Fowler-Nordheim tunneling (at high fields) from the top Si-rich SiO$_2$ injector.$^{(9)}$

DEIS EAROM's have been shown to have excellent breakdown characteristics, particularly when the structure is designed using capacitive coupling considerations to have most of the applied voltage dropped across the DEIS stack.$^{(2,9,10)}$ This phenomenon is due to the ability of the Si islands in the Si-rich SiO$_2$ layers closest to the contacting electrodes to build up a reversible space charge when a localized point at the contact-insulator interface starts to inject charge due to particulate or roughness at this interface.$^{(2,9,10)}$

The capacitance of the DEIS stack for $\approx 13\%$ excess atomic Si in the Si-rich SiO$_2$ injectors has also been shown to switch from a low to high value with increasing electric field.$^{(1,7)}$ This phenomenon is due to the collapse of the electric field in the Si-rich SiO$_2$ regions as the Si islands fill up with space charge.$^{(1,7)}$

DEIS stacks have advantages from the aspect of processing tolerances. It has been shown that the amount of excess Si (for amounts $\geq 13\%$ atomic Si) and the thickness of the Si-rich SiO$_2$ layer (for thicknesses from 100 to 1000 Å) are not very critical in getting reproducible current vs. voltage characteristics.$^{(2)}$ Although high temperature annealing or processing has been shown to convert the amorphous Si islands into crystallites,$^{(4-6)}$ the electrical injection characteristics are again essentially unchanged provided the DEIS stack is not directly exposed to an oxygen containing ambient.$^{(1)}$ These flexible characteristics of the DEIS make it ideally suited for a manufacturing environment.

B. Charge Trapping Studies

Another application of Si-rich SiO$_2$ injectors has been demonstrated in the area of charge trapping studies in SiO$_2$ on either sites normally present or purposely introduced.$^{(7)}$ The injector is used as a means of obtaining large electron injection into the SiO$_2$ conduction band at moderate average bulk SiO$_2$ electric fields. Usually, electrons are injected at moderate fields by using internal photoemission which requires semi-transparent gate electrodes and ultra-violet light$^{(11)}$ or by avalanche injection from the Si substrate which requires driving the Si into deep depletion with a repetitive pulse train until avalanche multiplication occurs.$^{(11)}$ Using injectors as a source of electrons and ramping the gate voltage at a constant rate yields current-voltage curves with ledges caused by charge trapping.$^{(7)}$ The current position and voltage width of these ledges gives the magnitude of the capture cross section and the total number of traps weighted by a centroid factor.$^{(7)}$ Centroid position can be determined using ledge widths from ramped current-voltage curves for both voltage polarities if DEIS structures are used. If a SEIS structure similar to that depicted in Fig. 3a is used, the centroid position can be obtained from the voltage ledge determined under electron injection from the top Si-rich SiO$_2$ injector and from the flat-band voltage shift observed using capacitance-voltage measurements before and after the ramped current-voltage measurement.$^{(7)}$ There is an advantage in using Si-rich SiO$_2$ injectors and ramped current-voltage measurements to determine charge trapping parameters as opposed to the other techniques such as photocurrent-voltage (photo I-V)$^{(11)}$ and capacitance-voltage (C-V) with flat-band voltage tracking.$^{(11)}$ This advantage is speed which allows a large number of capacitors to be studied.
III. Conclusions

Several uses of stacked layers of insulators such as Si-rich SiO₂ and SiO₂ with unique electrical properties have been discussed. Si-rich SiO₂ injectors have been used both in advancing our understanding of the physics of charge trapping in SiO₂ layers and in creating a new type of non-volatile EAROM. Insulator engineering should produce other novel devices in the future as our knowledge of stacked layers of two phase materials and insulators is expanded.

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Fig. 1. Point by point magnitude of the dark current as a function of negative gate voltage on MIS structures with various stacks of Si-rich SiO₂ on top of thermal SiO₂. In this measurement, the gate voltage was stepped by -2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si-rich SiO₂ layer was either stepped or graded with R₀, defined as [N₂O]/[SiH₄] as an indicator of the Si content of this layer. R₀ from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO₂ layer (R₀ = 10 + 3) or when a graded layer was used (R₀ = 10 → 3). Taken from Reference 1.

Fig. 2. Schematic energy band representation of conduction in the Si-rich SiO₂ layer via direct tunneling between isolated Si regions in the SiO₂ matrix of this two phase system and subsequent high field injection into the underlying SiO₂ region due to local electric field enhancement caused by the curved surfaces of the Si regions. Electronic Fowler-Nordheim tunneling into SiO₂ from a planar Si surface is shown for comparison. Taken from Reference 2.
Fig. 3. Schematic representation of a) SEIS with a Si-rich SiO$_2$ injector on top of the SiO$_2$ layer and under the control gate electrode, b) SEIS with a Si-rich SiO$_2$ injector on top of the Si substrate and under the SiO$_2$ layer, c) DEIS with a Si-rich SiO$_2$–SiO$_2$–Si-rich SiO$_2$ stack sandwiched between the Si substrate and the control gate electrode.

Fig. 4. Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, $V_{g^-}$ ($V_{g^+}$), to the control gate which injects electrons from the top (bottom) Si-rich SiO$_2$ injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale. Taken from Reference 8.
conditions on DEIS FET's from wafer MDT-DIS 3-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FET's before cycling. The DEIS stack in these FET's consisted of deposited layers of 100 Å of Si-rich SiO₂, 100 Å of SiO₂, and 100 Å of Si-rich SiO₂ where the Si-rich SiO₂ layer had 46% atomic Si. The floating and control gates had equal areas of $8.4 \times 10^{-6}$ cm² and the gate oxide from the floating poly-Si layer to the Si substrate was 100 Å in thickness. Taken from Reference 10.

Fig. 5. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various write/erase cycles for two identical DEIS FET's from wafers DEIS II2 E and F, except that one of them (device F) had an annealing treatment in N₂ at 1000°C for 30 min prior to control gate poly-Si deposition. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The DEIS stack in these FET's consisted of deposited layers of 1000 Å of Si-rich SiO₂, 100 Å of SiO₂, and 1000 Å of Si-rich SiO₂ where the Si-rich SiO₂ layer had 46% atomic Si. The floating and control gates had areas of $1.1 \times 10^{-6}$ cm² and $6.8 \times 10^{-7}$ cm², respectively, and the gate oxide from the floating poly-Si layer to the Si substrate was 650 Å in thickness.