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CURRENT PATH IN AMORPHOUS-SILICON FIELD EFFECT TRANSISTORS

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Abstract.—On-resistance of amorphous-silicon field effect transistors with staggered electrodes was investigated. It was found that dependences of the on-resistance on geometrical parameters were classified into two groups. The origin was attributed to the residual resistance between the n⁺ electrode and the channel which was formed at the silicon-silicon dioxide interface. The resistance was analyzed by taking space charge effect into account, and we found that it changes in accordance with sample preparation conditions. It is pointed out that caution should be taken not only in transistor design but also in mobility evaluation and gap-state-density evaluation.

Introduction.—One of the important parameters of amorphous-silicon field effect transistors (a-SiFETs) (1) is the on-off current ratio. Recently, we obtained a high on-off current ratio (more than $10^8$) by using transistors with a staggered electrode structure (2). However, from a simple geometrical consideration, the maximum obtainable value was estimated to be $10^4$. In this paper, we would like to report that 1) this discrepancy arose from a drastic decrease of the residual resistance of the active n⁻ a-Si caused by the space charge effect, 2) this value changes by sample preparation conditions because it varies with localized state density, thickness and Fermi potential, and 3) the current path in the a-SiFETs changes from sample to sample according to the residual resistance.

Experimental Results.—Figure 1 shows a cross-sectional view of our FETs. The FET had $n^+ - n - n^-$ structure with staggered electrodes and was prepared on a crystal silicon substrate, with various $n^+$ electrode spacing $L$ and $n^-$ island length $L'$. The gate oxide thickness and channel width $W$ were fixed at 0.5μm and 200μm, respectively. The films were deposited by the hot cathode arc discharge decomposition method (3). Uniformity of the FET characteristics was excellent (on-current and off-current variations were less than 5%) but reproducibility was not good.

Figure 2 shows typical drain current $I_D$ vs. gate voltage $V_G$ characteristics. The maximum current was 130μA and the minimum current was about 1pA. Thus the on-off current ratio $\gamma$ is more than $10^8$.

Under low drain voltage $V_D$ and...
high $V_G$ conditions, a group of FETs on a substrate showed $I_D-V_D$ characteristics as shown in Fig. 3. The on-resistance

$$R_{on} = \frac{dV_D}{dI_D}$$

was not given by $L$ and was proportional to $L'$. Thus the current is considered to flow along the Si-SiO$_2$ interface from one edge of the n$^-$ island to the other edge of the n$^-$ island as shown by a solid line in Fig. 1. However, a group of FETs on another substrate showed $I_D-V_D$ characteristics as shown in Fig. 4. The on-resistance was proportional to $L$ and did not depend on $L'$. Thus it can be considered that the current first crosses the n$^-$ layer downwards, then flows along the Si-SiO$_2$ interface and again crosses the n$^-$ layer upwards, as shown by dotted lines in Fig. 1.

The different path that the current took was caused by the resistance $R$ between the n$^+$ electrode and the channel formed at the Si-SiO$_2$ interface. When $R$ is high, the FETs show the former characteristics because the voltage drop between the upper n$^+$ electrode and the lower channel is high. And when $R$ is low, the FET show the latter characteristics.

![Fig. 2. Typical semilogarithmic dependence of $I_D$ on $V_G$. $V_D$ was fixed at 40V.](image)

![Fig. 3. $I_D-V_D$ characteristics of the FETs with the current path shown by solid line in Fig. 1.](image)
Theoretical Results.- In case where the current flows along the dotted lines in Fig. 1 if we neglect channel resistance, $R_{on}$ equals to $2R$ and is given by

$$R_{on} = \frac{\rho_0 d}{W(L-L')}$$

where $\rho_0$ is the specific resistance of the n-layer, $d$ the thickness of the active n-layer. Since the off-resistance $R_{off}$ is expressed by

$$R_{off} = \frac{L}{\rho_0 Ld}$$

$\gamma$ becomes as

$$\gamma = \frac{R_{off}}{R_{on}} = \frac{(L-L')L}{4d^2}$$

Inserting typical values into $L, L'$ and $d$, $\gamma$ was calculated to be $10^4$, which is much less than the experimentally obtained value. This discrepancy can be explained by the fact that $R$ is a space charge limited resistance since a high resistive n-layer was sandwiched between the n+ electrode and the channel.

Figure 5 shows the calculated potential and carrier density distributions in the n+-n-n+ a-Si diodes. The localized state density distribution assumed is shown in Fig. 6. When the current flows, a large number of excess electrons appear in the n-layer, resulting in a drastic decrease of its resistance. However, distant from the n+ cathode, excess electron density decreases and resistivity approaches its equilibrium value. Thus the space charge limited resistance can be observed only in the case of extremely narrow n-layer and cannot be observed in conventional FE measurements. When the n-layer is 0.5$\mu$m and the current density is 1A/cm², which are
Fig. 5. Carrier and potential distributions in $n^+ - n^- - n^+$ a-Si diodes.

typical values in a-Si FETs, the voltage drop across the $n^-$ layer was calculated to be about 4V, which is 4 orders in magnitude less than the value calculated from specific resistance. Thus the high current ratio obtained experimentally can be explained by the decrease of $R$. Since $R$ changes with localized state density distribution and $n^-$ thickness and since it is comparable to the drain voltage of the a-Si FETs, the current path changes with sample preparation conditions.

It is important to express this space charge effect analytically. When we assume the localized state density near Fermi level to take the form $n_m \exp(E/kT)$ and when the thickness $d$ of the $n^-$ layer is much less than the characteristic thickness $d_0$ defined by

$$d_0 = \frac{\exp(J/qnT_o(a+kT))}{(qnT_o(a+kT))},$$

$R_{on}$ becomes

$$R_{on} = R_{ono} (a+kT) (d/d_0)^{a/(a+kT)}/(2a+kT),$$

where $J$ is the current density and $R_{ono}$ the resistance when the specific resistance is its equilibrium value.

Conclusion. - The importance of residual resistance in a-Si FETs was pointed out. Lack of reproducibility is partly caused by this resistance. And since the effective channel length changes with the resistance, careful examination of this resistance is necessary for evaluation of mobility and localized state density by FE method. To eliminate this resistance, coplanar electrode structure must be applied.

References.
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