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Automatic PCB Layout Optimization of a DC-DC Converter Through Genetic Algorithm Regarding EMC Constraints

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ABSTRACT This paper proposes an optimization approach for an automatic buck converter printed circuit board (PCB) design regarding the electromagnetic compatibility (EMC) constraints. The proposed solution is based on the combination of a genetic algorithm (GA) and a Dijkstra algorithm to generate the different PCB layout designs. Afterwards, a numerical modeling approach, taking into account all the stray elements, is proposed to obtain an accurate equivalent circuit for the PCB layout using ANSYS Q3D software. Subsequently, the complete behavior of the converter is simulated within SIMPLORER, including the electrical models of the components, the Line Impedance Stabilization Network (LISN) module as well as the PCB layout model. This aims to compute the conducted disturbances such as the common and the differential mode voltages. Then, this approach is implemented in an optimized process to reach the optimal geometry for the printed circuit board layout with the lowest parasitic effect to fit the EMC requirements. Finally, measurements are performed, and the optimization results are presented and investigated, in comparison with reference PCB layout to assess the efficiency of the proposed methodology.

INDEX TERMS Electromagnetic compatibility (EMC), PCB layout design, Dijkstra algorithm, genetic algorithm, automatic optimization.

I. INTRODUCTION

With the current evolution of electronics, the development of power electronics systems takes a very prominent place in various applications such as the automobile and aircraft applications. Power conversion devices are being developed rapidly to reach higher efficiency and power. However, with the requirements in terms of power density and reliability, many electronic devices have been developed for a higher switching frequency [1]. This increase in frequency involves an increase in the number of the electrical noise sources as well as the sensitivity of the electronic devices to electromagnetic (EM) noises. As shown in [2], the generated parasitic elements, such as stray inductances in power circuit, can cause voltage spikes and ringing due to the increased di/dt. This fact may have detrimental influences on switching losses and dynamic behaviours, and hence give rise to the electromagnetic emissions sources. Therefore, the interference problems have to be reduced in order to guarantee an appropriate operation of systems to achieve EMC.

Parasitic parameters that strongly affect the spectral signature of the converter are mainly derived from discrete components as well as copper traces of a direct-bonded-copper (DBC) [3], [4]. Thus, in order to minimize the impacts of these unintentional phenomena, many efforts were provided to act on the PCB layout designs [5]–[7]. Ning *et al.* [5] have proved that a good PCB layout is the most powerful key to obtain a significant reduction of a large number of disturbances problems. Besides, an improperly designed PCB layout can lead to electromagnetic interferences that may degrade the electronic device operation. Hence, the PCB layout designs for optimized power electronic circuits with low parasitic parameters have attracted more and more interest from the designers in both industrial and academic environments. In industry, most of the EMC experts use some rules of thumb, based on personal experience to design

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PCB layouts. Manual PCB layout designs process is, usually, based on iterations. Each cycle generates a PCB layout design which is compared to other design results and eventually the best layout is selected among the different candidates. Generally, the best candidate is not the best choice for the entire design space. However, the main dissatisfaction with this manual design is basically related to the design speed and the limited choice of tested solutions, which are time and money consuming [8]. Several guidelines and manual investigations have been also proposed in the literature [9]–[11] to perform the layout in order to reduce EM interferences, such as drawing large tracks to reduce stray inductances or thoughtful positioning of components to avoid large loops which generate magnetic interferences. Unfortunately, these techniques generally bring improvements and carry out a compromise at the level of EM couplings without ensuring that the adopted solutions are optimum compared to EMC constraints. Moreover, common solutions cannot be generalized and they are not suitable for all possible structures. For instance, the use of broad tracks decreases stray inductances, but it increases the parasitic capacitances [12].

Recently, automatic layout optimization tools have become a necessity to achieve designs which fulfil EMI requirements. Many efforts have been made to achieve automatic layout design regarding EMC constraints [13]–[15]. For example, Oliveira *et al*. [13] proposed an automatic PCB layout design of an EMC filter to reduce EM disturbances. Mandray *et al*. [14] presented thermal and simple EMC models to realize an automatic layout design of a double-sided power module without considering time and accuracy. These models include thermal effects and parasitic capacitors while inductance has been ignored. Work described in [15] used a GA for layout optimization of a simple power module to minimize parasitic elements. However, with this method, the computational population increased significantly due to all possible designs being considered. Many others optimization procedures have been presented in the literature, which focus on optimizing the layout, such as in [16], [17]–[19]. Nevertheless, the purpose of such references works mainly deals with the EMC filter layout optimization. Further, to ensure that the final product meets the requirement of the EMC standard, the appropriate techniques for eliminating EMI problems must be implemented at the converter level, instead of the final corrections, such as the filter optimization. Besides, some filters are not sufficient to ensure the conformity of the final product, because many studies in the filter optimization are often giving final solutions whose components are not always found at suppliers which in practice are not feasible, while others are too bulky and expensive [18]. Furthermore, all the stray EM effects cannot be solved only by using filters because when the stray elements of the layout are not optimized, the filtering efficiency can be dramatically reduced. Actually, the optimization tools currently used in commercial EM solvers fixed the starting from a predefined structure selected by the designer as a reference [19]. Therefore, this paper proposes to go further than the optimization of an EMC filter and the enhancement of the PCB layout. Our aim is to develop an automatic optimization process for a dc-dc converter PCB layout in order to reach the best solution respecting a reduced EMC signature. Thus, a main contribution of this paper is optimizing the converter before moving to the filtering solution which will reduce the cost and the volume of the filter. A buck converter is taken as an example for this optimization, but the stated method can be also suitable for other circuits as well, and can be generalized to any configuration. Associated with the optimization loop, a methodology is proposed to randomly design the PCB layouts. The PCB layouts modelling were achieved utilizing ANSYS Q3D software which is proposed to compute the parameters of the interconnection. The design optimization in question was processed using an evolutionary optimization algorithm. To reach this aim, a genetic algorithm has been adopted for the minimization of the fitness function. Finally, based on an objective function computation, the optimization process selects the layout corresponding to the optimal solution.

The remainder of this paper is organized as follows: The studied converter and the models of the different components are provided in section 2. Section 3 depicts our optimization methodology. This section will detail the proposed different steps of the optimization strategy. The results of the optimization process are presented and discussed in Section 4. This section presents the experimental measurements, which validate the proposed approach. Finally, section 5 gives the general conclusions of this work.

II. MODELLING THE REAL BEHAVIOUR OF DC-DC CONVERTER

As widely reported in various publications targeting the design of converters [20], [21], parasitic elements can have a significant impact on the dynamic performance of these devices. An accurate prediction of spurious elements is therefore very important to analyze the EM disturbances. In order to take these effects into account in the proposed design procedure, a modelling approach of the DC-DC converter, taking into account the parasitic elements of the non-ideal components and the parasitic elements of the routing, was tackled. The adopted models are here briefly discussed.

A. STUDIED CONVERTER

The studied converter is a series chopper (see Figure 1). The proposed model includes a source through, a Line Impedance Stabilization Network (LISN), two decoupling capacitors, a Si MOS transistor IRFP460 (500V / 20A), a Si Schottky diode SC250KG (1200V / 5A), and an R-L load. The DC bus voltage is fixed at 100V (VDC = 100 V) for a nominal load current of 1 A. The switching frequency is 50 kHz with a duty cycle of 50%.

B. DECOUPLING CAPACITOR

In the studied converter, two decoupling capacitors (a polyester capacitor C1 and a ceramic capacitor C2) are

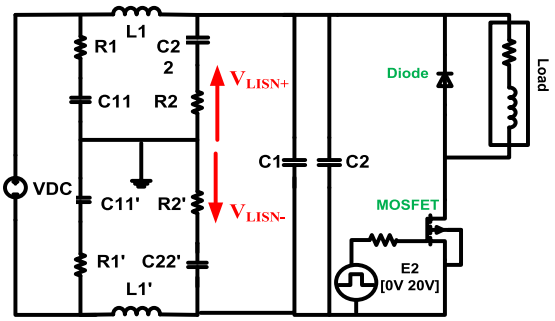


FIGURE 1. Studied structure.

used. The behaviour of capacitors is modelled with a conventional RLC equivalent circuit. The impedance measurements for both capacitors have been characterized with an HP4194A impedance bridge in [22]. This equivalent model of the capacitor is represented in Figure 2.

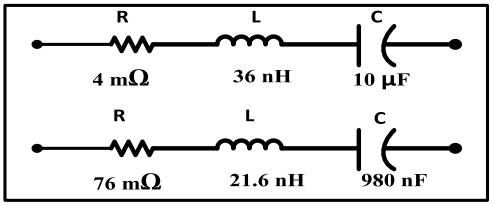


FIGURE 2. Decoupling capacitor circuit.

C. ACTIVE COMPONENTS

The SPICE level 3 model is chosen for MOSFET, which is appropriate for power electronic applications due to the large availability of SPICE simulators. This model allows considering the static characteristics and the dynamic effects such as the variations of the C_{GD} and C_{DS} capacities [23]. In order to model the Schottky diode SC250KG, we used the model provided in the SIMPLORER software library.

D. LISN

In order to measure the conducted disturbances, a LISN must be included in the considered circuit. The LISN is like a filter inserted between the device under test and the network. Its role is to isolate the network on which it can occur the common and the differential mode disturbances of the equipment under test. The single-phase model of the LISN used in the laboratory is a "50A: Prana Tegam- 50Ω - 50μH", for EN55022 standard (cf. Figure 3). Table 1 gives the equivalent values identified for the LISN. The equivalent electric model of the used LISN is proposed and validated in [24].

The total conducted EMI noise consists of two components: common-mode (CM) noise and differential-mode (DM) noise [2]. In order to quantify these two components, one can say that CM noise propagates between each conductor with respect to ground through parasitic components, while DM noise propagates between conductors. The Common mode and the differential mode voltages, noted

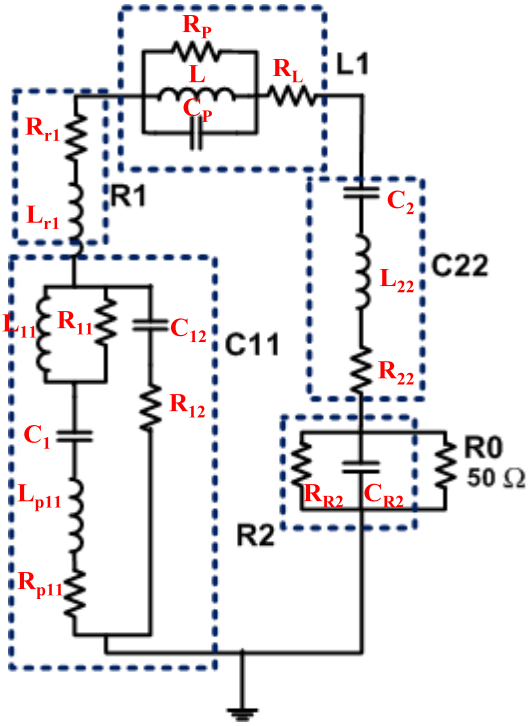


FIGURE 3. LISN equivalent circuit.

TABLE 1. Values of LISN equivalent circuit.

L1	R_L =1.3 kΩ
	R_p= 20 mΩ
	L= 44.6 µH
	C_p= 11.9 pF
C22	C_2 = 209 nF
	L_{22}= 4 nH
	R_{22}= 3 mΩ
R1	R_{r1}= 3 Ω
	L_{r1}= 0.54 µH
C11	C_{11}= 1.7 nF
	R_{12}= 331 Ω
	L_{11}= 32 nH
	R_{11}= 0.3 Ω
	C_1= 10 µH
	L_{p11}= 22 nH
	R_{p11}= 40 mΩ
R2	R_{R2}= 1 kΩ
	C_{R2}= 1 pF

respectively (VCM) and (VDM), are computed using the equations (1) and (2). The calculations are made in the resistances R2 and R2' of the LISN as illustrated in Figure 8.

$$VCM = \frac{v^{+}_{LISN} + v^{-}_{LISN}}{2} \tag{1}$$

$$VDM = V^{+}_{LISN} - V^{-}_{LISN} \tag{2}$$

E. LOAD

The load of the chopper is an RL load, equivalent to a 40 Ω resistor and an inductance of 2.5 mH. Three measurements were performed to build the model. This load model is represented by three impedances (Z1, Z2, and Z3) (cf. Figure 4). The impedance measured between the two terminals of the load and the ground plane is represented by two capacitors. From the results obtained in Figure 6, the parasitic elements of the load can be extracted by equation systems (3) and (4) [24]:

$$\begin{aligned} A &= Z3//Z1 \\ B &= Z2//Z3 \\ C &= Z1//Z2 \end{aligned} \tag{3}$$

$$\begin{cases} Z1 = \dfrac{2(A*B*C)}{A*B+C*B-A*C} \\ Z2 = \dfrac{2(A*B*C)}{A*B-B*C+C*A} \\ Z3 = \dfrac{2(A*B*C)}{-A*B+A*C+C*B} \end{cases} \tag{4}$$

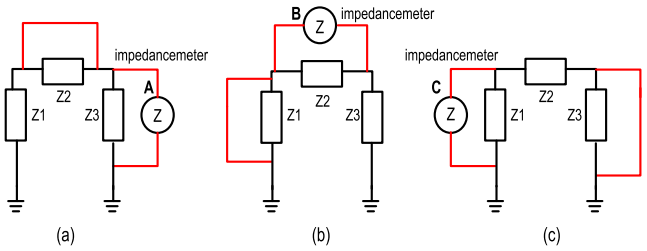


FIGURE 4. Load measurement configuration.

The electric model used (cf. Figure 5) has been compared and validated with experimental measurements performed with impedance meter for a frequency range of 100 Hz to 30 MHz (see Figure 7).

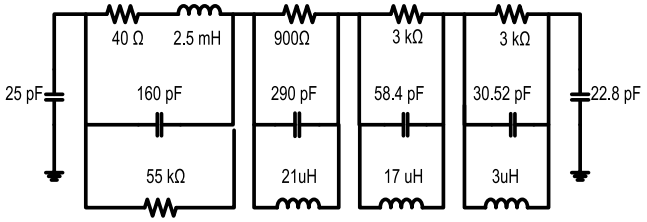


FIGURE 5. Load equivalent circuit.

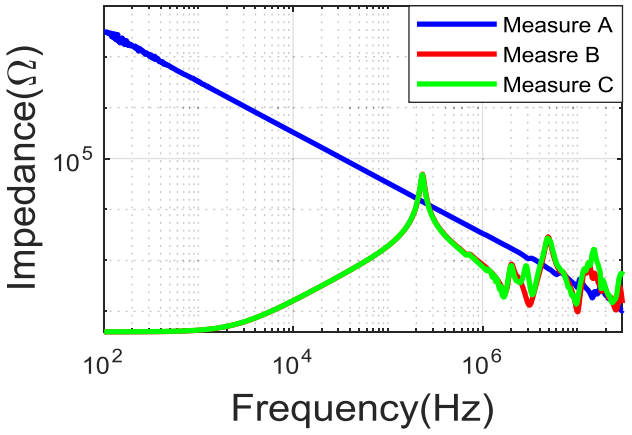


FIGURE 6. Load measurement results.

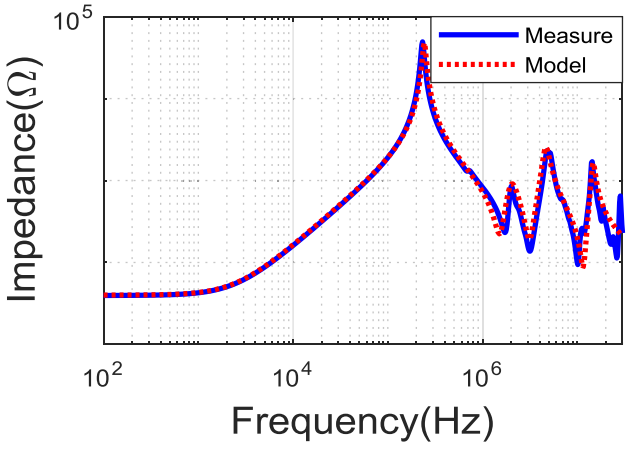


FIGURE 7. Measured and simulated impedance module of the load.

F. PCB LAYOUT MODELING AND ELECTRICAL SIMULATION

In this paper, a numerical modeling approach is used to accomplish the task of PCB layout modeling. The PCB layout is modeled using ANSYS Q3D extractor software. This software uses the method of moments (MoM) with integral formulation and the finite element method (FEM) to compute all the stray elements of the PCB layout such as resistance, inductance, and capacitance conductance (RLCG) matrices. This tool is used to perform both DC and AC analysis. In this work, the results of the AC analysis are taken into account since the values of the resistances are highly sensitive to the effects of skin and proximity, which vary with the frequency. Indeed, the skin effect is manifested primarily at high frequencies. This phenomenon exists for conductors which are crossed by alternating currents. With the rise of frequency, it will disrupt the distribution of the current which will be concentrated towards the outer surface of the conductor. The changing in the current distribution causes an increase in the resistance of the conductor and an asymptotic drop in the total inductance to static value called external inductance. To conclude, the resistance and internal inductance of PCB traces

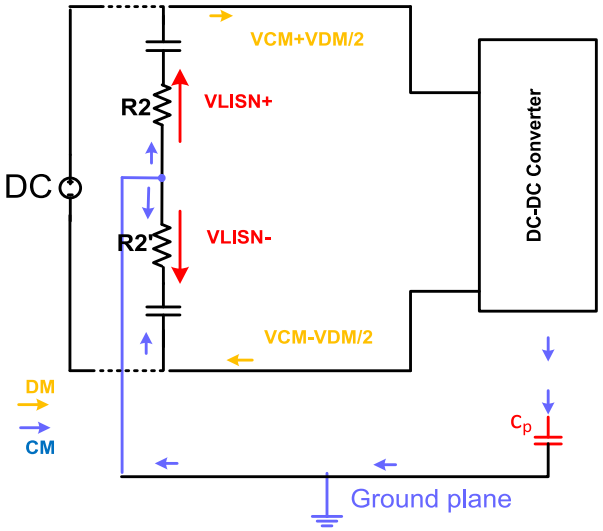


FIGURE 8. CM and DM propagation paths between a source and DC-DC converter.

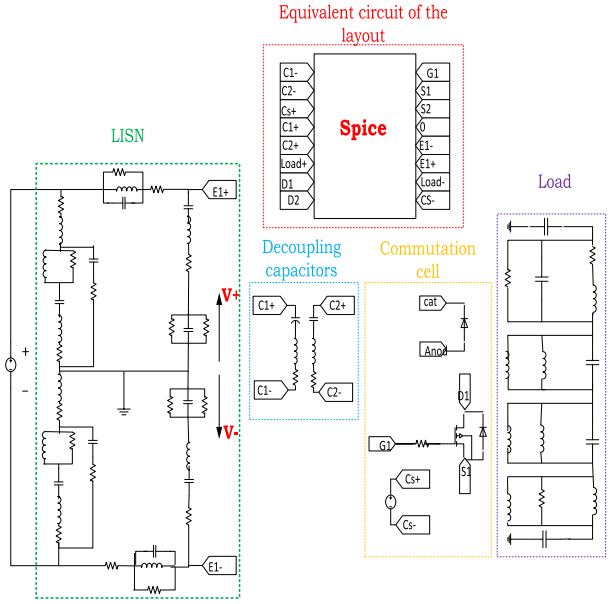


FIGURE 9. Chopper model with its imperfections under SIMPLORER.

rely on the current distribution in the conductor and vary according to the frequency [25]. Therefore, it is necessary to take into account the skin effect, as it modifies the value of resistance as a function of the frequency.

The chopper's circuit has a single layer, with 35 μm thick tracks, placed on a 1.6 mm thick FR4 epoxy substrate. Once the routing has been imported into Q3D extractor, the next step is to assign the materials (copper) on each track. The ground plane is modeled like a copper sheet located under the PCB circuit. To extract the parasitic elements, different nets are assigned in the circuit. In our case, we defined five nets, bus+, bus-, switching cell, signal control, and GND. After assigning the desired nets, we place automatically the different components pins on the PCB layout. Pins are then excited by the source and sink terminals in order to set up the simulation solution. A frequency sweep is performed between 10 kHz to 30 MHz. Finally, an equivalent circuit has been exported to the SIMPLORER software which allow the electrical behavior evaluation of the circuit under test (see Figure 9). The simulation parameters of the electrical circuit are given in table 2.

TABLE 2. Simulation parameters.

DC-bus voltage	100 V
Load inductance	2.5 mH
Load resistance	40 Ω
Switching frequency	20 kHz
Duty cycle	50%
Load current	1 A

III. OPTIMIZATION PROCESS

The purpose of this section is to set out the optimization process that is carried out on a chopper circuit. The optimization of the electromagnetic behavior of this converter was performed by varying its routing. Before running the optimization procedure, the algorithm begins by building the graph, which ensure the discretization of the circuit area where the different conductive tracks are defined. Afterwards, all the components are placed in the grid layout by following the electrical rules. We have fixed the location of the discrete components of each PCB layout solution. Thus, the aim is to, only, modify the PCB tracks geometries in order to just make an optimization on the PCB traces. Once the locations of the components are fixed, the optimization process will take place. The whole optimization process includes three steps. In the first step, an automatic routing algorithm has been applied, which is based on Dijkstra algorithm and governed by a GA. This latter is developed to execute the routing of the interconnected tracks. For the first generation, this algorithm allows to randomly generate several PCB layouts candidates by connecting the position of the components with copper trace. These candidates are grouped together as initial solutions within the same family. In the second step, after obtaining the PCB layout, it will be modeled through ANSYS Q3D. The coupling between MATLAB software and Q3D extractor software is established automatically thanks to DXF file. Subsequently, the PCB layouts are modeled to characterize the parasitic elements. All these elements, such as resistive, inductive and capacitive effects, are taken into account to obtain an accurate equivalent circuit of the layout. An equivalent model is then generated for each layout, which will be implemented in the SIMPLORER time-domain simulator. The complete circuit including active and passive components models and PCB layouts models are analyzed in SIMPLORER to simulate the complete circuit behavior performance. Following that, the output is automatically used in an optimization process to evaluate the cost function,

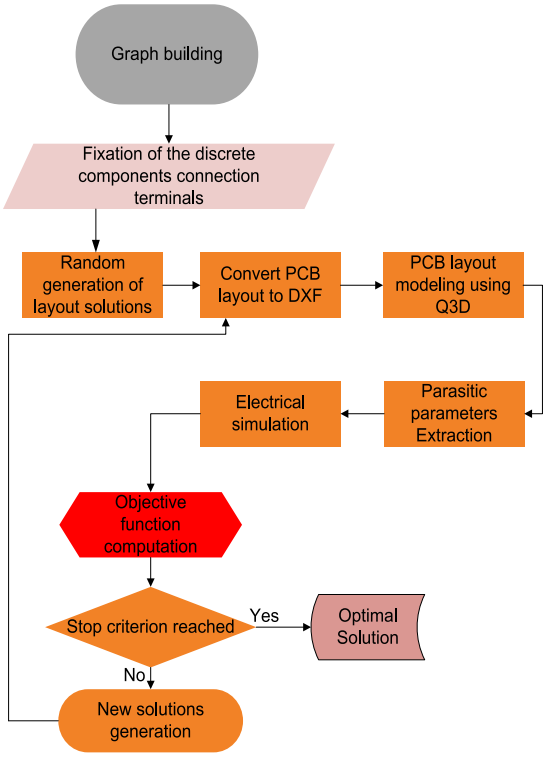


FIGURE 10. Optimization flowchart.

allowing obtains of the optimal solution for the PCB layout, in order to acquire the best possible converter behavior for EMC.

Finally, a fast fourrier transform (FFT) is performed to obtain the EMI spectrum and then an objective function is computed for each solution. The process of finding an optimized layout solution relies on modifying the existing routing solution, which is already tested until having the best one in an EMC perspective. Indeed, this research is performed using GA to minimize the objective function in a given frequency band (cf. paragraph III.B.3). Therefore, from these last solutions, a new generation is created with crossover and mutation operation. These newly established solutions are in turn analyzed in order to converge towards an optimal one. The algorithm execution is repeated until satisfying the objective function, or when a maximum number of generations are reached. Once the optimization process is complete, it will provide the best circuit topology among the explored solutions, the associated cost function and estimated performance indicators (VCM and VDM voltages). A flowchart of the proposed optimization procedure is shown in Figure 10. The following sections describe the details of the inputs requirements and the main steps of the optimization process.

A. GRAPH BUILDING AND FIXATION OF THE DISCRETE COMPONENTS TERMINALS

Step 0 - creation of a weighting grid: the first step aims to create a graph which represents the discretization surface.

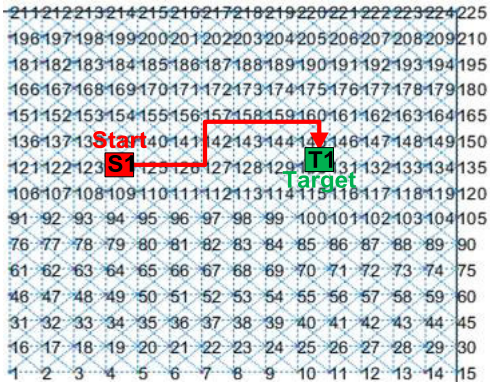


FIGURE 11. The PCB layout grid.

The graph is represented by an M × M matrix (M = number of nodes). The graph is composed of a set of nodes connected to each other by weighted edges (see Figure 11). These edges are defined by weight values $\boldsymbol{P_{ij}} = \boldsymbol{G}(\boldsymbol{i},\boldsymbol{j}) = \boldsymbol{G_{ij}}$ called costs, which are randomly initialized by the Dijkstra algorithm. This space refers to the 2D area, where the paths are defined. The vertices represent the positions of the components and the edges correspond to the different possible paths to connect from one node to another. We have chosen to define the distance between two vertices of the same line or column at 1mm. The diagonal distance between two vertices is set to $\sqrt{2}$ mm. The matrix G is defined as follows:

$$G = \begin{pmatrix} G_{11} & \cdots & G_{1M} \\ \vdots & \ddots & \vdots \\ G_{M1} & \cdots & G_{MM} \end{pmatrix} \tag{5}$$

$$G = \begin{pmatrix} P_{11} & P_{12} & \infty & \ldots & G_{1M} \\ P_{21} & P_{22} & P_{23} & \ldots & G_{2M} \\ \infty & P_{32} & P_{33} & \ldots & G_{3M} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ G_{M1} & G_{M2} & G_{M3} & \ldots & G_{MM} \end{pmatrix} \tag{6}$$

It is worth nothing that:

- $G_{ij} = P_{ij}$, when there is a direct route between nodes i and j
- $G_{ij} = \infty$, when the nodes i and j are disconnected

As an example, between nodes 1 and 2 there is a direct link, $G_{11} = P_{11}$ while there is no connection between node 3 and node 1 so $G_{13} = \infty$.

Some requirements were taken into account when designing the DC-DC converter. Before performing the optimization procedure, the following parameters are configured:

- The maximum circuit size **Xmax** and **Ymax**, which are considered as maximum boundaries during the design of the final PCB layout.
- The step **N** between nodes
- The number of nodes **M**
- The vectors **S**= {Si; i = 1…L}, and **T**= {Tj, j = 1…N}, which represent the positions of the components

and contain the staring nodes and the targeting nodes, respectively.

B. OPTIMIZATION STRATEGY

We propose to use GA-based optimization strategy to design the DC-DC converter. GAs are global heuristic search algorithms based on natural genetics. This search technique is basically established on the evolutionary principle of Darwin's natural selection in order to find a solution to a given search optimization problem. A GA starts with a set of initial solutions that are replicated to create a new generation of solutions. By repeating this cycle, we obtain a population composed of better solutions. During the genetic process, the solutions are evaluated using specific techniques, such as fitness and selection, and genetic operators such as crossover and mutation. As a result, GAs may be more effective in achieving the global minimum (even if there is no guarantee that the global minimum will be obtained in a limited time), while those based on the gradient are more likely to be trapped in a local optimum. GAs work well in design optimization techniques with excellent results [5], [17]. The main advantages of GA include the robustness at initialization and their convergences do not depend on the initial value. Moreover, GA can be easily parallelized because each solution of a generation is computed independently from the other solutions of the same generation.

1) REDUCTION OF THE VARIABLES

Usually, graph theory algorithms modify the path between two nodes based on edges information. Therefore, we randomly assigned the weight $\boldsymbol{P_{ij}}$ of each arc. Consequently, the matrix G is modifiable at each iteration to generate a different routing solution. If we analyze this step, for M = 225 nodes, we have 1849 variables in matrix G. The complexity of the problem implies that it is not possible to solve our problem and to govern these variables by the GA in global optimization toolbox algorithm. Indeed, asking a GA to govern a large number of variables doesn't work. These variables being very numerous, the optimization is found to be hampered and within the impossibility to effectively look for new solutions which might tend towards the respect of the EMC constraints. It was therefore necessary to find a cleverer formulation in order to overcome this problem. We have proposed to fix the matrix G. Therefore, from a matrix G of size (225 x 225), we end up with another matrix R with the same size (225 x 225). Indeed, we have chosen to multiply the first 15 rows of the matrix G by a random vector Xi {i = 1…15} with Xi= randi ([1, 10]) and continuing in the same way until the last row of matrix G. In such a manner, at each iteration we have only 15 variables instead of 1849 in the case where M = 225. We were able to reduce the number of variables to generate different paths. This reduction will facilitate the formulation of our problem by the genetic optimization algorithm. Finally, the most considerable advantage of this reduction is the possibility of controlling the routing process by the GA coupled with the Dijkstra algorithm. Thus, the parameters of the optimization are the Xi vectors while the objective to be minimized is related to the disturbance spectra.

2) PCB LAYOUT DESIGN PROCEDURE BASED ON DIJKSTRA ALGORITHM AND GOVERNED BY GA TOOLBOX

The purpose of the PCB routing generation procedure proposed in this paper is to generate several solutions as a first panel of solutions. These solutions will be evaluated and optimized in a second step.

Several algorithms have been used to draw a path from point A to point B. In the literature, many algorithms have been developed, such as Lee's algorithm. The main objective of these algorithms is to find the shortest path connecting two distant points, which is not necessarily the best one in terms of EMC point of view. Moreover, they rely on geometric criteria to determine the shortest path. However, there are other algorithms based on graph theory. The path search problem is a classic problem of research in graph theory. This later is a widely useful approach for dealing with path searching in the fields of a computer network, communication, and transport. Numerous graph search algorithms have been used [26], [27] for finding a path between nodes such as the Floyd algorithm, the Dijkstra algorithm, the A∗algorithm and the D∗ [28], [29]. Compared to the existing algorithms, these algorithms allow the search for the shortest path between two objects whose advantage is to consider any physical aspect to define a routing solution and not only geometric criterion. In this paper, the Dijkstra algorithm was adopted since it is one of the best algorithms for computing the shortest path in a graph where the weights are positive. The Dijkstra algorithm is also a simple and efficient deterministic algorithm for shortest paths (SP) problems. Dijkstra's algorithm in its original version searches for all the optimal paths between a starting node and all the other nodes of the graph. However, the main objective is enable the generation of several different paths from the starting point to the target point depending on the obstacles in the grid. For this reason, we have made improvements to the classical Dijkstra algorithm. We stopped Dijkstra's algorithm as soon as it finds the desired end node, as a first improvement. Hence, the first modification concerns the stop condition. With the second modification, the Dijkstra algorithm gives several paths between two nodes. This modification allows the algorithm to look for the shortest path between two nodes instead of the shortest paths between a node and all other nodes in the graph. The third modification is the addition of electrical constraints to obtain a conformal connection circuit. The principle of this algorithm is the repetition of Dijkstra's algorithm several times, with a test of path change between iterations. These three improvements lead us to modify the Dijkstra algorithm in order to achieve our goals. The modified Dijkstra algorithm gives us a set of several paths for a given initial node to a goal node. For example, for $N = 49$ nodes, we have $n = 361$ variables. In the figure (cf. Figure 12), we notice that each time a different path between two points is obtained.

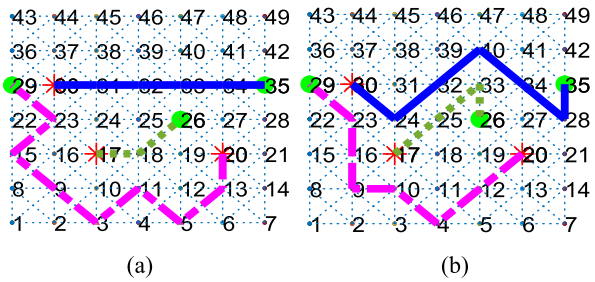


FIGURE 12. First possible solution (a), second possible solution (b).

- Unvisited nodes
- Destination nodes
- Starting points

Path 1
Path 2
Path 3

Path 1 = **30** 31 32 33 34 **35**
Path 2 = **29** 23 15 9 3 11 5 13 **20**
Path 3 = **17** 18 **26**

Path 1 = **30** 24 32 40 34 28 **35**
Path 2 = **29** 23 16 9 10 4 12 **20**
Path 3 = **17** 25 33 **26**

a: DESCRIPTION OF THE REQUIREMENTS IN THE ROUTING STRATEGY

The PCB layout grid is a real representation of the studied converter. Therefore, it is essential to build the graph by following the packaging components limits and rules. The requirement for the routing algorithm is to, randomly, generate PCB layouts avoiding crossings between tracks. It is necessary to check the proper connection circuit in order to guarantee the absence of short circuits and the unwanted crossing between the normally isolated tracks.

A function has been developed within the Dijkstra algorithm which allows for each run to test the realized connection circuit. The definition of the constraints must be generically established so that any connection circuit can be analyzed. Consequently, we will be able to perfectly control the geometry of the layout throughout the optimization process. In our case, there are two types of crossing: crossing between diagonal arcs and crossing between nodes. Firstly, to avoid the crossing between the diagonal edges (cf. Figure 13), the algorithm allows verifying that the edge connecting the two selected nodes is valid. It means, to establish a path between two nodes, the Dijkstra algorithm starts from a node called ''father'' and then analyzes the validity of its neighbors also called ''child nodes''. Once the child has been chosen, the dijkstra algorithm will verify if the edge connecting it to the parent node is valid. The purpose is to ensure that using this arc does not lead to the crossing of another edge previously established. If this is the case, then it is imperative to prohibit the use of this arc. At this point, the Dijkstra algorithm will prevent the use of this current node and will check the other parent neighbors until finding another valid one. Secondly, to avoid the intersection in one node (cf. Figure 14), all the points that constitute an already established path have been inserted in a closed list. It means that in each iteration, the saved list points are excluded from the search and cannot be included again in the other paths.

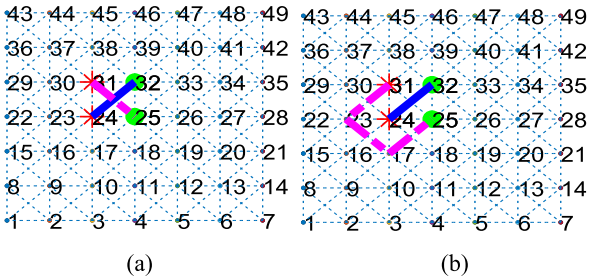


FIGURE 13. Example of crossing diagonal edges (a), possible solution after adding the function to avoid the diagonal crossing (b).

Path 1 = **31** **25**
Path 2 = **24** **32**

Path 1 = **31** 23 17 **25**
Path 2 = **24** **32**

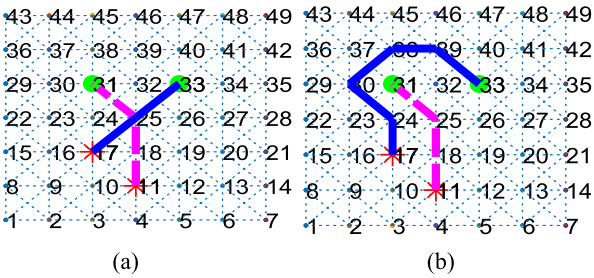


FIGURE 14. Example of crossing in one node (a), possible solution after adding the function to avoid the intersection in the nodes (b).

Path 1 = **11** 18 **25** **31**
Path 2 = **17** **25** **33**

Path 1 = **11** 18 25 **31**
Path 2 = **17** 24 30 38 39 **33**

b: EXAMPLES OF AUTOMATIC GENERATION OF THE PCB LAYOUT

The conductive tracks are built on the discretization grid and have the role of ensuring connections between the various discrete components. The paths obtained under MATLAB are used to build the tracks. For example, from a path between two nodes A and B with A (X_A, Y_A) and B (X_B, Y_B), we built a rectangle representing the conductive track (see Figure 15). It was therefore necessary to determine the coordinates of the points F = (X_F, Y_F) and C = (X_C, Y_C).

We will start by computing the angle θ which is given as:

$$\theta = \tan^{-1}\left(\frac{DX}{DY}\right) \tag{7}$$

Since the width of the track l and X_A are known, the relation between points A and C are described by the following two relations:

$$\cos\left(\frac{\pi}{2} - \theta\right) = \frac{X_C - X_A}{l/2} \tag{8}$$

$$\sin\left(\frac{\pi}{2} - \theta\right) = \frac{Y_A - Y_C}{l/2} \tag{9}$$

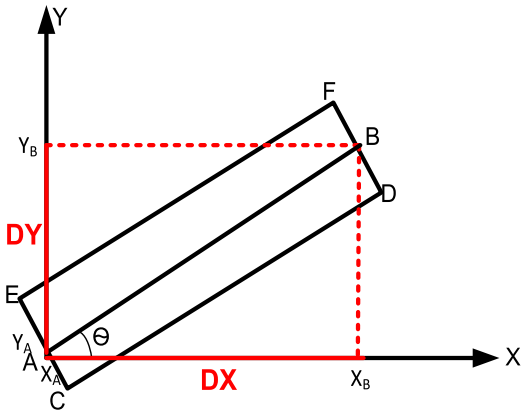


FIGURE 15. Illustrative construction of a PCB.

Thus, we get such that:

$$X_C = l/2 \cos\left(\frac{\pi}{2} - \theta\right) + X_A \tag{10}$$

$$Y_C = -l/2 \sin\left(\frac{\pi}{2} - \theta\right) + Y_A \tag{11}$$

Likewise, we can determine the coordinates of point F, so we have:

$$X_F = -l/2 \cos\left(\frac{\pi}{2} - \theta\right) + X_B \tag{12}$$

$$Y_F = l/2 \sin\left(\frac{\pi}{2} - \theta\right) + X_B \tag{13}$$

The degrees of freedom in the path generation procedure are based mainly on:

1) PCB trace width, designed according to input rated voltage, current and over-heating [30], [31]. However, the distance between the components is fixed. The optimization process that we have developed does not allow defining a track width larger than the value of the discretization step N=1cm of the grid. We have chosen to vary the width fully randomly between 2 mm to 6 mm, which is greater than the minimum width (0.3 mm). This is to make sure that no overlap can occur between two parallel tracks to ensure sufficient insulation between them. When using high currents, we can increase the discretization step of the grid and we can exceed the maximum fixed width of 6 mm and we compute the range of the appropriate width according to the applied current.

2) The distance between the parallel PCB traces is at least equal to the width of the tracks.

3) All angles between the paths are allowed.

These several rules must be followed by the optimization algorithm. Two examples of solutions generated by the routing algorithm are presented below.

3) THE OBJECTIVE FUNCTION

The main objective of this study is to find the best PCB layout solution, allowing the best behavior with respect to EMC aspects related to conducted emissions. The proposed objective function minimizes the spectra of disturbances conducted over a selected frequency range. In fact, the circuit generates conducted disturbances that can be recovered at the LISN. The proposed objective function is the sum of the differences between the spectrum amplitude of the routing disturbances of the current iteration which are denoted y(i) and the threshold y_0 according to the EMC standard EN 55022 (y_0), unless the spectral lines y(i) are greater than y_0, as defined in equation (14). Therefore, the objective function calculates the amplitude of the spectrum that exceeds the limit accepted by the EMC standard. The limits of the frequency range (f_0 and f_t) must be determined precisely. Since the spectrum is defined over a wide frequency band that varies between 100 kHz and 30 MHz, it is difficult to minimize the spectrum amplitude over the entire spectrum with a single optimization. Moreover, it has been shown in [22] that the PCB layout has a significant influence on the voltage in CM and DM in the high frequencies. Given that, the influence of PCB layout is negligible at low frequency (LF), it is not necessary to set a low limit (f_0) too low and it is not essential to choose a maximum frequency (f_t) either too important because our analytical model is valid up to 30MHz. We have chosen to calculate the objective function over a frequency range (f_0, f_t) from 5 MHz to 30 MHz. The quality of the optimum obtained therefore depends on the considered frequency band.

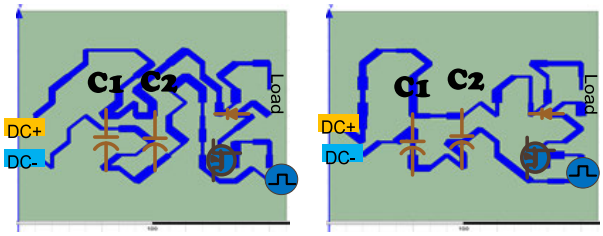


FIGURE 16. Examples of PCB layouts.

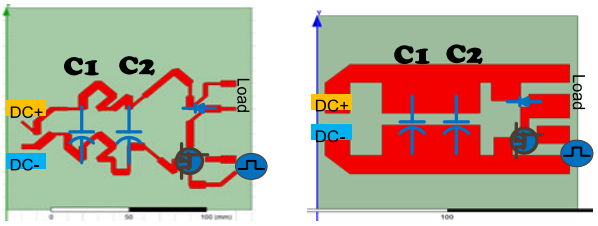
The goal of the optimization is to minimize this objective function and therefore minimize the amplitudes of the disturbance spectrum.

$$\text{Fobj} = \sum_{i=f_0}^{f_t} (\text{y\_CM (i)} - y_0(i)) + \sum_{i=f_0}^{f_t} (\text{y\_DM (i)} - y_0(i)) \tag{14}$$

IV. OPTIMIZATION RESULTS AND DISCUSSION

In this optimization, we fix the location of the components and we try to improve the performance of the converter by adjusting the routing. Therefore, the optimization parameters of PCB layout are gathered in the vector Xi where the number of variable is 15.

The maximum size of the circuit has been set at 16 cm × 16 cm. The optimization process was launched to obtain the lowest conducted disturbances for emissions in CM and DM modes. In fact, the optimization process tested



(a) (b)

FIGURE 17. Optimized PCB layout (a), Standard PCB layout (b).

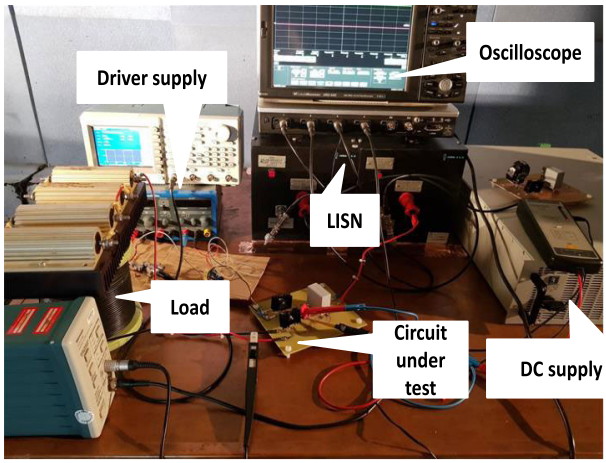


FIGURE 18. The Experimental test of the DC-DC converter.

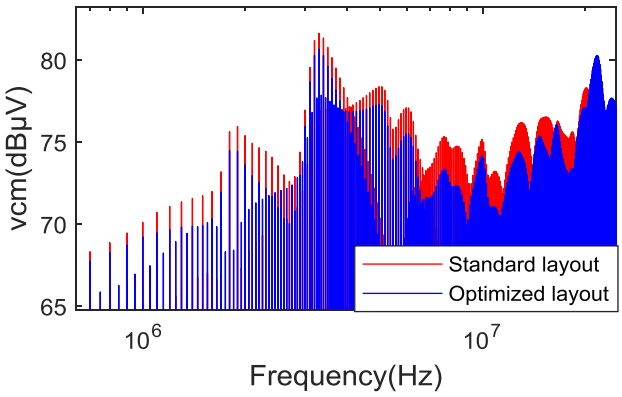


FIGURE 19. Comparison of measured CM perturbations.

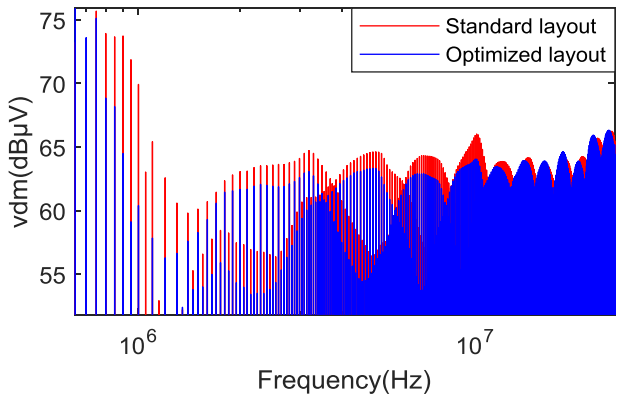


FIGURE 20. Comparison of measured DM perturbations.

1500 different PCB layout solutions to obtain the optimized solution presented in Figure 17 (a). The results of the optimization were obtained with the following set of parameters: size of the initial population in the loop P = 50, stopping criterion A = 30 iterations. The standard topology that was designed manually is shown in the Figure 17 (b). These solutions have been evaluated using both two-mode analysis (CM and DM) and impedance analysis.

A. EXPERIMENTAL VALIDATION

An experimental comparison was made to validate the optimization process. Measurements are performed with an oscilloscope (LeCroy HRO 66Zi), on resistors R2 and R2' in the line impedance stabilization network (LISN) (cf. Figure 18). The PCB layout of the optimized process and the other layouts have been built and tested in order to be able to compare the optimization results with standard solutions. In fact, we choose to fabricate a classic solution with straight and slightly wide tracks as a reference solution. Then, the common mode voltages for the manual test case (red spectrum for the reference topology) as well as the common mode voltage of the solution obtained by the optimization process (blue spectrum) are displayed together in Figure 19. Figure 20 displays the comparison between waveform of the differential mode voltage (red spectrum for reference PCB layout as well as blue spectrum for the optimized solution).

The results show that optimized PCB leads to better CM and DM behaviors compared to a standard PCB layout. On the one hand, a 3 dB improvement for VCM spectrum between the best solution and the reference is noticed from a frequency of 5 MHz. On the other hand, the EMI obtained reduction is of 4dB for VMD spectrum especially from 800 KHz.

B. IMPEDANCE MEASUREMENTS

To validate the optimization results, impedance measurements were taken while the converter is not operating. Impedances were measured using an Agilent 4294A precision impedance analyzer, which has a frequency range of 40 Hz to 110 MHz. The sweep source was set as a magnitude equal to 0.1 V and a frequency of 100 Hz to 30 MHz. After calibrating the impedance analyzer and the probe, a set of measurement configurations was tested under various conditions. The active components of the circuit were replaced by short circuits or open circuits.

1) CONFIGURATION 1: ZMC MEASURMENTS

The experimental setup for the measurement is shown in Figure 21. In this Figure, the impedance analyzer is placed between the terminal of the output to the circuit under test

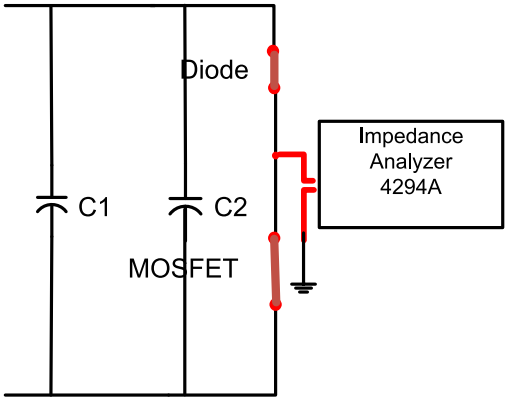


FIGURE 21. Setup ZCM measurement.

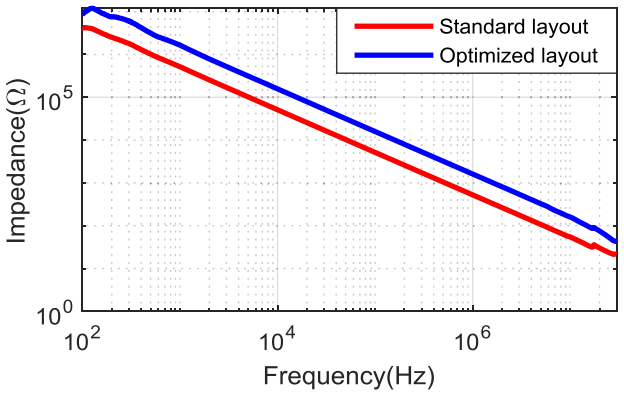


FIGURE 22. Comparison of measured CM impedance.

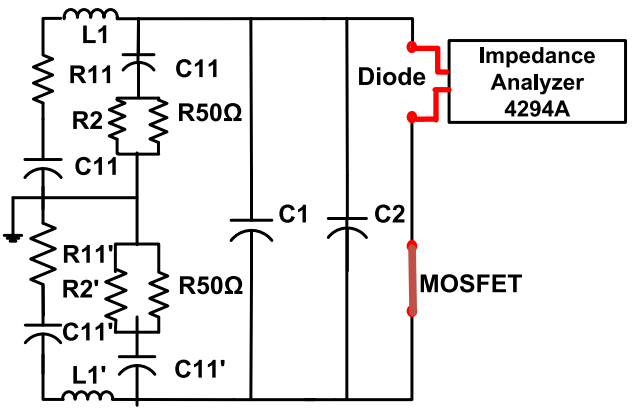


FIGURE 23. Setup ZDM measurement.

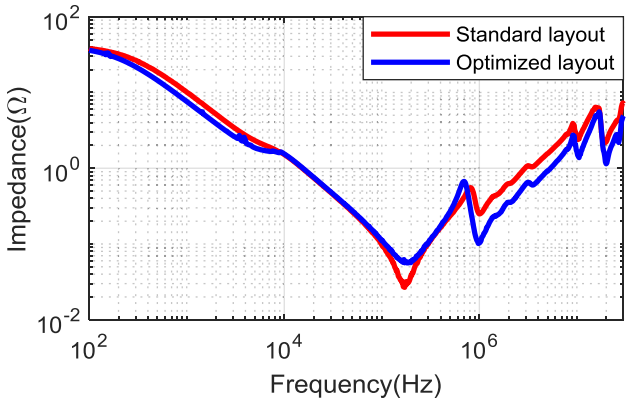


FIGURE 24. Comparison of measured DM impedance.

and ground. This setup involves measuring the equivalent common mode impedance "seen" from the output point with the active components replaced by shorts circuits and disconnecting the LISN and the load at the same time. The CM depends, essentially, on the coupling capacitances Cp (Figure 8) between the tracks and the ground as well as the variations of voltage (dv/dt). A comparison of the impedance curves between the two PCB layouts for this configuration is shown in Figure 22, where we observe capacitive behaviors between the whole circuits and the ground. As shown in Figure 17, the optimized model has a lower overall surface area which causes a decrease in the coupling capacitances Cp. These findings are confirmed by results shown in Figure 22 where we notice an increase of the impedance curves which will permit the reduction of the common mode current and therefore the voltage VCM spectrum is reduced. This validates the relevance of the experiments optimization results.

2) CONFIGURATION 2: ZDM MEASUREMENTS

The measurement of DM impedance is made using the configuration shown in Figure 23. Using this setup, the measurement is made at the location of the diode and the MOSFET is replaced with a short circuit. For the DM, this difference is important because the DM depends on the parasitic inductances of the tracks as well as the variations in current (di/dt). The Figure 24 shows the comparison between the measurements for the two PCB layouts. In this figure, we notice the difference between the resonant frequencies as well as the impedance amplitude. These results are consistent especially in the frequency band of [1MHz, 10MHZ], where we observe an inductive behavior of the whole circuit. The optimized layout has lower impedance which allowed the reduction of the differential mode voltage over this entire interval.

V. CONCLUSION

In this paper, an optimization method for the automatic PCB layout design respecting the EM disturbances has been proposed. This approach uses a GA implemented in optimization toolbox coupled with a Dijkstra algorithm in order to automatically generate PCB layouts for the chopper circuit. Then these layouts are analyzed one by one for the purpose of retaining a layout, which has enhanced EMC performance. Indeed, an automatic modelling and simulation methodology using the ANSYS EM tools have been presented. After computing all the parasitic elements using ANSYS Q3D, the complete circuit has been simulated using ANSYS SIMPLORER's. Once the disturbances such as VCM and

VDM are computed, the waveforms from transient simulations are imported into the optimization process. The algorithm proceeds until the given objective function is satisfied. The obtained simulation results by the proposed automatic optimization process were compared with reference PCB layout simulation results. The findings demonstrate that, for the selected frequency range, the optimized layout has a better performance than the layout from manual design. Following that, the PCB layout was made for experimental validation. The measurements show good agreement with the simulations, which shows the efficiency of this work. This approach could help engineers to guarantee PCB designs with optimum EMC constraints and save the designer's time to reduce the costly cycle for EMI/EMC testing. The placement of the components has an important impact on the couplings which, consequently, can be affecting the conducted disturbances. This optimization method will be further improved. Future activities will be explored by considering the placement of components with routing optimization.

REFERENCES

[1] B. Hao, Y. Mei, and P. Ning, "A hybrid genetic algorithm for automatic layout design of power module," in *Proc. 18th Int. Conf. Electron. Packag. Technol. (ICEPT)*, Aug. 2017, pp. 1143–1146.

[2] Q. Chen, X. Yang, J. Liu, and Z. Wang, "Practical design considerations for IPEM-based PFC converter employing CoolMOS and SiC diode," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf.*, Mar. 2006, pp. 1693–1698.

[3] I. Abari, A. Lahouar, M. Hamouda, J. B. H. Slama, and K. Al-Haddad, "Fault detection methods for three-level NPC inverter based on DC-bus electromagnetic signatures," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5224–5236, Jul. 2018.

[4] A. Bhargava, D. Pommerenke, K. W. Kam, F. Centola, and C. W. Lam, "DC–DC buck converter EMI reduction using PCB layout modification," *IEEE Trans. Electromagn. Compat.*, vol. 53, no. 3, pp. 806–813, Aug. 2011.

[5] N. Puqi, W. Fei, and K. D. T. Ngo, "Automatic layout design for power module," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 481–487, Jan. 2013.

[6] M. Hammadi, J. Y. Choley, and O. Penas, "Layout optimization of power modules using a sequentially coupled approach," *Int. J. Simul. Model.*, vol. 10, no. 3, pp. 122–132, Sep. 2011.

[7] C. Martin, J. M. Guichon, J. L. Schanen, and R. Pasterczyk, "Gate circuit layout optimization of power module regarding transient current imbalance," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 541–546.

[8] P. Ning, X. Wen, Y. Li, and X. Ge, "An improved automatic layout method for planar power module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 3080–3085.

[9] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Stray inductance reduction of commutation loop in the P-cell and N-cell-based IGBT phase leg module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, Jul. 2014.

[10] J. Ardizonni, "A practical guide to high-speed printed-circuit-board layout," *Analog Dialogue*, vol. 39, no. 9, Sep. 2005, pp. 1–6.

[11] T. Hubing, "PCB EMC design guidelines: A brief annotated list," in *Proc. IEEE Symp. Electromagn. Compat. Symp. Rec.*, Boston, MA, USA, Aug. 2003, pp. 34–36.

[12] O. Mühlfeld and F. W. Fuchs, "Comprehensive optimization method for thermal properties and parasitics in power modules," in *Proc. IEEE Energy Convers. Congr. Expo.*, Atlanta, GA, USA, Sep. 2010, pp. 2266–2271.

[13] T. De-Oliveira, J.-L. Schanen, J.-M. Guichon, and L. Gerbaud, "Optimal stray magnetic couplings for EMC filters," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1619–1627, Jul. 2013.

[14] S. Mandray, J. Guichon, J. Schanen, S. Vieillard, and A. Bouzourene, "Automatic layout optimization of a double sided power module regarding thermal and EMC constraints," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 1046–1051.

[15] P. Ning, X. Wen, Y. Mei, and T. Fan, "A fast universal power module layout method," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 4132–4137.

[16] M. Ferber, R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, and A. Nagari, "Power efficiency and EMI attenuation optimization in filter design," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 6, pp. 1811–1818, Dec. 2018.

[17] J.-. Schanen, L. Jourdan, and J. Roudet, "Layout optimization to reduce EMI of a switched mode power supply," in *Proc. IEEE 33rd Annu. IEEE Power Electron. Spec. Conf.*, Cairns, QLD, Australia, vol. 4, Jun. 2002, pp. 2021–2026.

[18] F. Viani, F. Robol, M. Salucci, and R. Azaro, "Automatic EMI filter design through particle swarm optimization," *IEEE Trans. Electron. Compat.*, vol. 59, no. 4, pp. 1079–1094, Aug. 2017.

[19] B. Touré, J.-L. Schanen, L. Gerbaud, T. Meynard, J. Roudet, and R. Ruelland, "EMC modeling of drives for aircraft applications: Modeling process, EMI filter optimization, and technological choice," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1145–1156, Mar. 2013.

[20] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A multi-loop method for minimization of parasitic inductance in GaN-based high-frequency DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4728–4740, Jun. 2017.

[21] S. Busquets-Monge, J.-C. Crebier, S. Ragon, E. Hertz, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D. Lindner, "Design of a boost power factor correction converter using optimization techniques," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1388–1396, Nov. 2004.

[22] W. Belloumi, A. Bréard, J. B. H. Slama, and C. Vollaire, "Impact of layout on the conducted emissions of a DC–DC converter using numerical approach," in *Proc. 15th Int. Multi-Conf. Syst., Signals Devices (SSD)*, Hammamet, Tunisia, Mar. 2018, pp. 287–291.

[23] J. B. H. Slama, S. Hrigua, F. Costa, B. Revol, and C. Gautier, "Relevant parameters of SPICE3 MOSFET model for EMC analysis," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Austin, TX, USA, Aug. 2009, pp. 319–323.

[24] E. Rondon-Pinilla, F. Morel, C. Vollaire, and J.-L. Schanen, "Modeling of a buck converter with a SiC JFET to predict EMC conducted emissions," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2246–2260, May 2014.

[25] J. B. H. Slama and W. Labiedh, "Library of EMC models for passive components and printed circuit board," in *Proc. 16th IEEE Medit. Electrotech. Conf.*, Mar. 2012, pp. 325–330.

[26] G. Sandhiya and R. Jothikumar, "Enhanced K-means with Dijikstra algorithm for energy consumption in wireless sensor network," in *Proc. 10th Int. Conf. Intell. Syst. Control (ISCO)*, Jan. 2016, pp. 1–5.

[27] M. Nosrati, R. Karimi, and H. A. Hasanvand, "Investigation of the ∗ (star) search algorithms: Characteristics methods and approaches," *World Appl. Program.*, vol. 2, no. 4, pp. 251–256, 2012.

[28] O. V. G. Swathika and S. Hemamalini, "Prims-aided Dijkstra algorithm for adaptive protection in microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1279–1286, Dec. 2016.

[29] R. Y. Chang, W. H. Chung, and S. J. Lin, "A* algorithm inspired memory-efficient detection for MIMO systems," *IEEE Wireless Commun. Lett.*, vol. 1, no. 5, pp. 508–511, Oct. 2012.

[30] L. Coppola, D. Cottet, and F. Wildner, "Investigation on current density limits in power printed circuit boards," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 205–210.

[31] Y. Wang, S. W. H. de Haan, and J. A. Ferreira, "Thermal design guideline of PCB traces under DC and AC current," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 1240–1246.

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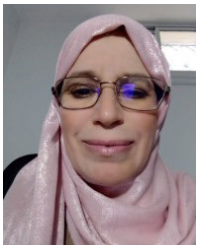

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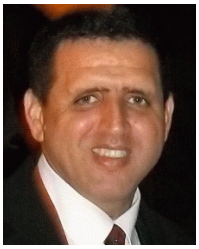

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