Thermal Simulation and Characterization of GaN HEMT using Gate Resistance Thermometry and Thermoreflectance imaging

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***Abstract* — Two electrical methods and one optical method are used, in order to measure the temperature of the hot spot of a 150nm, 2x150µm GaN HEMT. One of the electrical methods is based on Gate Resistance Thermometry (GTR) [1] and the other one is based on the On State resistance Ron obtained from Id(Vgs,Vds) drain current characterization [2]. The optical one uses the reflectivity variation principle to measure the surface temperature and is based on CCD-thermoreflectance [3]. The measurement results are supported by nonlinear simulation, using Finite Element Method (FEM). The use of the GTR electrical method allows a characterization of the temperature along the gates close to the hot spot region and averages the temperature over the gate width. This method demonstrates a relative linearity in the variation of thermal resistance as function of the applied power dissipation and notably a higher thermal resistance value compared to the conventional way of R_{ON} extraction. We may notice that with the On State resistance, the average is realized over the Source-Drain length. The optical method based on the ThermoReflectance (TR) allows a measurement of the surface temperature of the component at the hot spot. The values obtained are consistent with those found by electrical methods and FEM simulation up to 10W/mm.**

***Index Terms* — GaN HEMT, Gate Resistance Thermometry, Thermoreflectance, temperature, FEM thermal simulation, 10W/mm.**

I. Introduction

In recent years, the advancement of applications based on the use of GaN HEMT transistors has allowed to obtain power performances in several fields of activity. However, these components are subjected to high power densities which induce high temperatures affecting their reliability and degrading their electrical performances. Thus, the thermal study of these power components becomes critical. In this paper, thermal simulations as well as thermal characterization by several methods are performed and compared in order to extract the temperature of the device and thermal resistance

II ELECTRICAL MEASUREMENTS OF THERMAL RESISTANCE

In order to measure the temperature of the UMS 2x150µm GaN HEMT two different electrical methods are used. The "Ron method" involves two steps: (a) calibration step and (b) measurement step. The detailed procedure of this measurement technique can be found in [2]. The second method involves the calibration of the gate [1].

II.1. R_{th} measurement using R_{ON} calibration method

The first step (Temperature calibration) is used to express the device on-state resistance (R_{ON}) as a function of the temperature; this temperature is provided extrinsically by a thermal chuck on which the Device Under Test (DUT) is placed. The calibration is performed by varying the temperature of the thermal chuck, typically up to 125°C for a quiescent bias point (Vgs = Vds = 0V). The R_{ON} value is extracted from the linear region of the device characteristics using pulsed I(V) measurement for various chuck temperatures. Figure 1 shows that the extracted resistance R_{ON} increases linearly with temperature:

$$R_{ON} = a_T.\Delta T + b \qquad (1)$$

The second step (Power measurement) is used to express R_{ON} as a function of the power dissipation. It can be obtained by applying different drain biasing conditionsV_{DS0} for V_{GS0} = 0V.

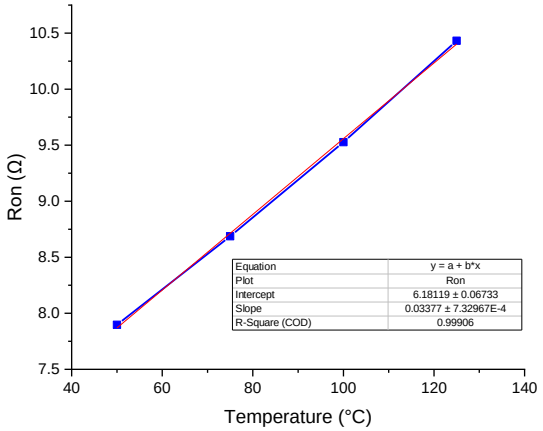

Figure 1 : On-state resistance RON vs thermal Chuck temperature

The extracted R_{ON}, is a linear function of the dissipated power (Figure 2), and it can be expressed in the following form:

$$R_{ON} = a_P . P_{diss} + b \quad (2)$$

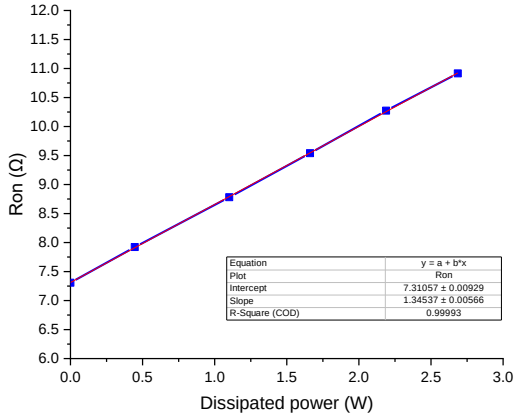

Figure 2 : On-state resistance R_{ON} vs dissipated power

From the two previous equations (1) and (2), it is possible to express the temperature variation as a function of dissipated power because b is the same for (1) and (2).

$$a_T . \Delta T = a_P . P_{diss} \quad (3)$$

With: $b = R_{ON}$ at $T = T_0$ or $P_{diss} = 0\ W$

The thermal resistance can be obtained using "Thermal Ohm's Law" as the ratio of the slope coefficients of (1) and (2)

$$R_{th} = \frac{\Delta_T}{P_{diss}} = \frac{a_p}{a_T} \quad (4)$$

Note that the thermal resistance is a constant value and the extracted thermal resistance is $R_{th} = 39.8°C/W$

II.2. R_{th} measurement using Gate Resistance Thermometry

The special interest of the transistor used in this experiment relies on the fact that the gates are connected on both side as shown in Figure 7 b) and can be used as a temperature sensor. The two terminals of the gate are set to a small difference of electrical potentials allowing a small current flow to take place between them. The gate resistance can be deduced and its variation with the temperature can be monitored. The first assumption is that the signal injected in the gate probe resistance is negligeable to increase the temperature of the device. The first step consists in a calibration of the resistance of the gate versus temperature provided by the thermal chuck. No dissipated power is applied, and the drain is grounded.

This calibration curve is shown in Figure 3 and exhibits that the gate resistance increases linearly with the temperature of the thermal chuck and can be expressed by:

$$R_g = a_T . \Delta T + b \quad (5)$$

where $a_T = 0.00347$ and b = 11.47. These values are consistent with a gate metal temperature coefficient around 3.4E-4 corresponding to the ratio a_T/b and mainly due to Au metal.

The second step consists of expressing R_g as a function of the different dissipated powers applied in the channel thanks to different DC drain biasing voltages V_{ds}. The dissipated power in the channel creates an increase of the temperature of the channel. This thermal energy is then transferred to the rest of the transistor by conduction and notably to the gates. Measurements show in Figure 4 that the gate resistance R_g is a quadratic function of the dissipated power.

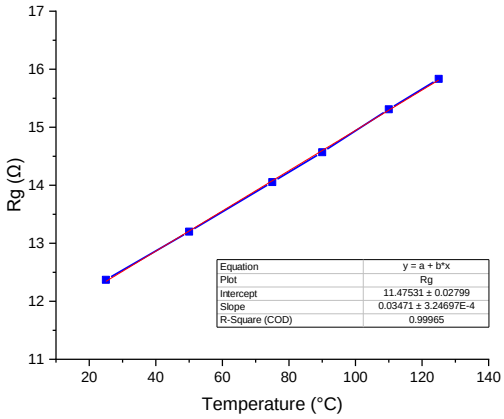

Figure 3 : Gates resistor vs thermal chuck temperature

The R_g resistance can therefore be expressed as a function of power as follows:

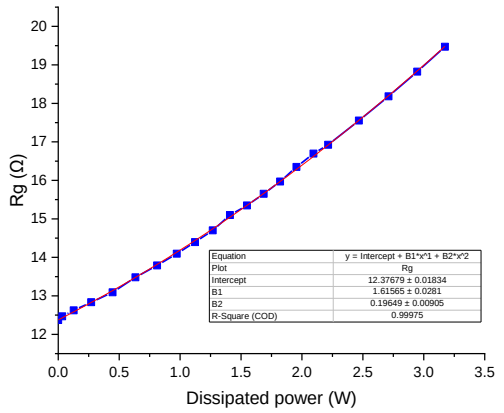

Figure 4 : Gate resistor vs dissipated power

$$R_g(P_{diss}) = a_2 P_{diss}^2 + a_3 P_{diss} + b \quad (6)$$

From (5) and (6), it is possible to express the temperature rise also as a quadratic function of power dissipation:

$$\Delta T = \frac{a_2}{a_T} {P_{diss}}^2 + \frac{a_3}{a_T} P_{diss} \quad (7)$$

Thermal resistance can be expressed, according to "Ohm's Law" for Thermal Resistance, in terms of temperature difference and power dissipation using the following form:

$$R_{th} = \frac{\Delta T}{P_{diss}} \quad (8)$$

The measurements show that the thermal resistance is not constant and varies according to the dissipated power (Figure 5), it can be expressed as:

$$R_{th} = \frac{a_2}{a_T} P_{diss} + \frac{a_3}{a_T} \quad (9)$$

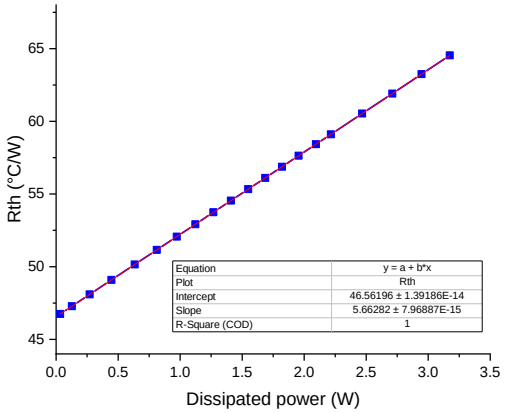

Figure 5 : R_{th} vs dissipated power

The temperature is maximum in the channel below the gate on the drain side because the electric field is the most intense in this area (Figure 6), using the gates as a temperature sensor allows for a more accurate temperature measurement. Finally, the temperature averaged along the gates can be expressed according to the following equation:

$$T = \frac{a_2}{a_T} P_{diss}^2 + \frac{a_3}{a_T} P_{diss} + T_0 \quad (10)$$

III. OPTICAL MEASUREMENT BY THERMOREFLECTANCE OF THERMAL RESISTANCE

The reflectivity of the material varies with the variation of its temperature [3], so it is possible to express the relationship between the relative change in reflectance (ΔR/R0) and the surface temperature by:

$$\frac{\Delta R}{R_0} = C_{th}.\Delta T \quad (14)$$

The coefficient C_{th} depends on the surface of the material and the wavelength of the excitation LED. This coefficient is obtained during calibration by placing the transistor on a thermal stage. The reflectance is measured for two different temperatures 25°C and 100°C respectively. It is important to select the optimum wavelength that gives the highest C_{th} value for a better measurement sensitivity.

III. 1. CALIBRATION

Considering the SiN passivation layer, a near UV wavelength of 365 nm is used to measure the temperature on the AlGaN layer through the SiN layer as close as possible to the hot spot.

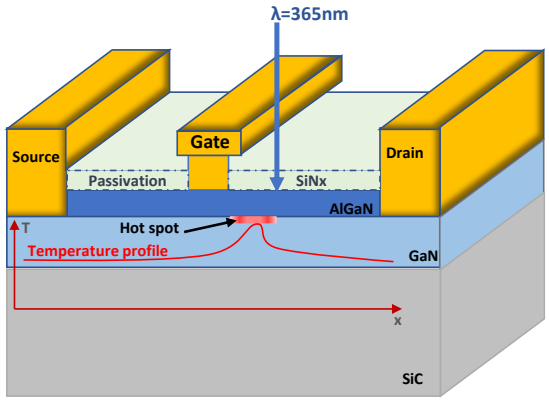

Figure 6 : Simplified structure of GaN HEMT transistor showing measurement spots and respective wavelengths used.

The TR coefficient measured through the calibration process is $C_{th} = -3x10^{-3} \pm 1x10^{-5}\ °C^{-1}$ for λ=365nm

III. 2. MEASUREMENTS

A steady state measurement has been performed for several dissipated powers near the gates between the two air bridges as shown in Figure 7 with the TR and CCD images of the 2x150µm transistor, illustrating the hot spot regions of the device.

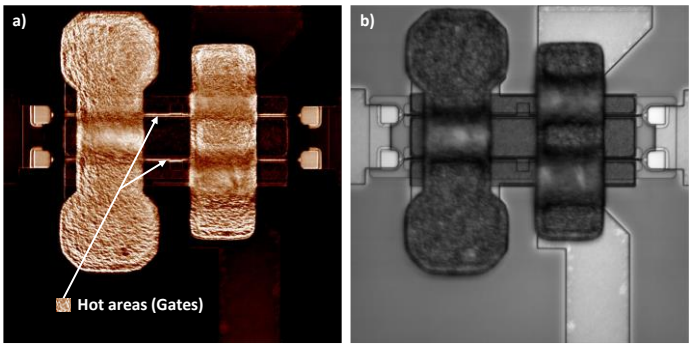

Figure 7. a) TR image showing hot areas **b)** CCD camera image during measurement

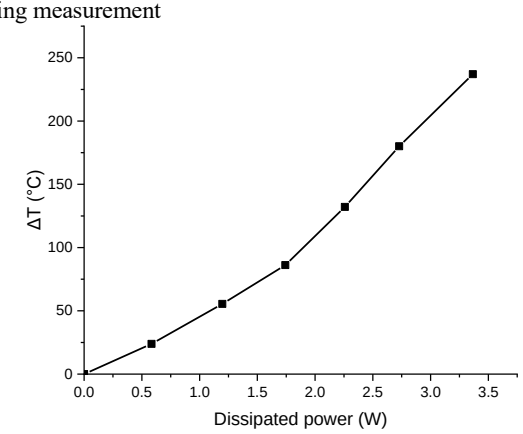

Figure 8 : Temperature increase versus dissipated power

The results are similar to those obtained by GTR method which exhibit a variable thermal resistance versus dissipated power.

IV. NUMERICAL SIMULATION

A finite element thermal simulation using Salome-Meca software is performed in order to validate the measurement results. The nonlinear properties of materials are taken into consideration. Table 1 shows the equation used to define the thermal response of the different materials used in this work.

$$k(T) = k_{300} \cdot \left(\frac{T}{300}\right)^{-\alpha} \quad (15)$$

Material	ρ *(kg/m³)*	C_p *(J/kg/K)*	k_{300} *(W/m/K)*	α
Au	*19300*	*137*	*310*	*-*
GaN	*6100*	*490*	*160*	*1.45*
SiC	*3220*	*690*	*340*	*1.5*
Nucleation Layer	*6100*	*490*	*6.7*	*2.7*

Table 1. Material properties [6]

The device structure of a 2x150µm is considered symmetric with respect to X-axis and Y-Axis and therefore only the quarter of the device structure is used for the simulation. Meshing the device structure is an important aspect of device simulations. The mesh density should be fine in the device areas where the temperature and heat flux vary rapidly (99282 surface elements and 531342 volume elements).

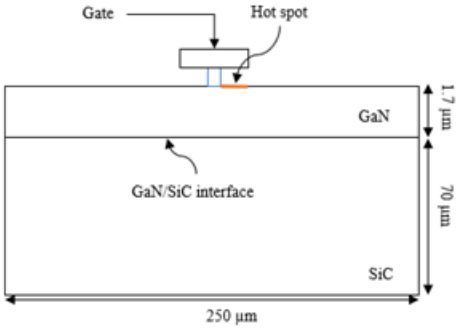

Figure 9. Quarter of the simplified geometry of the transistor

The boundary conditions are: an initial temperature of 25 °C, imposed at the baseplate of the SiC material, a surface heat flux density φ applied to the hot spot (Figure 9) described as:

$$\varphi = (k(T)\nabla T) \cdot \vec{n} = \frac{P_{DISS}}{4 \cdot S_g} \quad (16)$$

where S_g section of the hot spot and $P_{DISS} = I_{DS0} \cdot V_{DS0}$

V. DISCUSSIONS

Figure 10 presents a comparison between simulation and the various measurements performed on the device. Results reveal a good agreement between measurements and simulation on a large range of dissipated power. This demonstrates on one hand the possibility of estimating the operating temperature of the transistor by means of pure thermal simulation, and on the other hand the complementarity of the electrical based and optical based measurements.

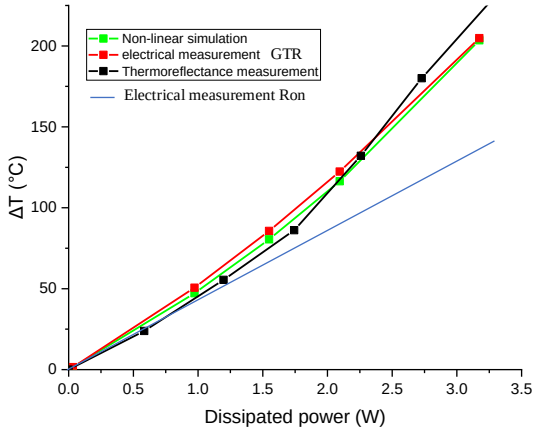

Figure 10. Comparison of the different temperature results

VI. CONCLUSION

The temperature of a 150nm, 2x150µm GaN HEMT has been determined by several measurement methods including Ron thermometry, Gate Resistance Thermometry, Thermoreflectance imaging as well as FEM simulation for a power density up to 10W/mm. The R_{ON} method exhibits a constant thermal resistance of 40°C/W leading to a linear variation of temperature versus dissipated power. The other methods or the FEM simulation provide very close results even at high dissipated power. The break in the slope of the thermoreflectance results may be due to the calibration of thermoreflectance coefficient Cth performed only between 25°C and 100°C which is probably not sufficient to reach the best accuracy in the temperature determination at very high temperature and moreover for a semiconductor material.

ACKNOWLEDGEMENT

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REFERENCES

[1] G. Pavlidis and al, "Characterization of AlGaN/GaN HEMTs Using Gate Resistance Thermometry," in *IEEE Trans. on Electron Devices*, vol. 64, no. 1, pp. 78-83, Jan. 2017

[2] R. Sommet and al, "Thermal modeling and measurements of AlGaN/GaN HEMTs including thermal boundary resistance", Microelectronics Journal, Volume 43, Issue 9, 2012, Pages 611-617

[3] D. Kendig *et al.*, "UV Thermal Imaging of RF GaN Devices with GaN Resistor Validation," *2018 91st ARFTG (ARFTG)*, 2018, pp. 1-4

[4] Raymond A. Serway "Principles of Physics (2nd Edition) Fort Worth, Texas, London, Saunders College Pub p602

[5] A. A. Wilson and al, "Kapitza Resistance at the Two-Dimensional Electron Gas Interface," *2019 18th IEEE ITherm*, 2019, pp. 766-771

[6] Amar, A.; Radi, B.; El Abdelkhalak, H. Electrothermal Reliability of the High Electron Mobility Transistor (HEMT). *Appl. Sci.* **2021**, *11*, 10720.